



**WELCOME To**

**ISSCC 2014  
SESSION 23  
ENERGY  
HARVESTING**

# **A 0.15-V Input Energy Harvesting Charge Pump with Switching Body Biasing and Adaptive Dead-Time for Efficiency Improvement**

Jungmoon Kim<sup>1,2</sup>, Philip K. T. Mok<sup>1</sup>, and Chulwoo Kim<sup>2</sup>

***<sup>1</sup>Hong Kong University of Science and Technology, Hong Kong***

***<sup>2</sup>Korea University, Korea***

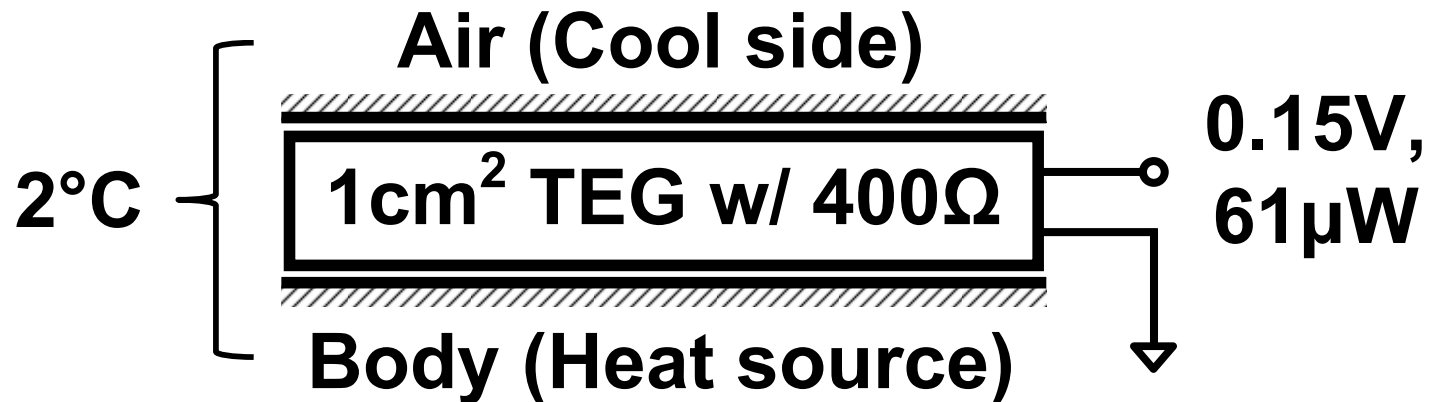


# Outline

- **Motivation**
- **Proposed Architecture**
  - **Switching body biasing (SBB)**
  - **Adaptive dead-time (AD)**
  - **Switch-conductance (SW-G) enhancement**
- **Measurement Results**
- **Conclusions**

# Small-Scale Energy Harvesting

- **Energy Harvesting (EH)**
  - Low voltage and low power condition
  - An example of thermoelectric EH\*



- **Low-input-voltage ( $V_{IN}$ ) up-converters**
  - Inductive type vs. Capacitive type

\* MPG-D751, Micropelt, Germany.



# Inductive DC-DC for Low- $V_{IN}$

- **Inductive DC-DC Converters**

- External battery\* :  $V_{IN,MIN} = 20\text{mV}$
- External mechanical switch\*\* :  $V_{IN,MIN} = 35\text{mV}$
- Post-fabrication process\*\*\* :  $V_{IN,MIN} = 95\text{mV}$
- Transformer† :  $V_{IN,MIN} = 40\text{mV}$
- LC-tank oscillator†† :  $V_{IN,MIN} = 50\text{mV}$

- **Challenges**

- **Electrical start-up**
- **Bulky components**

\* Carlson, *VLSI* 2009

\*\* Y. K. Ramadass, *ISSCC* 2010

\*\*\* P-H Chen, *ISSCC* 2011

† J.-P. Im, *ISSCC* 2012

†† H.-Y. Tang, *VLSI* 2012

# Capacitive DC-DC for Low- $V_{IN}$

- **Capacitive DC-DC Converters**
  - No bulky inductor
  - Not start-up issue, just min.  $V_{DD}$  issue
- **Challenges**
  - Voltage conversion efficiency (VCE)
  - Power conversion efficiency (PCE)
  - Low- $V_{IN}$  operation
    - Meindl limit
    - Conduction loss ( $R_{ON}$  drop)
    - Dead-time ( $T_D$ ) limitations

# Meindl Limit\*

- **Fundamental limit on signal transfer for binary switching transition**

$$\text{Min. } V_{DD} = 2\ln\left(2\frac{kT}{q}\right) \cong 52\text{mV} \cdot \ln\left(1 + \frac{S_S}{60\text{mV}}\right) \text{ at } 300^\circ\text{K}$$

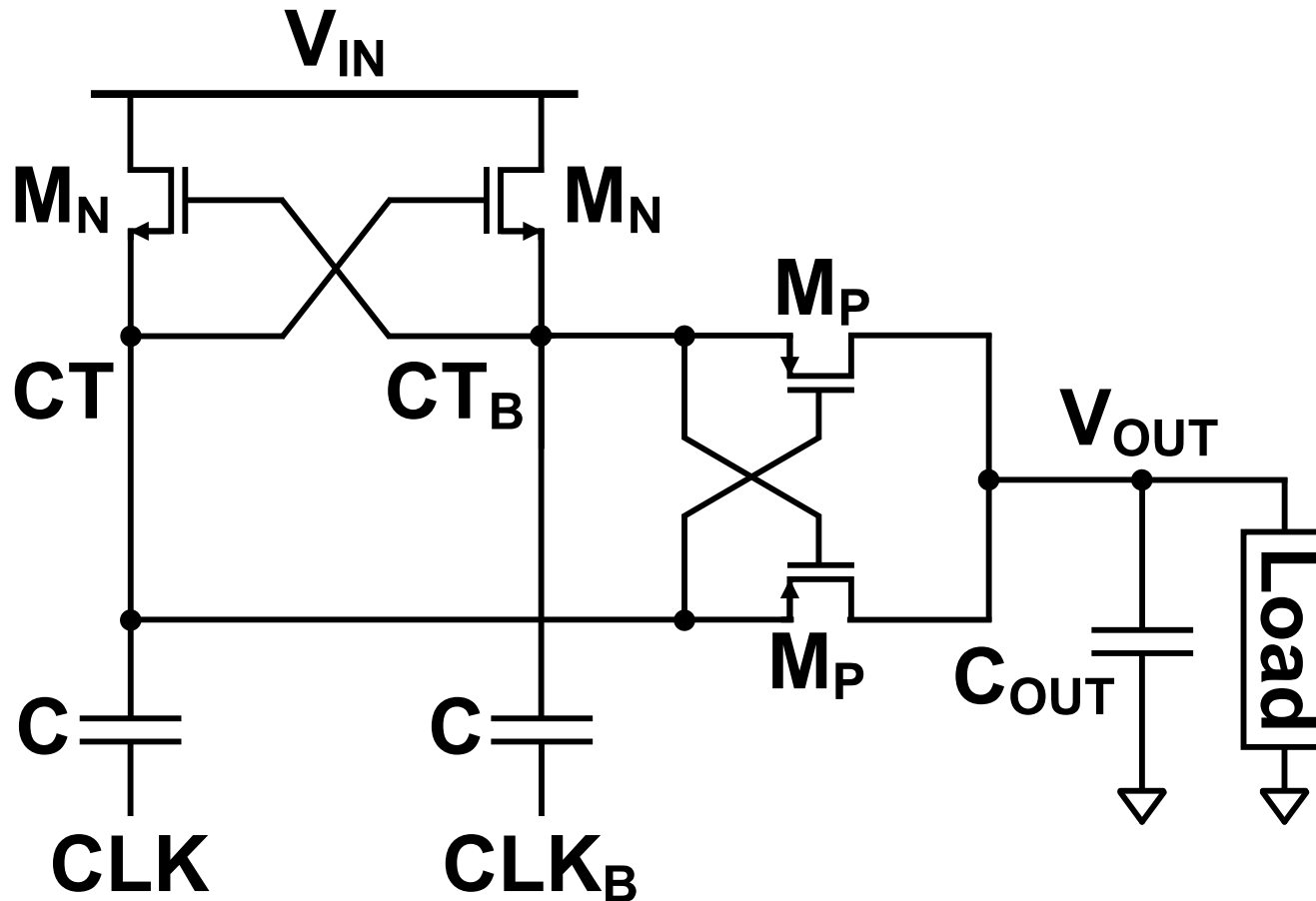
- Min.  $V_{DD}$  depends on subthreshold swing ( $S_S$ )\*\*
  - $S_S = 60\text{mV/dec.} \sim 100\text{mV/dec.}$
  - Min.  $V_{DD} = 36\text{mV} \sim 50\text{mV}$
- **Capacitive converter limit = Meindl limit**

\* J. D. Meindl and A. J. Davis, *JSSC* 2000, pp 1515-1516.

\*\* Bo Zhai *et al.*, *TVLSI* 2005, pp 1239-1252.

# Conventional Doublers (1)

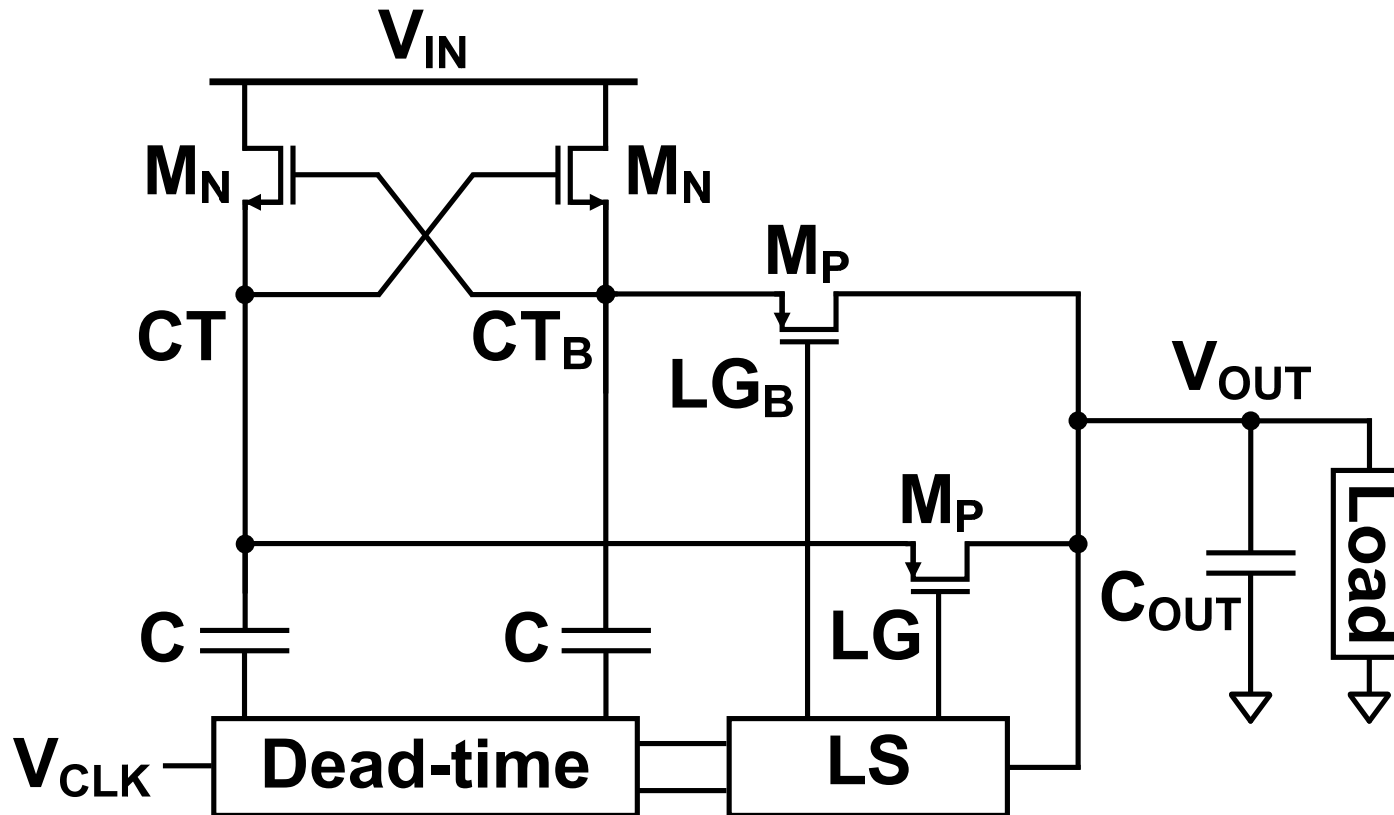
- **CP-cross w/ cross-coupled load switches\***



\* Y. Nakagome *et al.*, *JSSC* 1991, pp 465-472.

# Conventional Doublers (2)

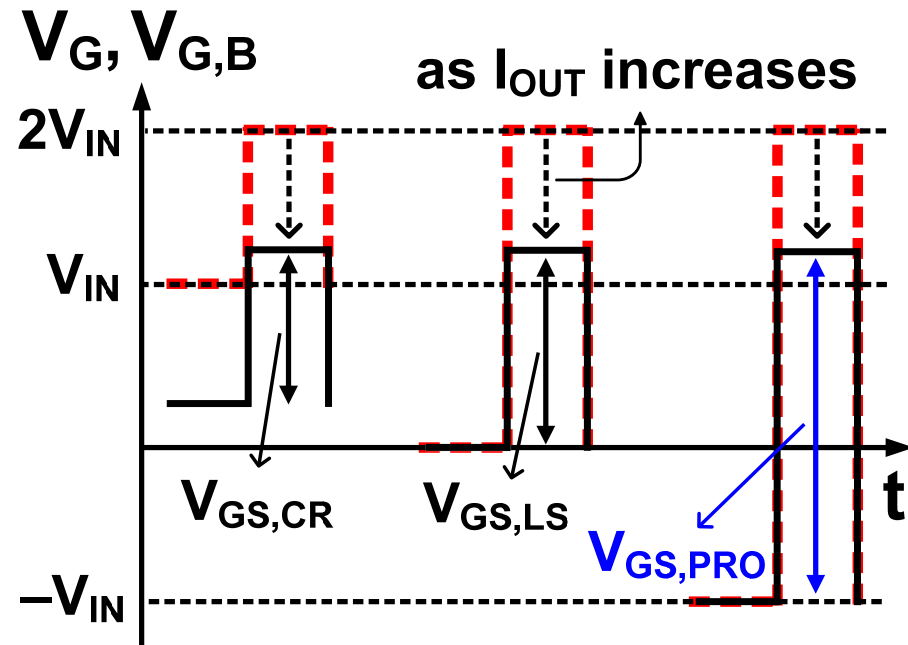
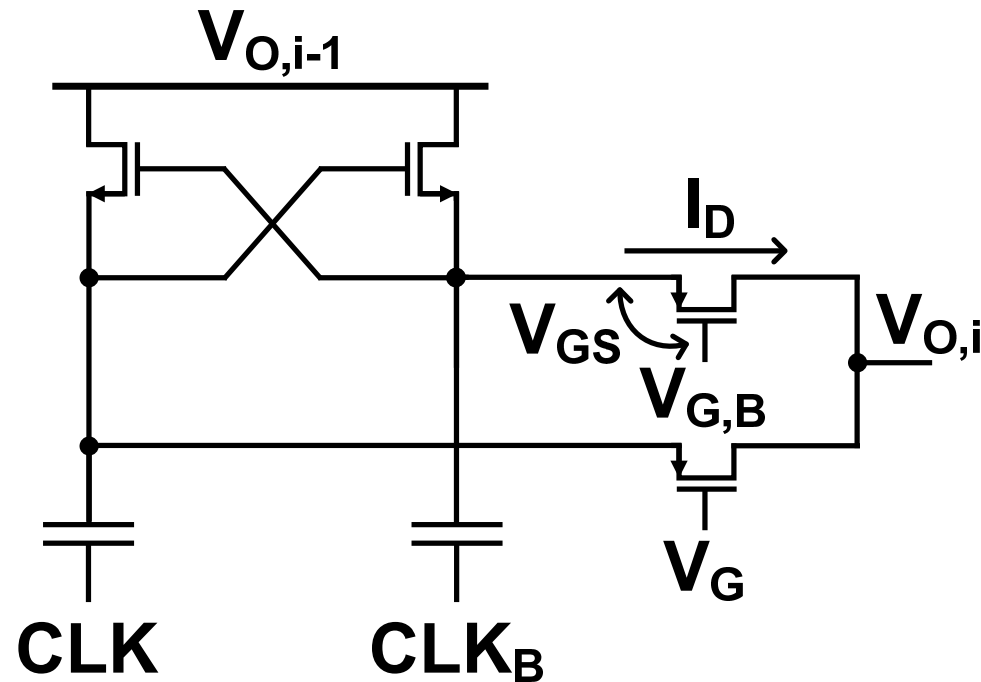
- **CP-LS w/ load switches driven by level shifter (LS)\***



\* P. Favrat *et al.*, JSSC 1998, pp 410-416.

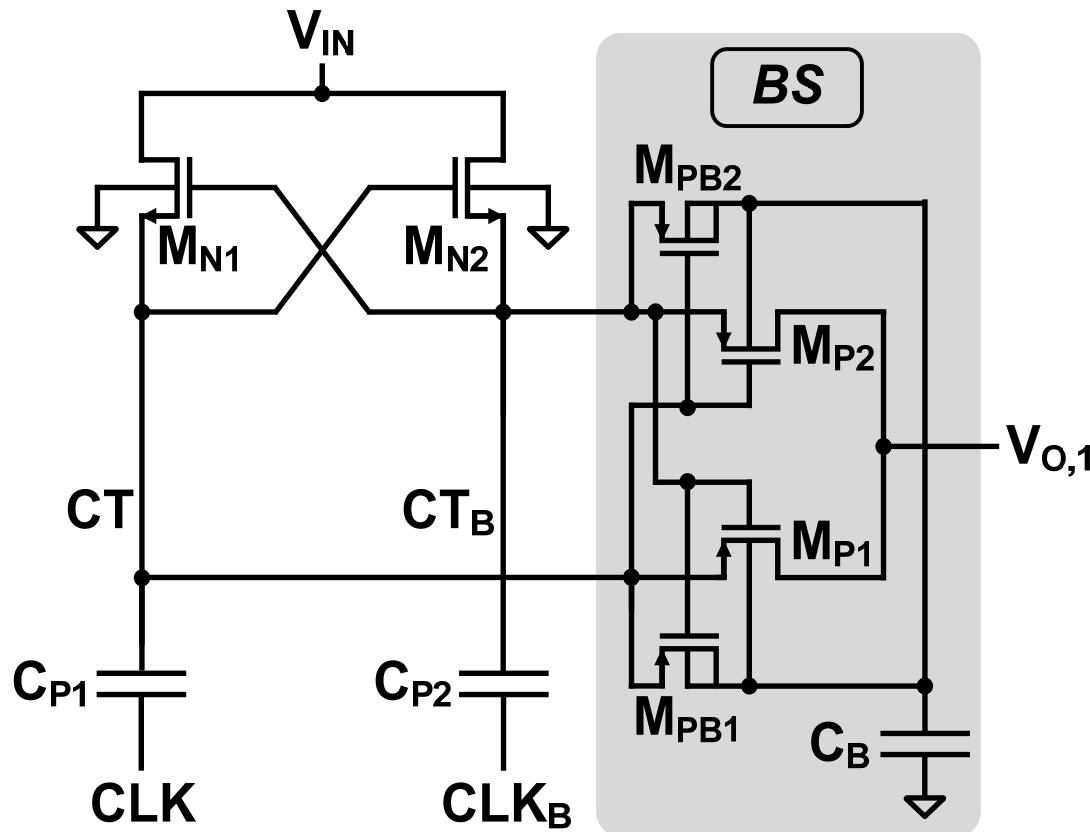
# Conductance Comparison

- Conductance degradation @ low  $V_{IN}$



# Bulk Switching (BS)

- **BS\*** : Poor VCE and PCE at low  $V_{IN}$



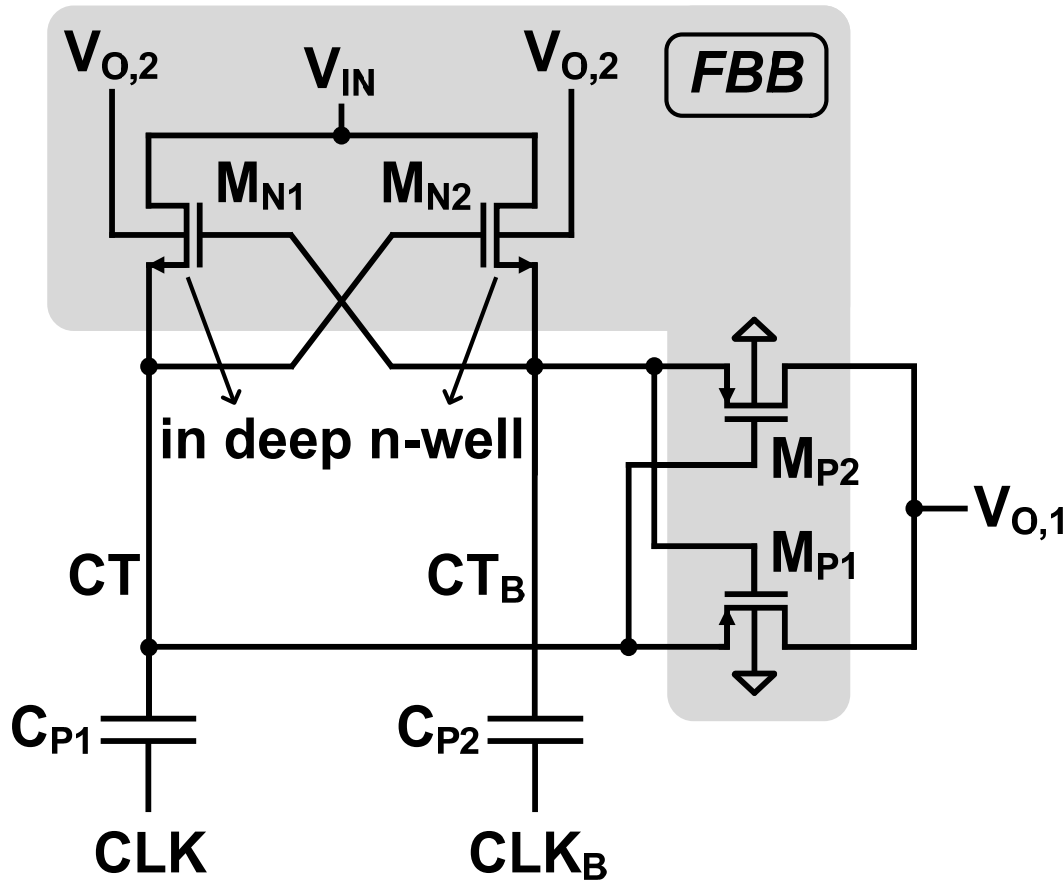
	$M_{N1}, M_{N2}$
ON	<b>Low <math>I_{ON}</math></b>
	<i>Reverse bias</i>
OFF	<b>Low leakage</b>
	<i>Reverse bias</i>

	$M_{P1}, M_{P2}$
ON	<b>Normal <math>I_{ON}</math></b>
	<i>No body effect</i>
OFF	<b>Normal leakage</b>
	<i>No body effect</i>

\* P. Favrat *et al.*, JSSC 1998, pp 410-416.

# Forward Body Biasing (FBB)

- **FBB\*** : Good VCE but poor PCE



	$M_{N1}, M_{N2}$
ON	High $I_{ON}$
	Forward bias
OFF	High leakage
	Forward bias

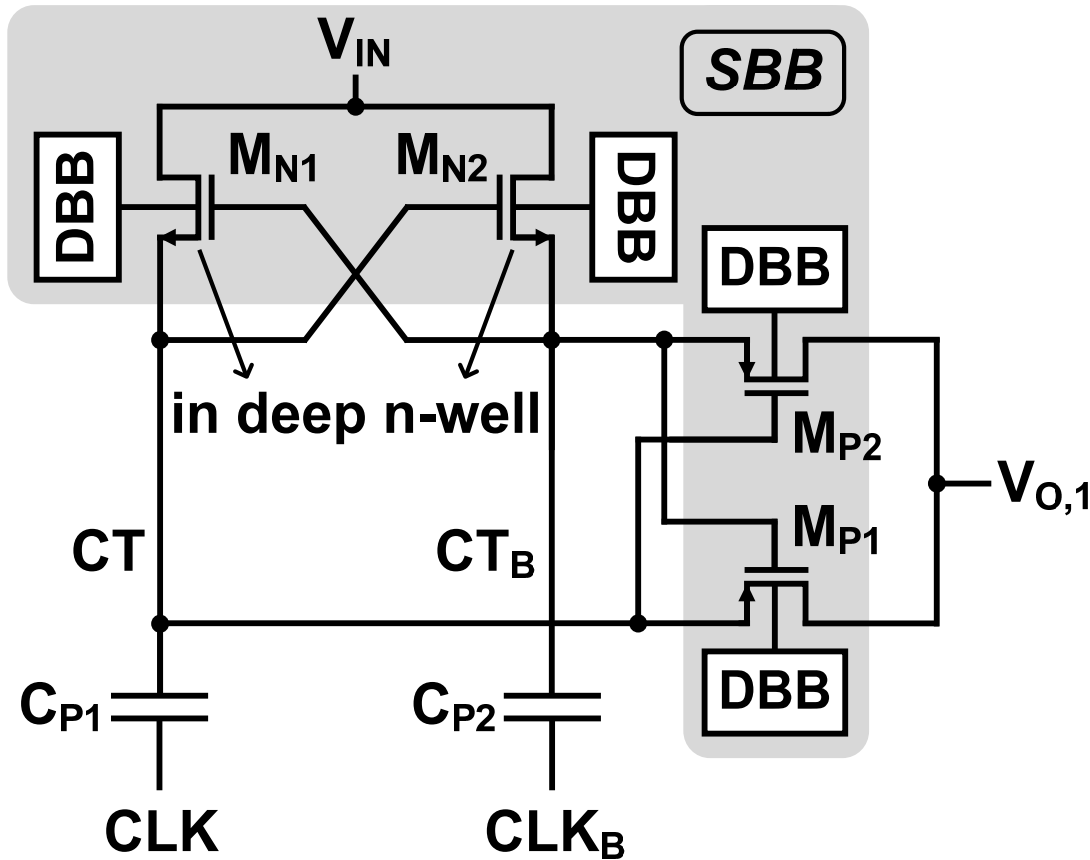
	$M_{P1}, M_{P2}$
ON	High $I_{ON}$
	Forward bias
OFF	High leakage
	Forward bias

\* P.-H. Chen *et al.*, *CICC* 2010, pp 239-242.



# Switching Body Biasing (SBB)

- Proposed SBB : How to control?

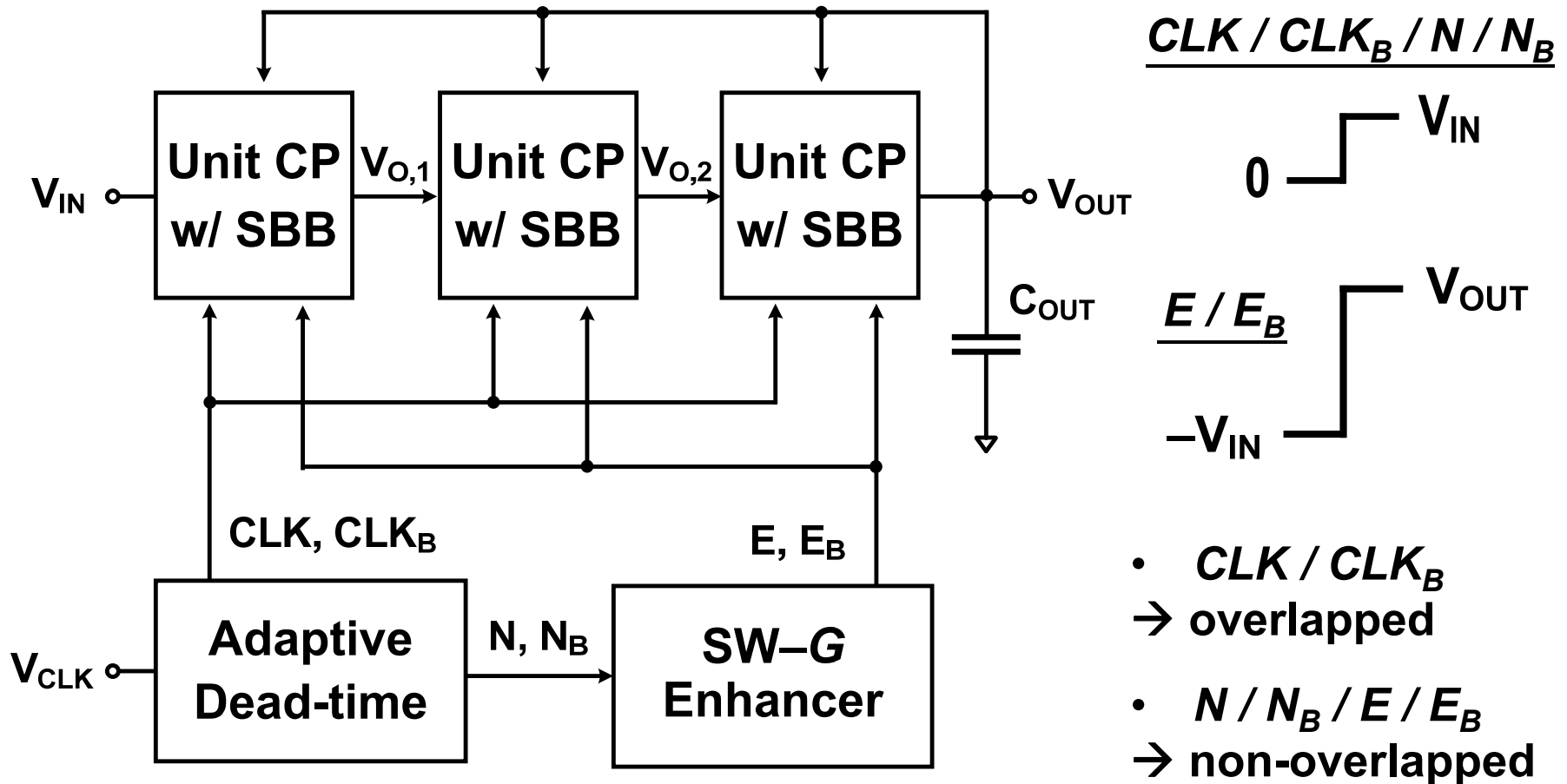


	$M_{N1}, M_{N2}$
ON	High $I_{ON}$
	Forward bias
OFF	Low leakage
	Reverse bias

	$M_{P1}, M_{P2}$
ON	High $I_{ON}$
	Forward bias
OFF	Low leakage
	Reverse bias

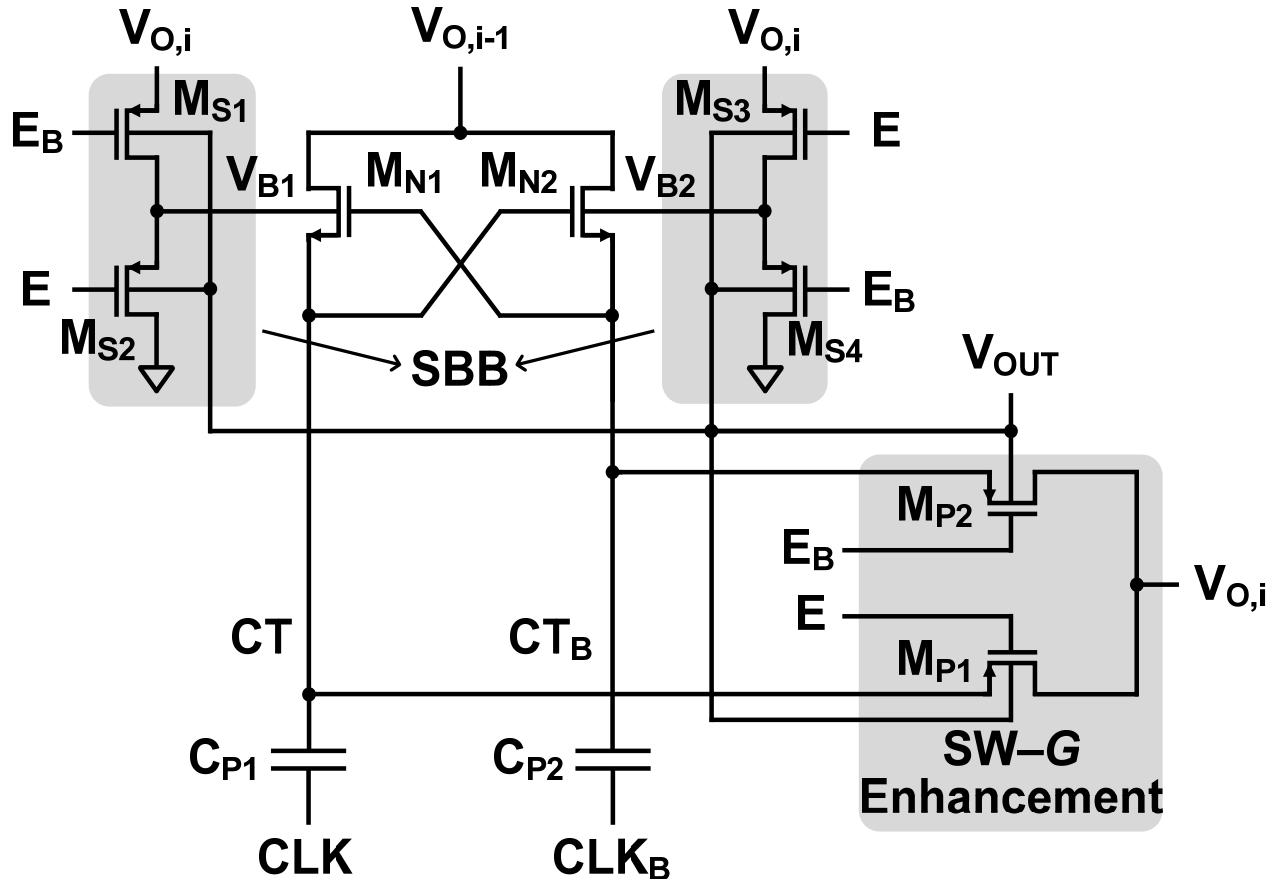
# Proposed CP Architecture

- Low  $V_{IN}$  operation and PCE improvement by three simple & cost-effective solutions



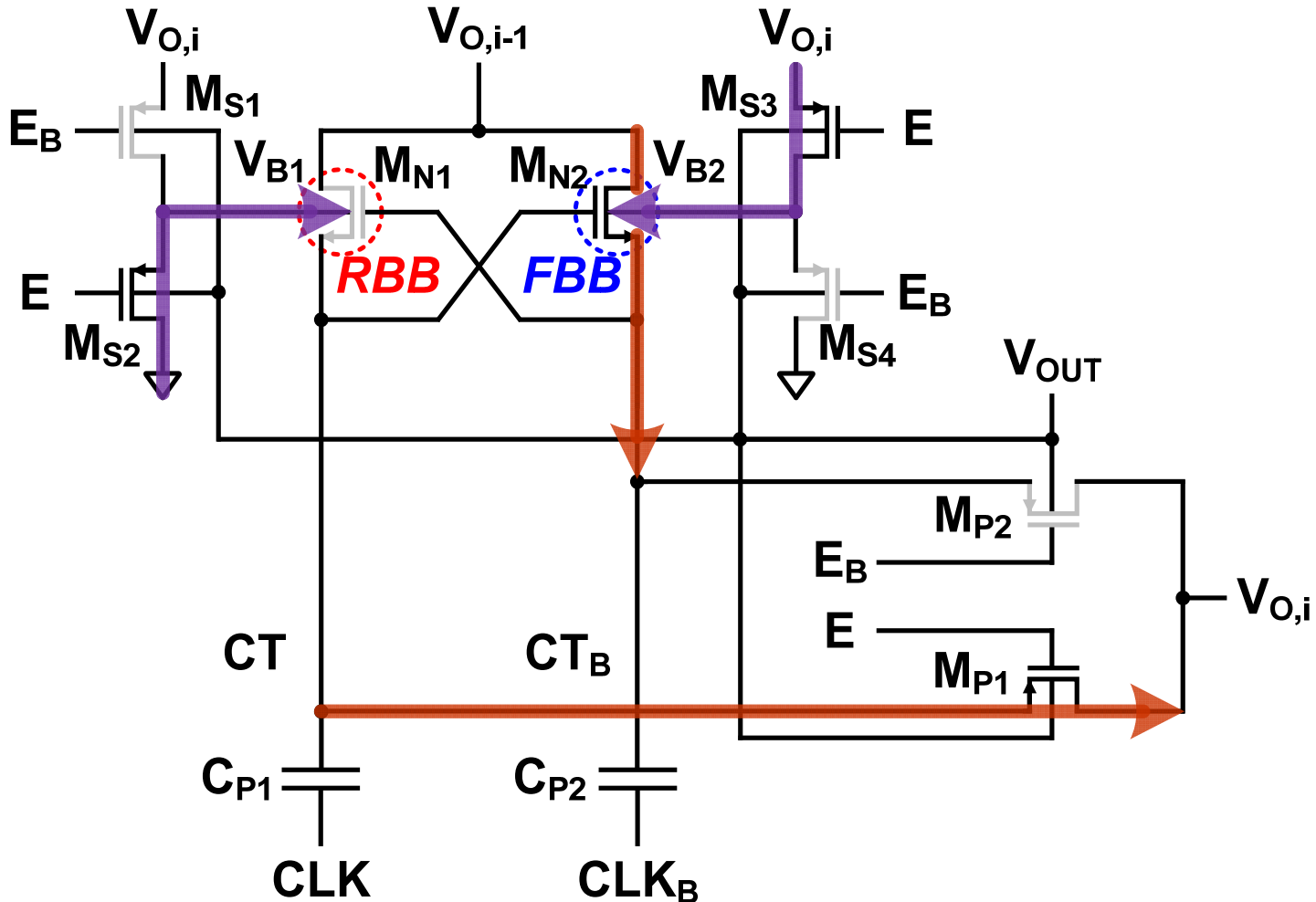
# Unit CP

- **SBB to maximize PCE**
- **SW-conductance enhancement for low  $V_{IN}$**



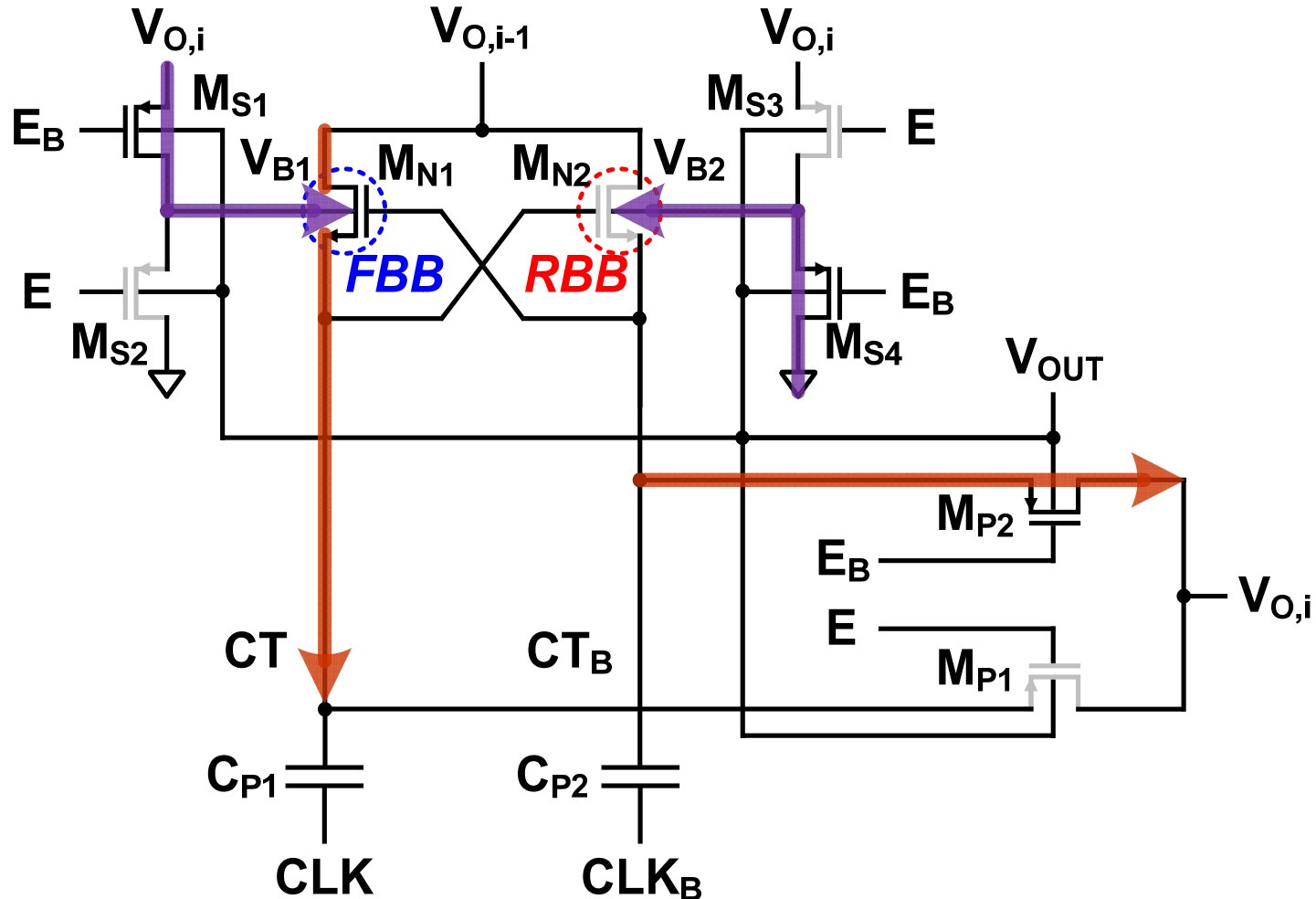
# SBB : CLK = High, E = Low

- $M_{N1}$  off  $\leftarrow$  RBB,  $M_{N2}$  on  $\leftarrow$  FBB



# SBB : CLK = Low, E = High

- $M_{N1}$  on  $\leftarrow$  FBB,  $M_{N2}$  off  $\leftarrow$  RBB

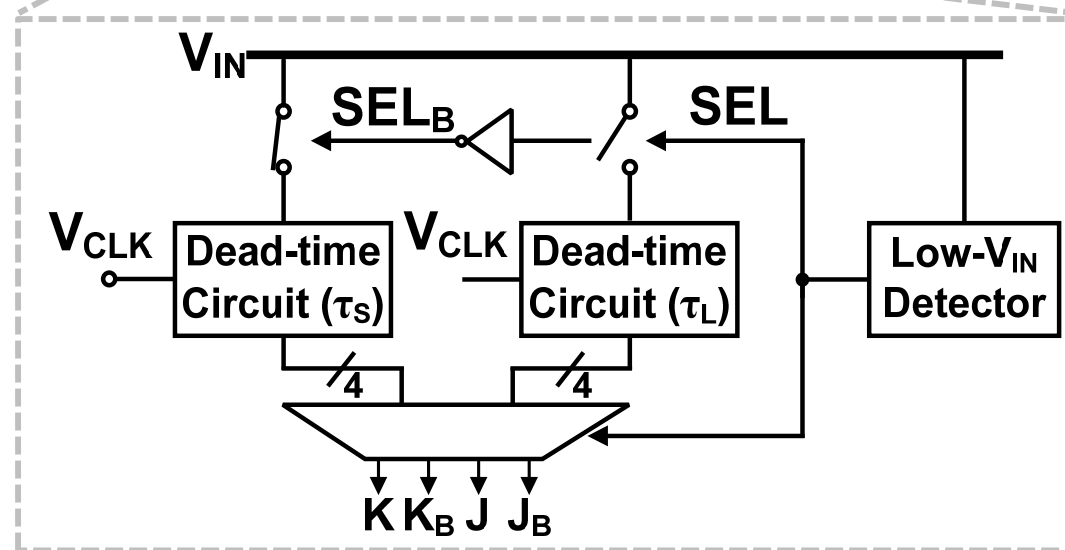
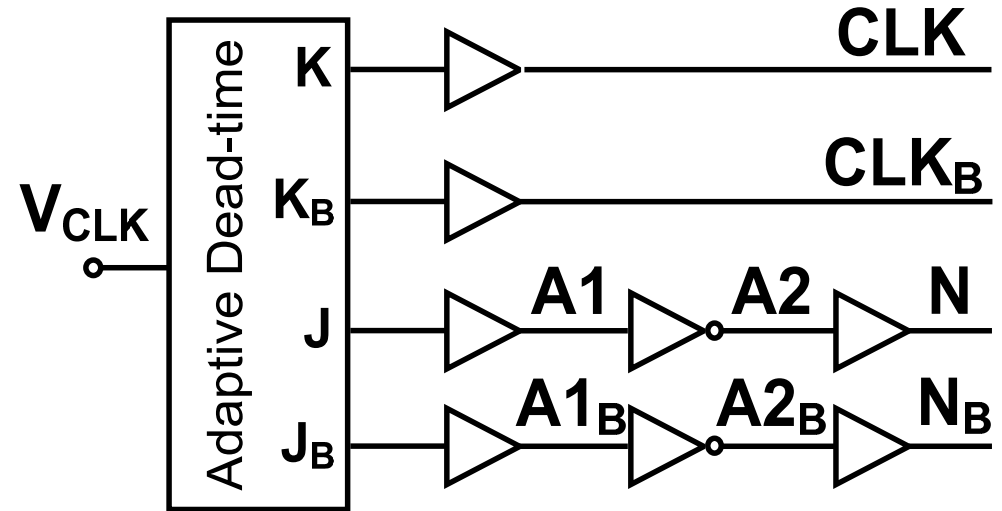
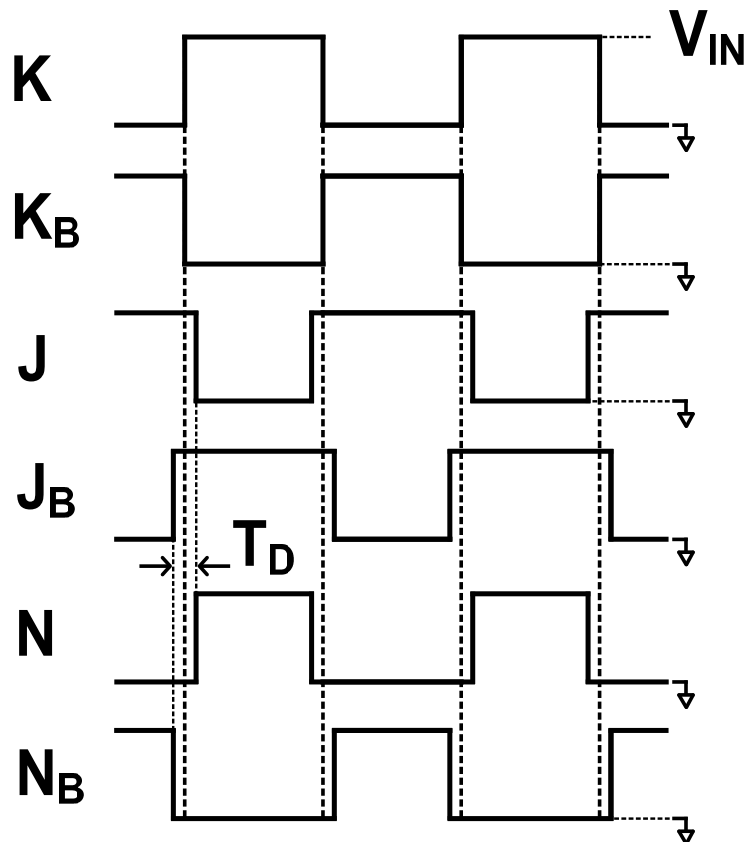


# Fixed Dead-time Circuit

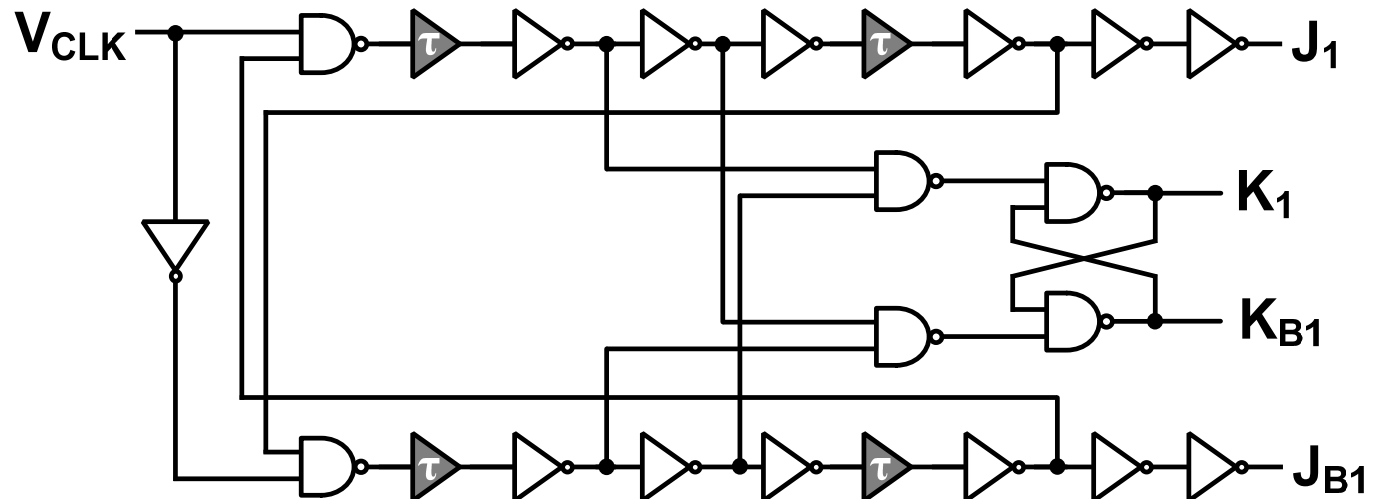
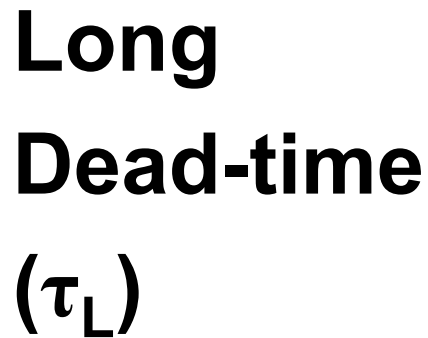
- In EH CP,  $V_{IN}$  is low and not fixed  $\rightarrow T_D$  variation
  - Power throughput, PCE, and reliability issues
- Fixed dead-time circuit is not effective @ low  $V_{IN}$
- How to control  $T_D$  for low-power and low-voltage charge pump?
  1. Supplying more current @ low  $V_{IN}$  for faster transition of delay cells
  2. Multiplexing : long  $T_D$  @ high  $V_{IN}$ , short  $T_D$  @ low  $V_{IN} \rightarrow$  Parallelism
    - Where should MUX be inserted?

# Adaptive Dead-time (AD) Circuit

- Binary selection for dead-times



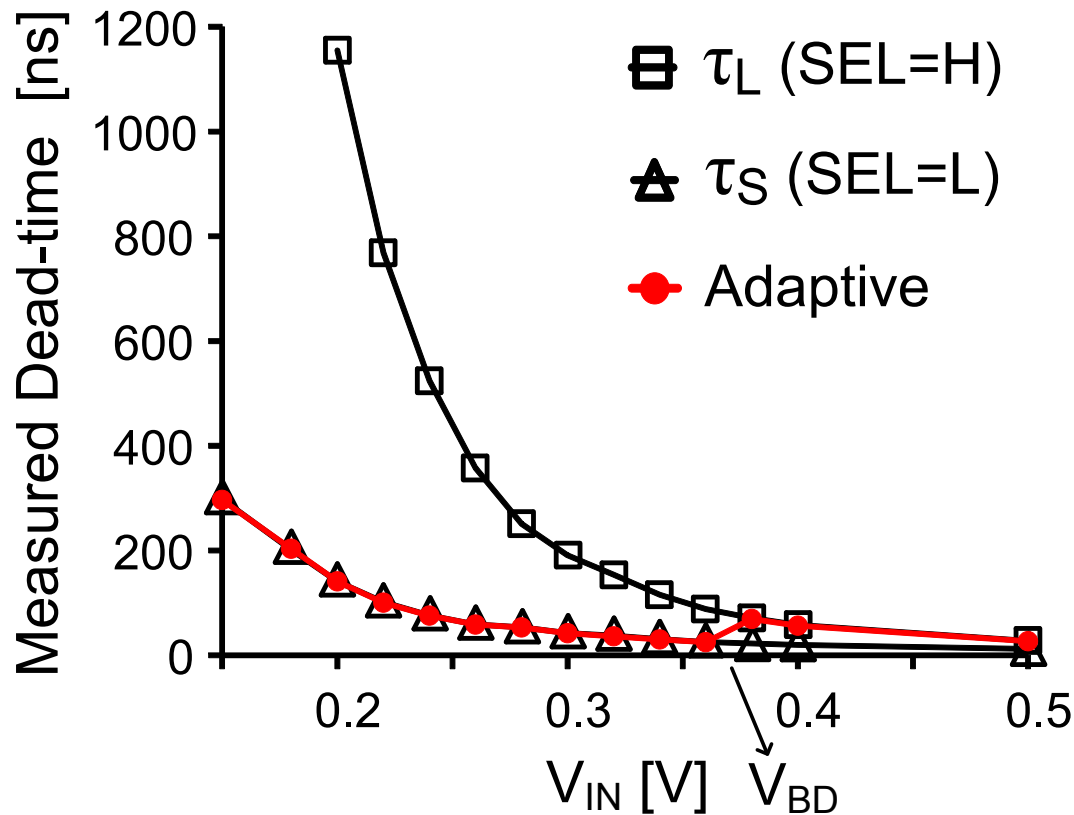
# Short Dead-time ( $\tau_s$ )





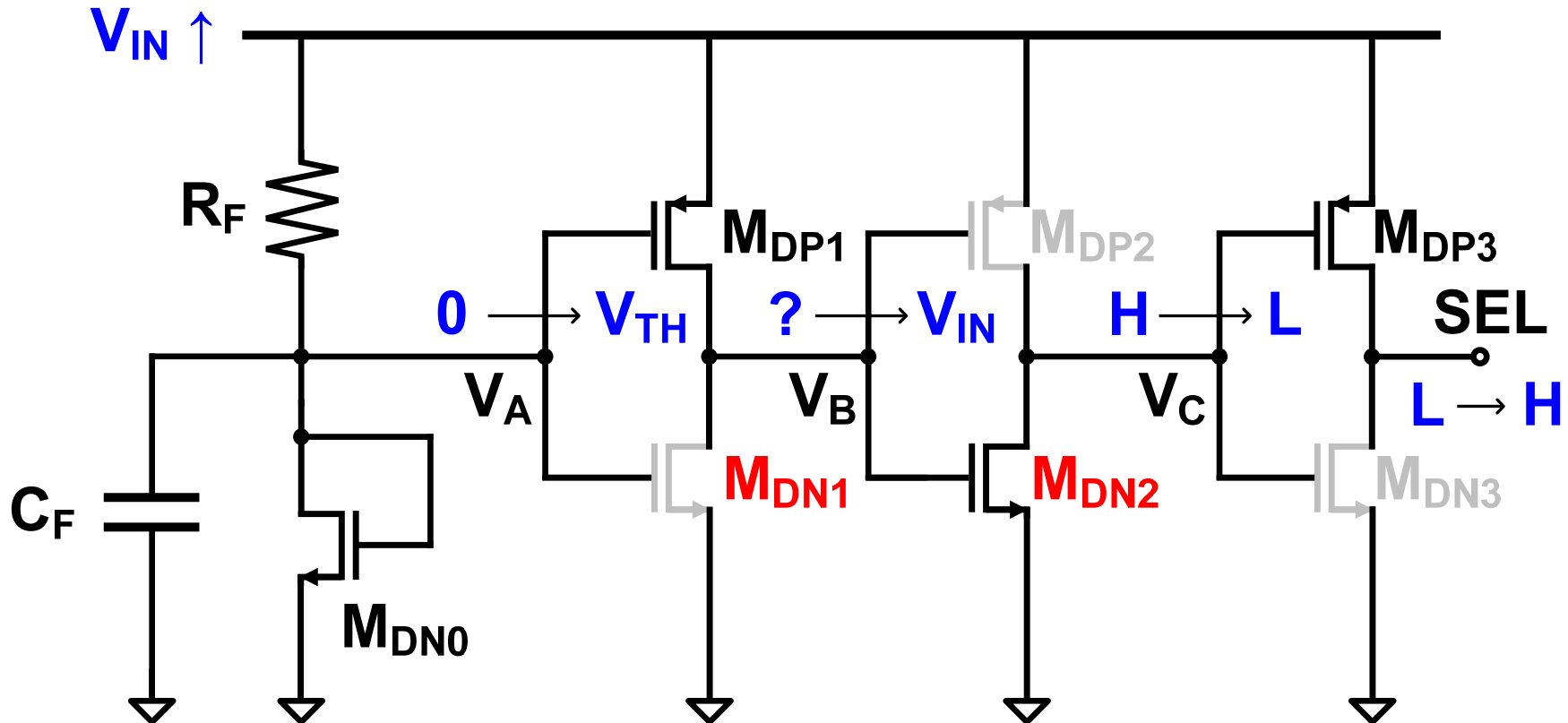
# Dead-time vs. $V_{IN}$

- As  $V_{IN}$  increases,  $\tau_S$  causes reverse current.
- As  $V_{IN}$  decreases,  $\tau_L$  is prohibitively increased.
- $t_{pHL} \propto \alpha / (V_{DD} - V_{TH,N} - V_{DSATn}/2)$



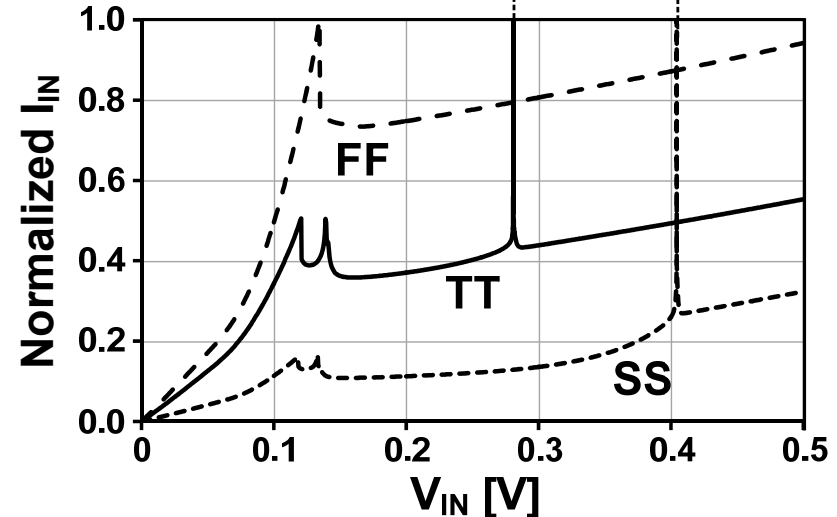
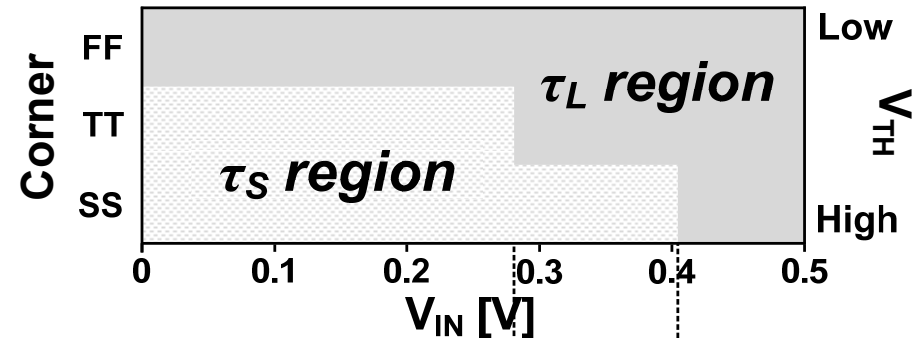
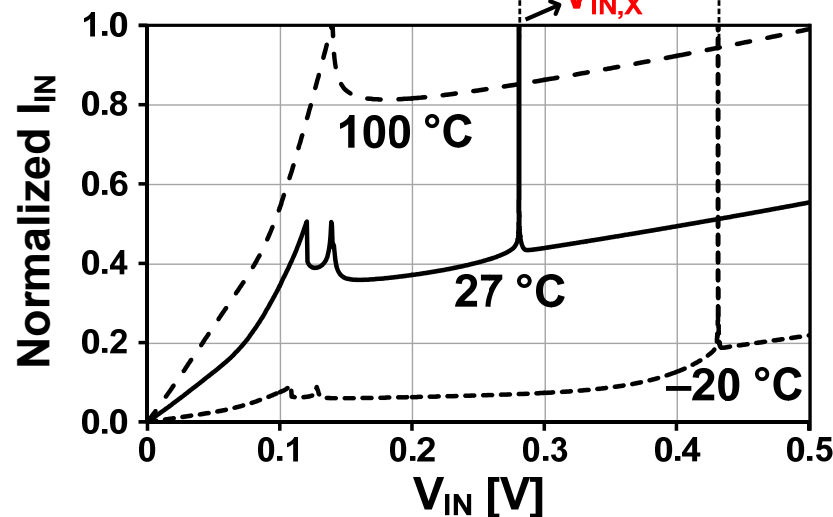
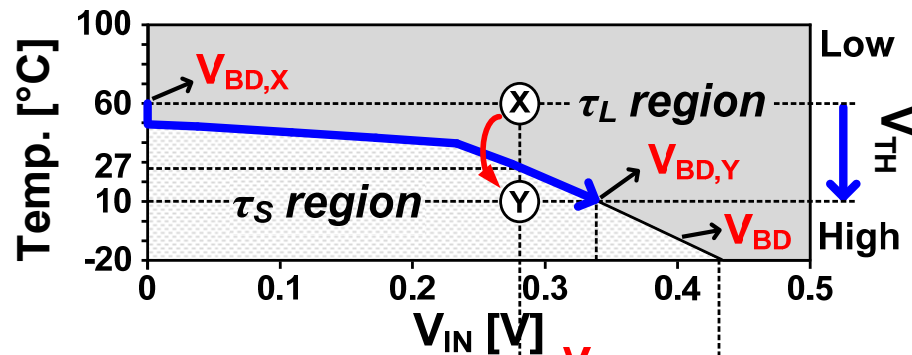
# Low- $V_{IN}$ Detector

- As  $V_{IN}$  increases,  $SEL = L \rightarrow H$
- $V_{IN} < V_{BD} : SEL=L, V_{IN} > V_{BD} : SEL=H$



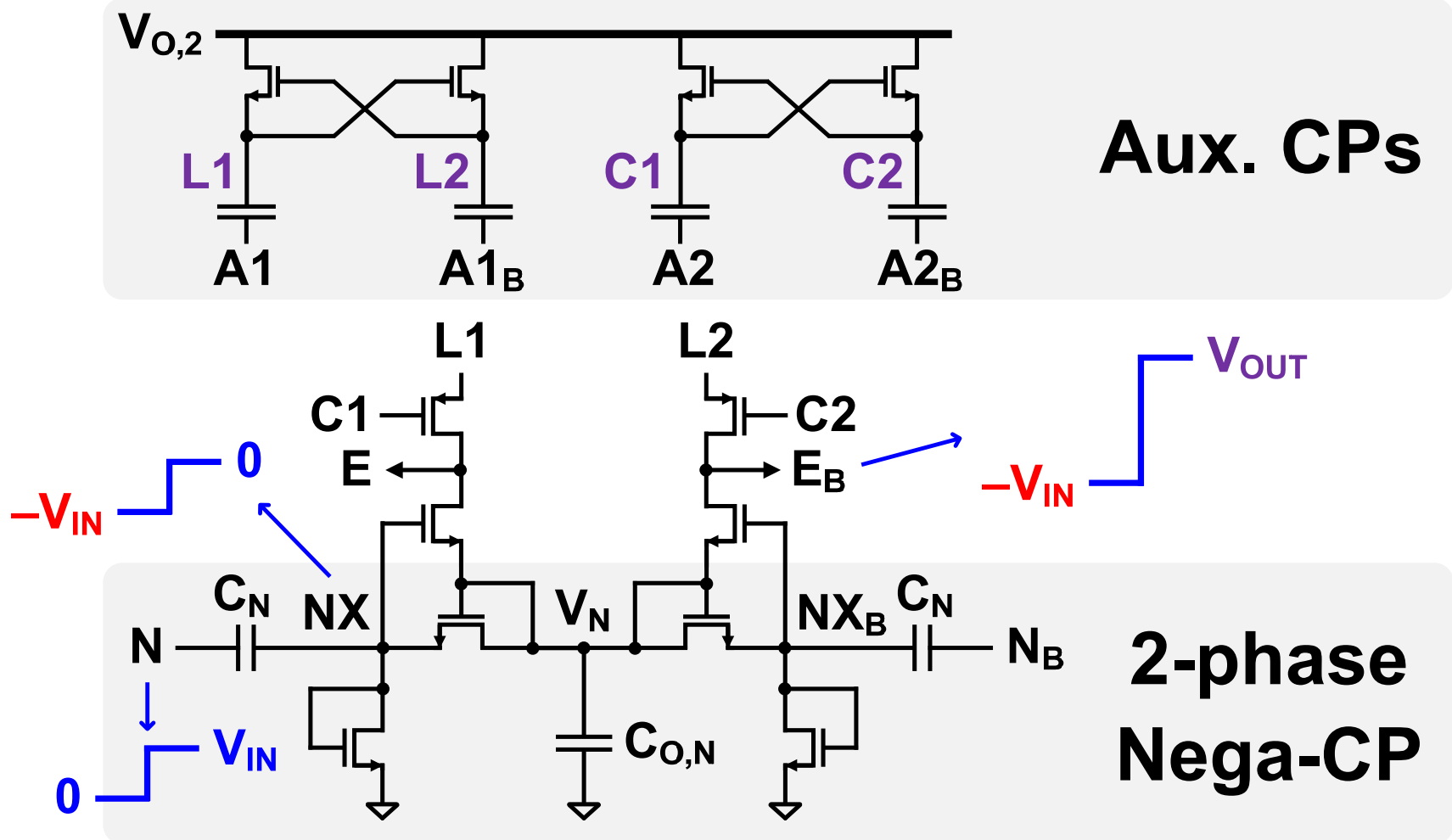
# Temp. & Process Variations

- $V_{IN} = V_{IN,X} : \tau_L @ 60^\circ\text{C} \rightarrow \tau_S @ 10^\circ\text{C}$
- $V_{BD}$  is shifted from  $V_{BD,X} (= 0)$  to  $V_{BD,Y}$



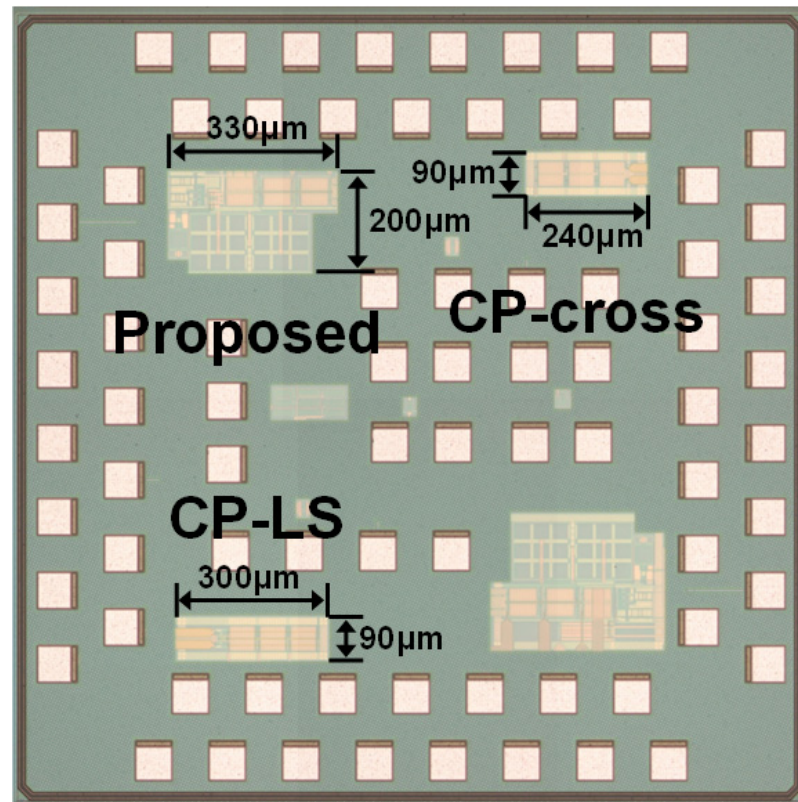
# Switch-Conductance Enhancer

- $E$  and  $E_B$  for SBB and SW-G enhancement



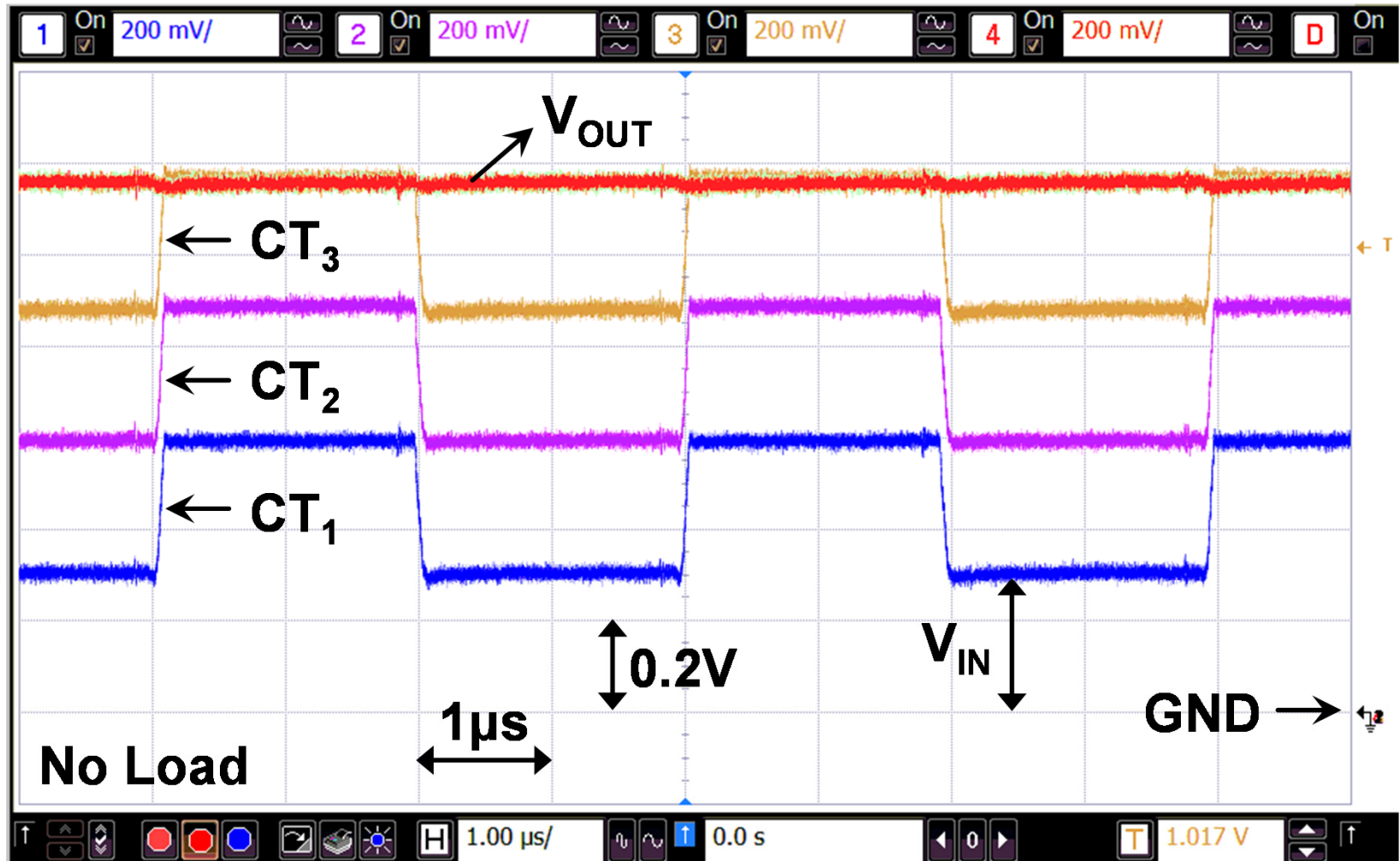
# Chip Microphotograph

- 0.13 $\mu\text{m}$  CMOS technology w/ triple well
- 10nF off-chip pumping capacitors  
→ low-frequency and low-voltage CP



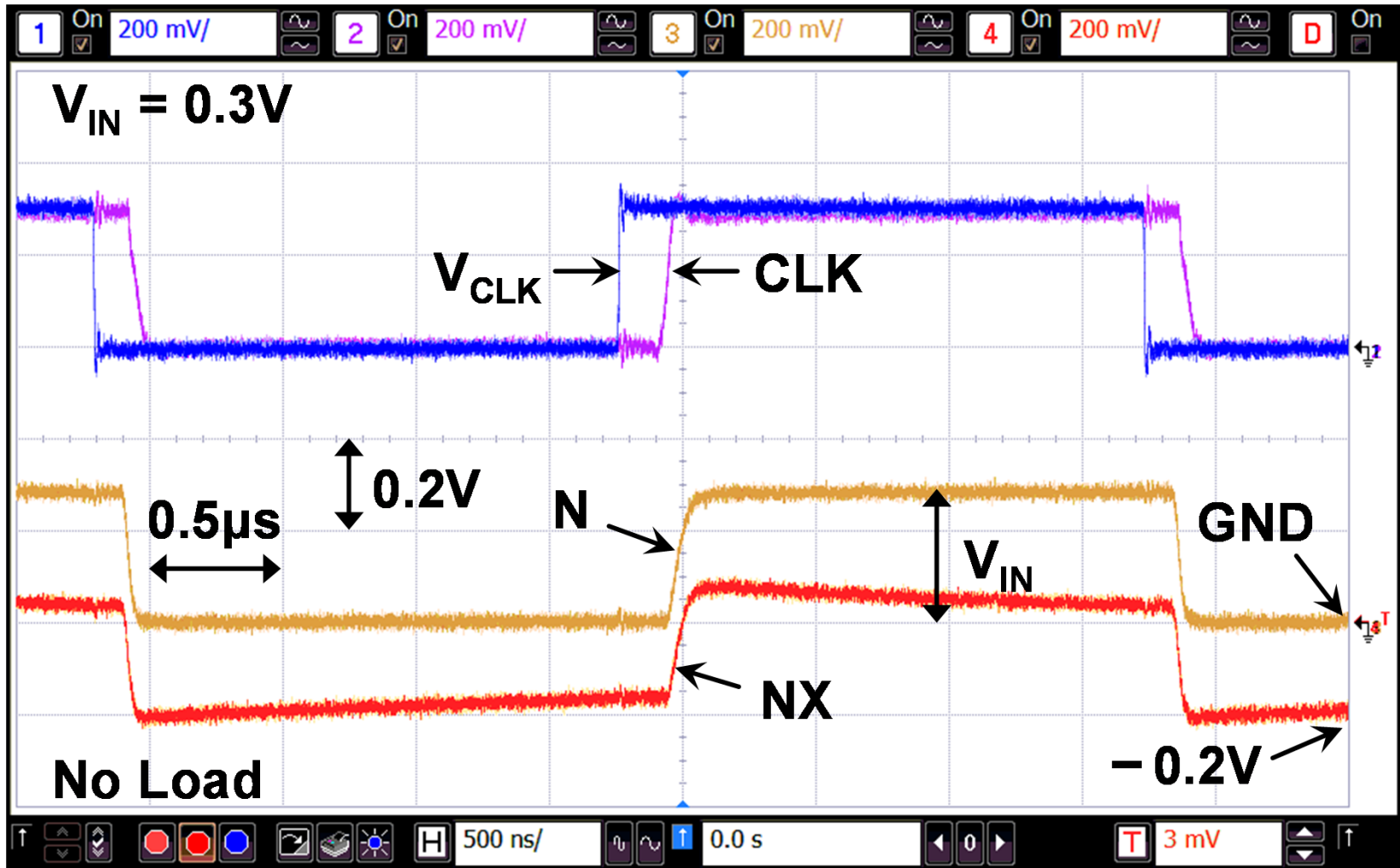
# Measurement Results (Unit-CP)

- Pumped CLKs and  $V_{OUT}$  @  $V_{IN} = 0.3V$



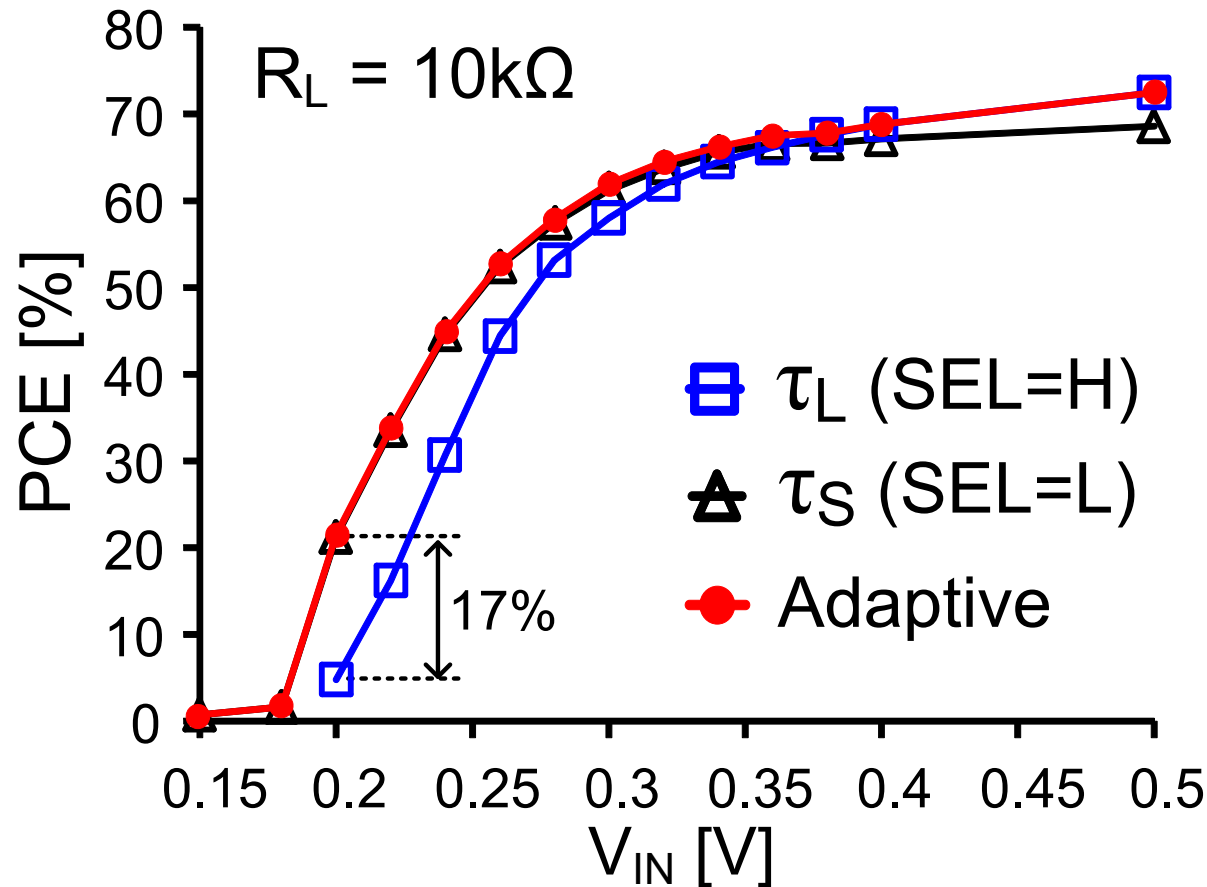
# Measurement Results (Nega-CP)

- $C_N$  should be optimized for better PCE



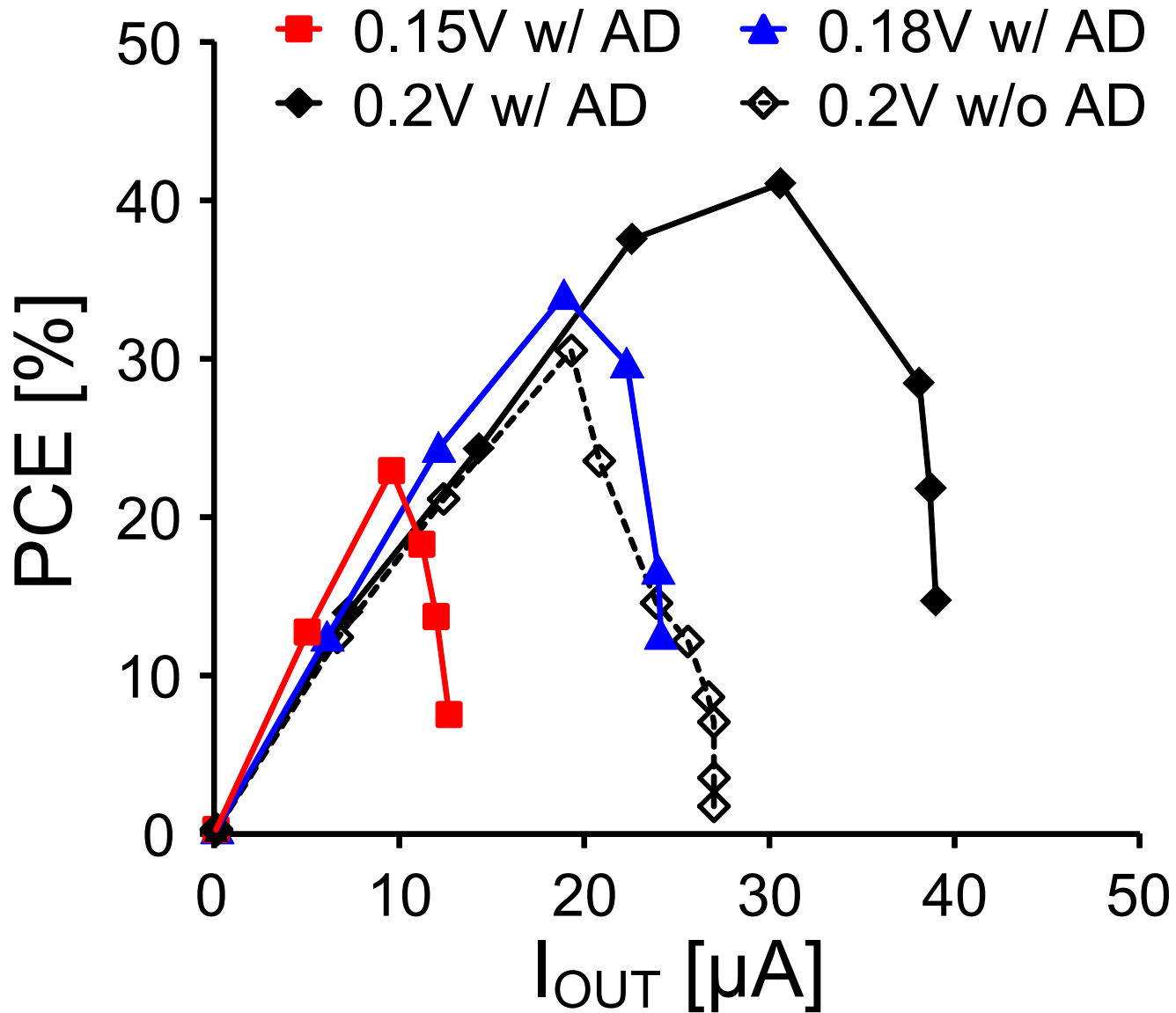
# Dead-time Measurement

- SBB and SW-G techniques are applied
- $V_{BD}$  was *up-shifted* from simulated value

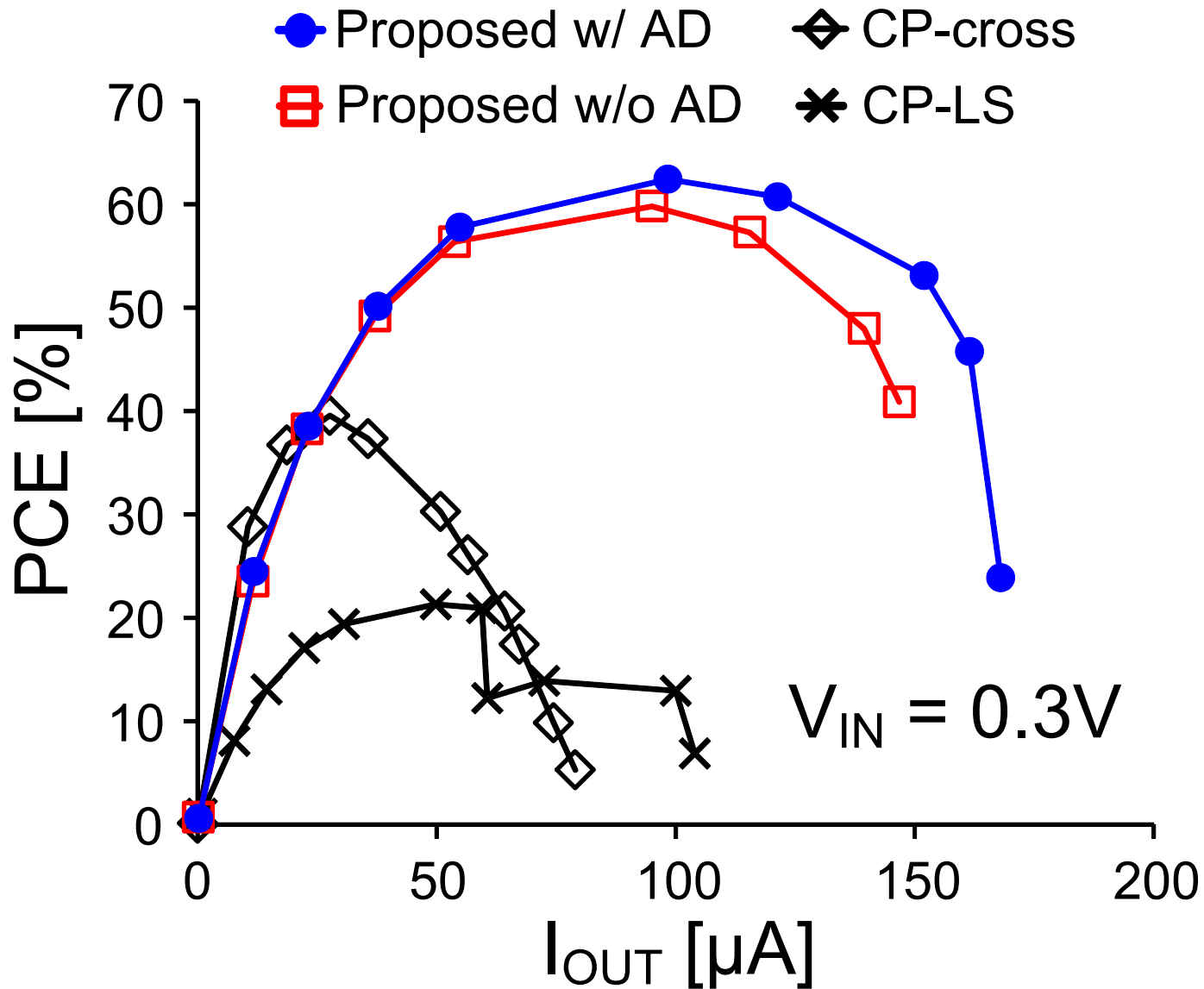




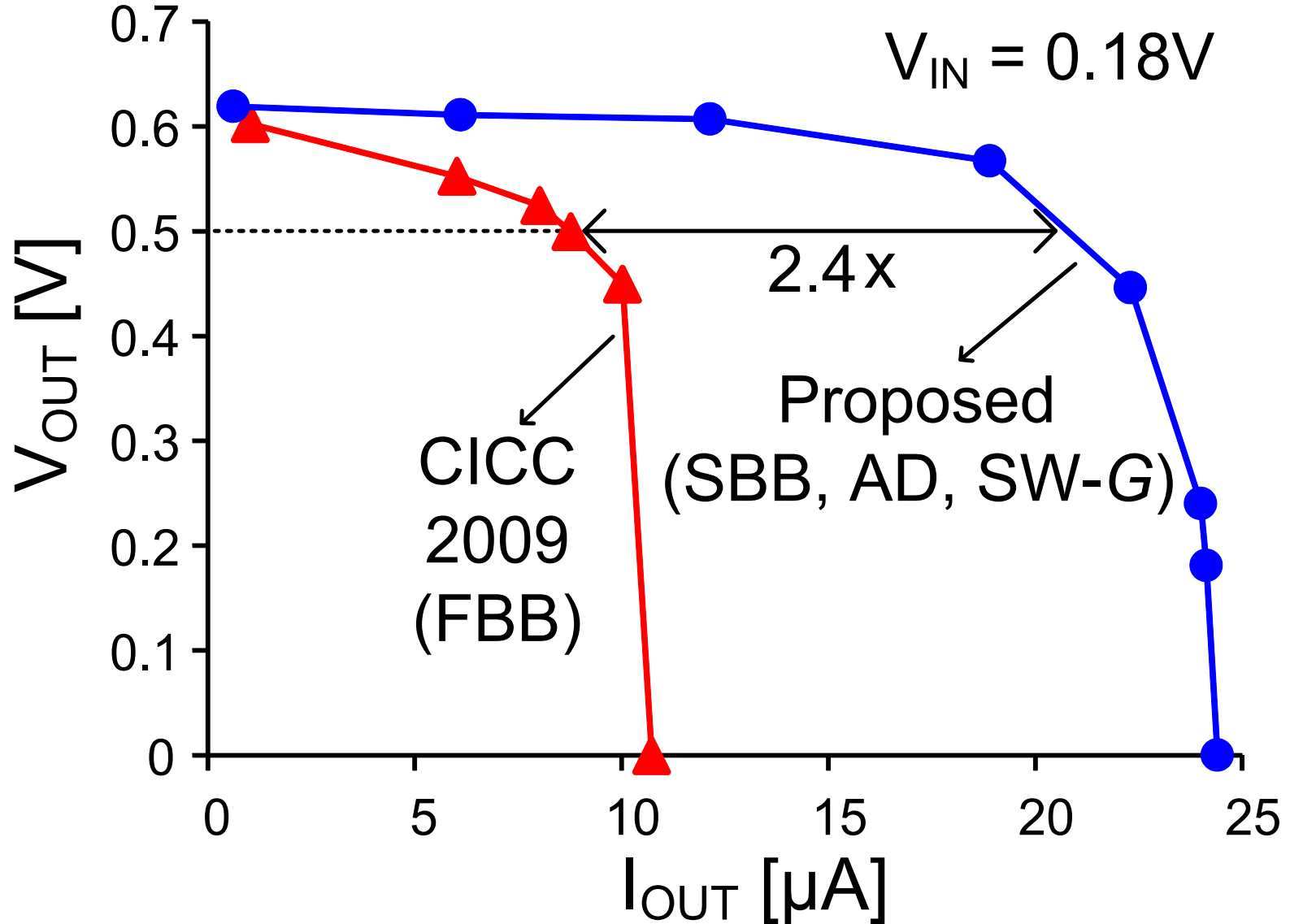
# Efficiency at Low- $V_{IN}$



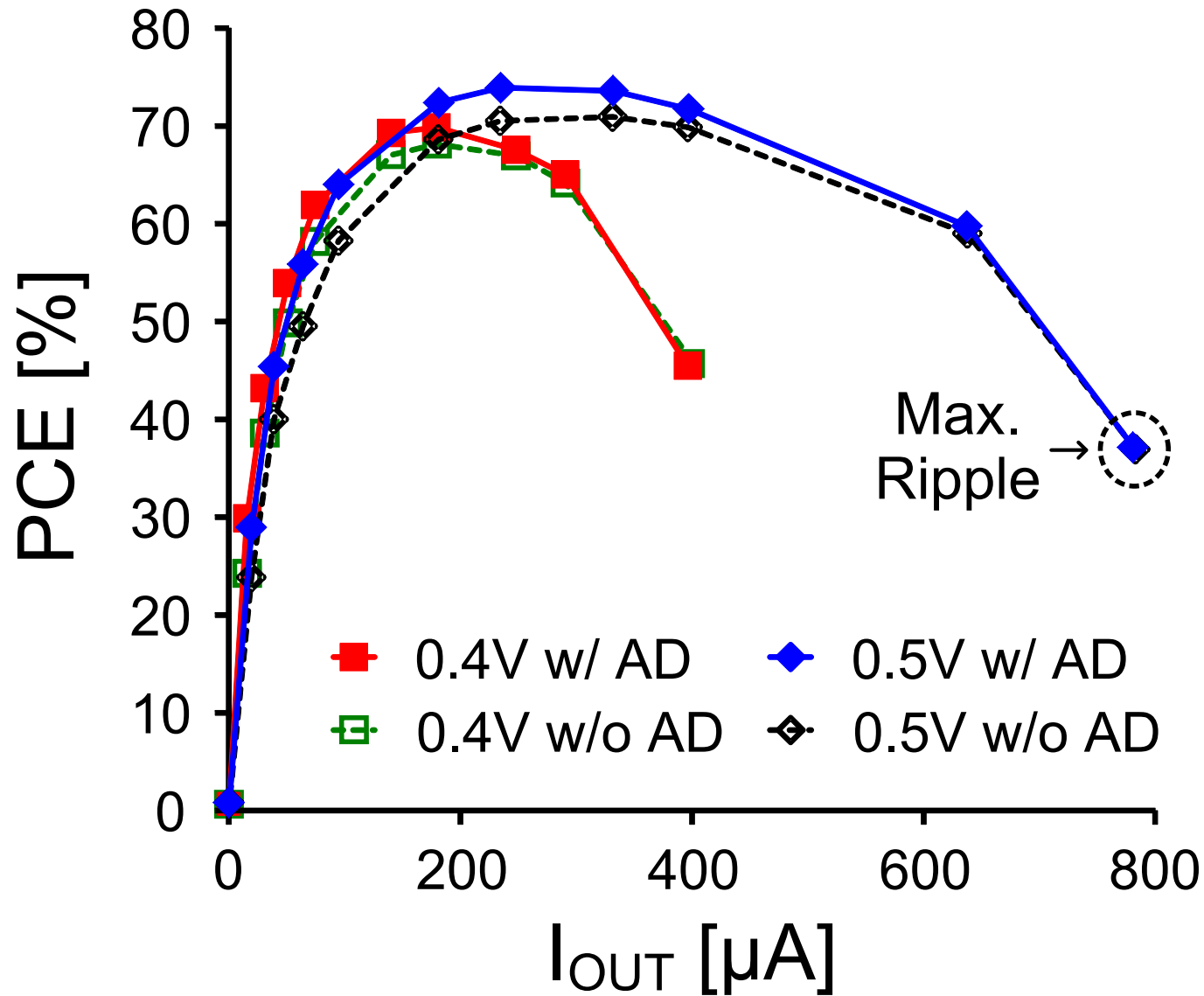
# PCE Comparison of CPs



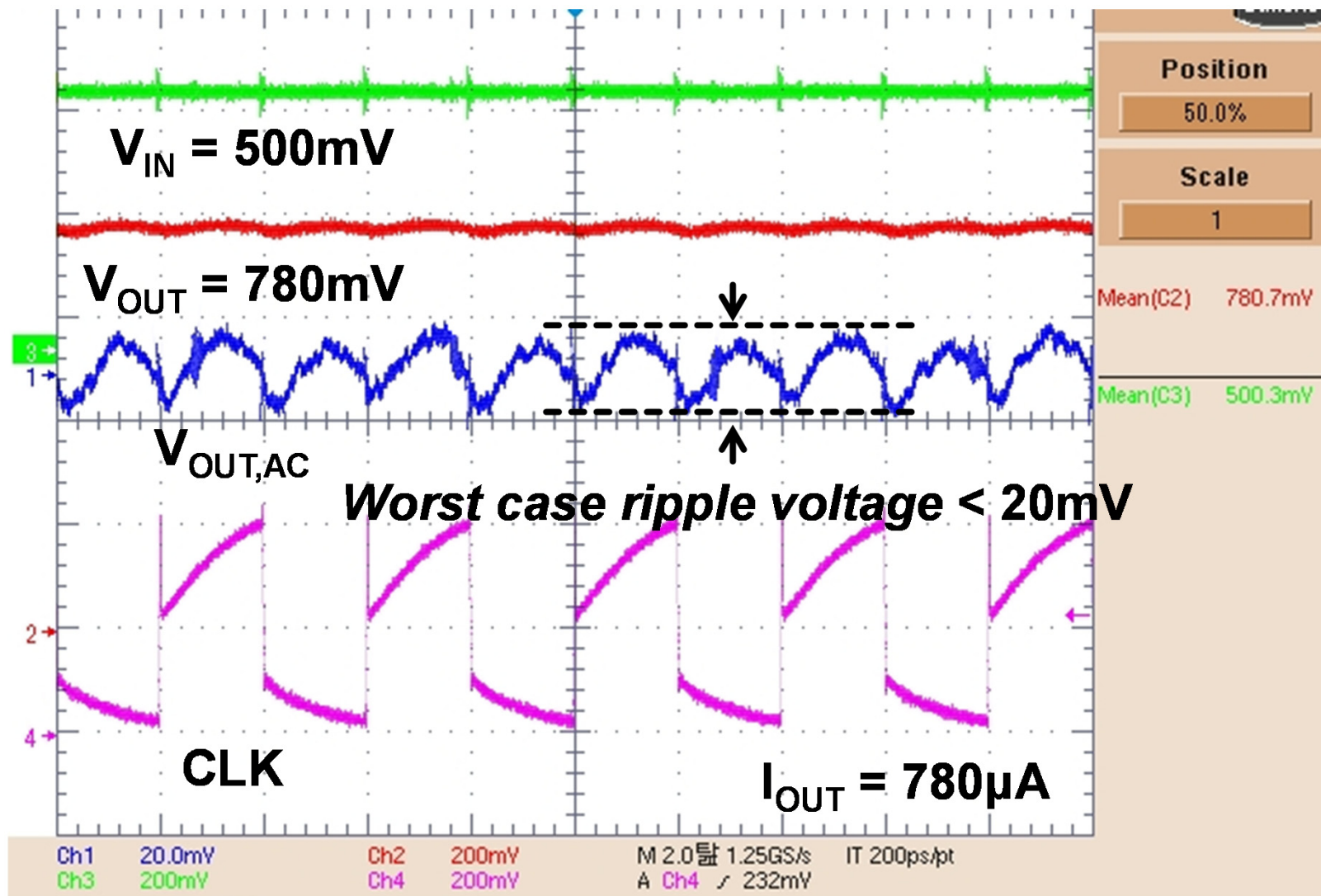
# Power Throughput Improvement



# Efficiency at High- $V_{IN}$



# Maximum Ripple Voltage



# Performance Comparison

	CICC 2010	ASP-DAC 2012	TCAS-II 2011	This work
Process	65nm CMOS	65nm CMOS	0.13 $\mu$ m CMOS	0.13 $\mu$ m CMOS
CP Type	3-stg doubler	10-stg CP	3-stg CP	3-stg doubler
Clock Freq.	10MHz	1MHz, 20MHz	800kHz	250kHz
Min. $V_{IN}$	0.18V	0.12V	0.27V	0.15V
$V_{OUT}$ @ No load	0.6V @ $V_{IN} = 0.18V$	0.77V @ $V_{IN} = 0.12V$	1.3V @ $V_{IN} = 0.35V$	0.619V @ $V_{IN} = 0.18V$
Max. PCE	N/A	38.8% @ $V_{IN} = 0.12V$	56% @ $V_{IN} = 0.45V$	34% @ $V_{IN} = 0.18V$ , 72.5% @ $V_{IN} = 0.45V$
$I_{OUT}$ @ $V_{OUT} = 0.5V$	8.75 $\mu$ A @ $V_{IN} = 0.18V$	7 $\mu$ A @ $V_{IN} = 0.12V$ (by extrapolation)	5 $\mu$ A @ $V_{IN} = 0.45V$	21 $\mu$ A @ $V_{IN} = 0.18V$

# Conclusions

- **SBB improves PCE at low  $V_{IN}$**
- **AD circuit and SW-G enhancer push  $V_{IN}$  of CP to lower value**
- **PCE is improved by 17% at  $V_{IN}=0.2V$  by turning on AD circuit**
- **Also, the proposed CP works at  $V_{IN,MIN} = 0.15V$**

# A 1.1nW Energy Harvesting System with 544pW Quiescent Power for Next-Generation Implants

Saurav Bandyopadhyay<sup>1,\*</sup>, Patrick P. Mercier<sup>1,2</sup>,  
Andrew C. Lysaght<sup>3</sup>, Konstantina M. Stankovic<sup>3,4</sup> and  
Anantha P. Chandrakasan<sup>1</sup>

<sup>1</sup>Massachusetts Institute of Technology, Cambridge MA,

<sup>2</sup>University of California, San Diego, La Jolla, CA,

<sup>3</sup>Massachusetts Eye and Ear Infirmary, Boston, MA,

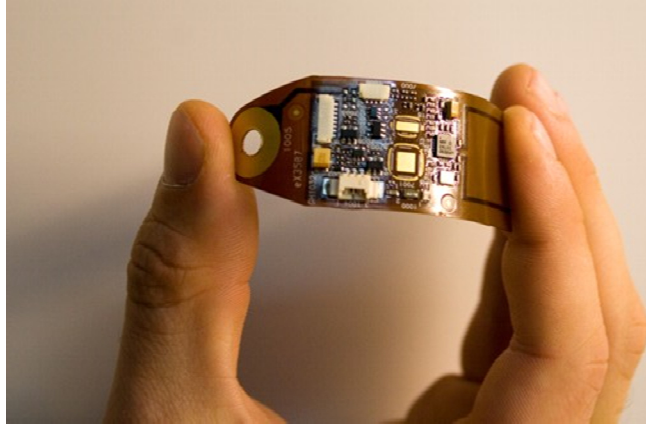
<sup>4</sup>Massachusetts General Hospital, Harvard University, Boston, MA

\*now with Texas Instruments, Dallas, TX

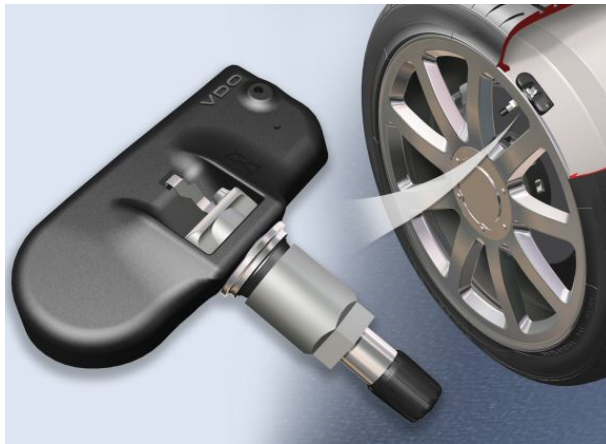


# Motivation for Energy Harvesting

## Electronic Sensors

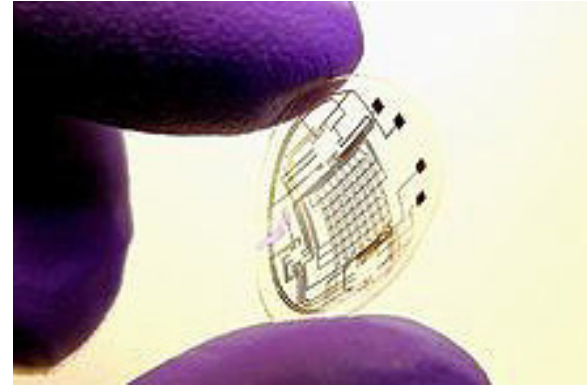


Wearable ECG Patch (IMEC, 2008)

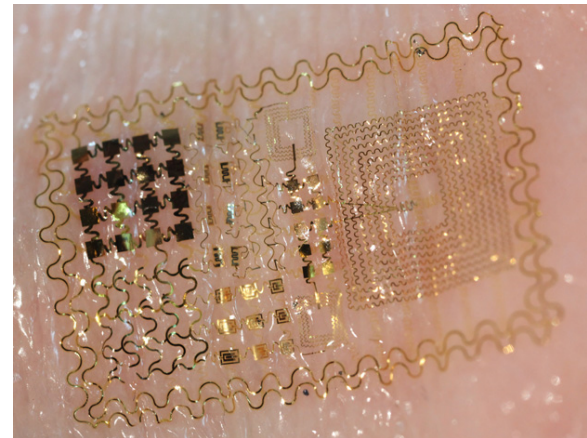


Automotive Applications

## Emerging Biomedical Circuits and Systems

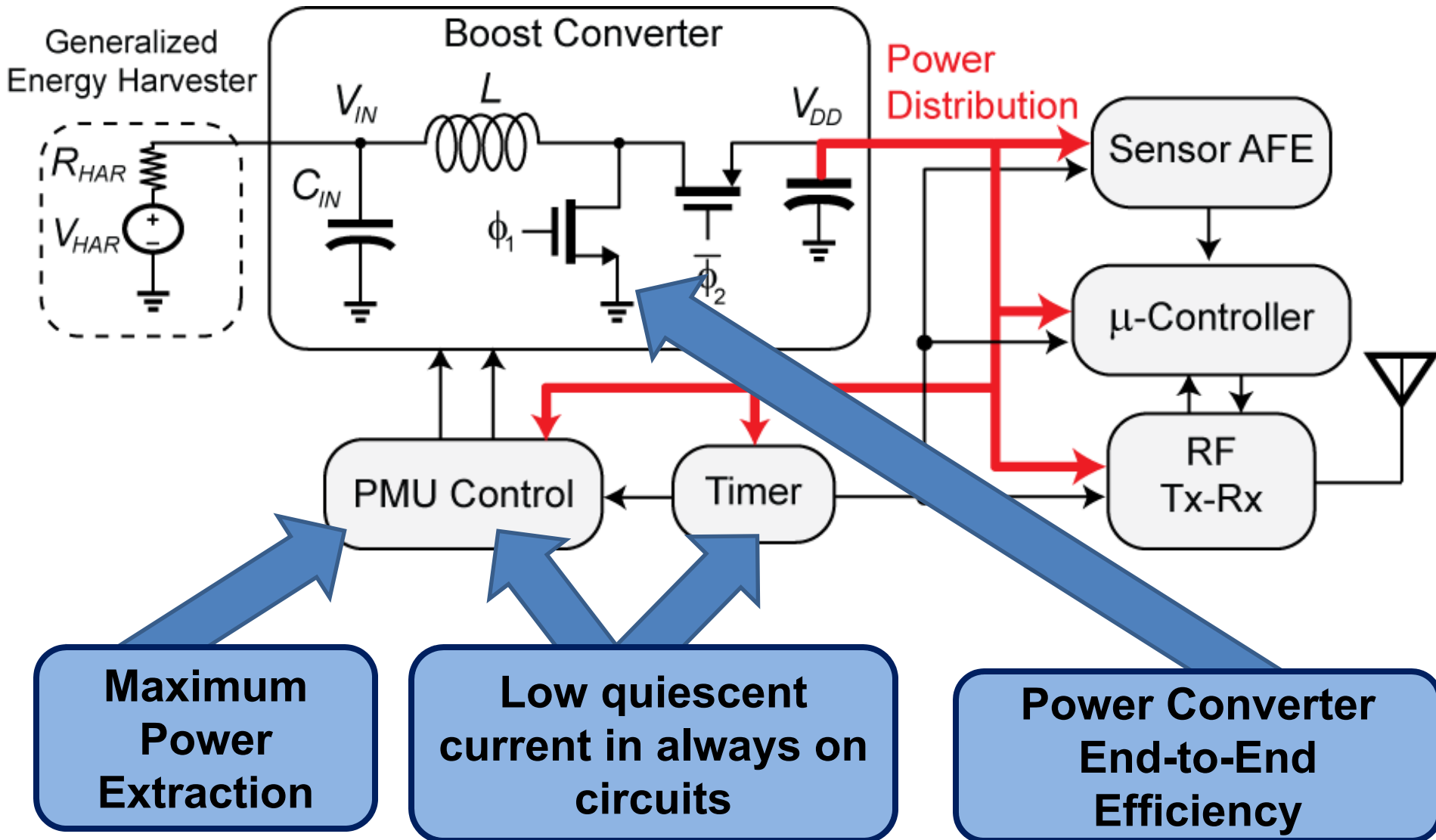


Bionic Lens (Univ. Washington, 2008)

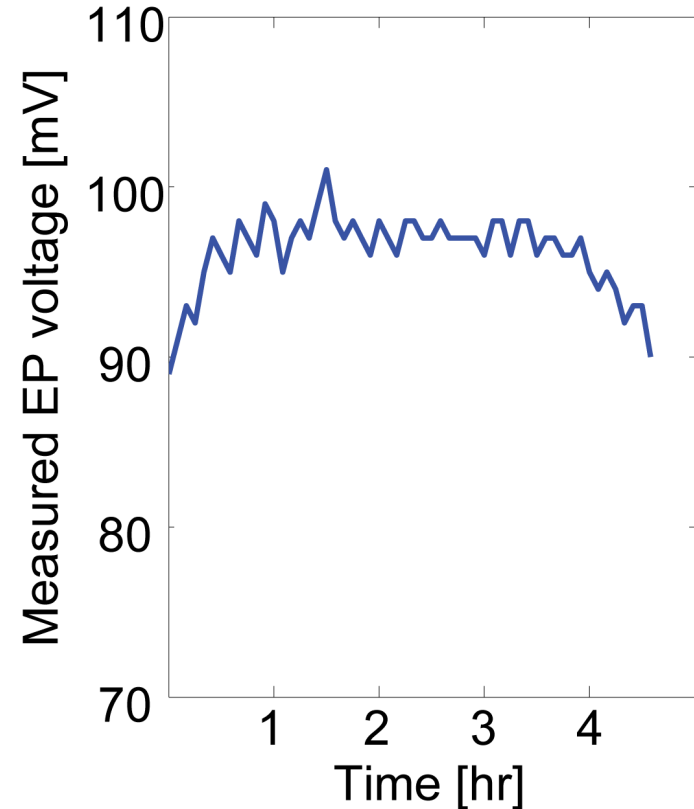
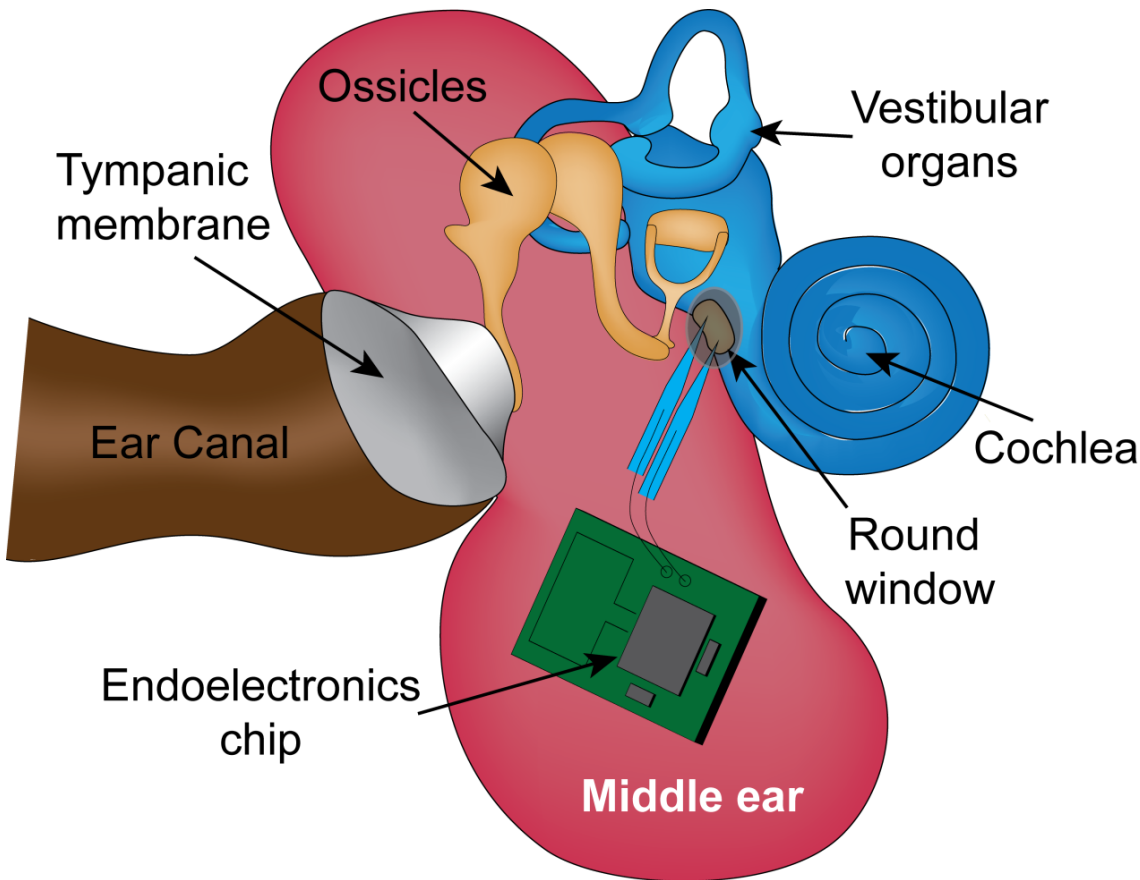


Flexible circuits (Univ. Illinois, 2012)

# PMU Challenges in Energy Harvesting



# Recent Advancement in Harvesting Bio-Potentials



*Reference:- P.P. Mercier, A.C. Lysaght, S. Bandyopadhyay, K.M. Stankovic and A.P. Chandrakasan, "Energy Extraction from the biologic battery in the inner ear", Nature Biotechnology, Dec 2012*

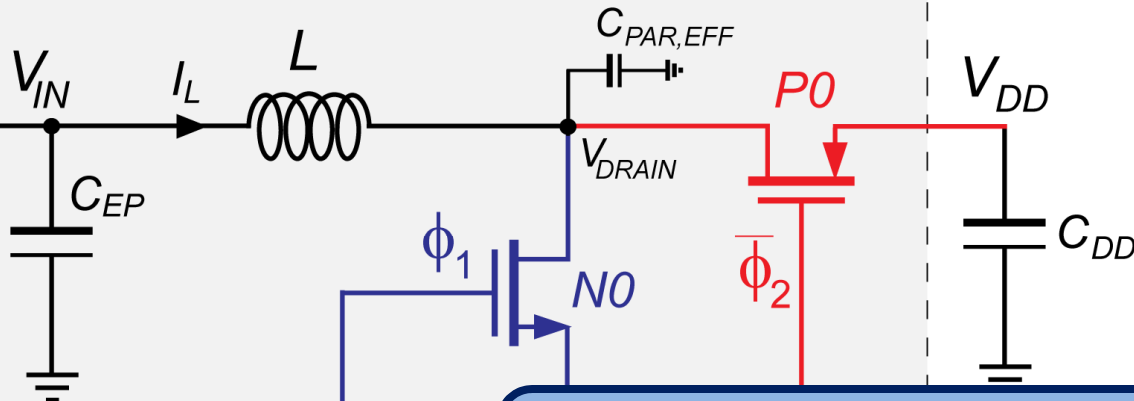
# nW Power Management Unit

Energy Source Model

$R_{HAR}$   
400k $\Omega$ -1M $\Omega$

$V_{HAR}$   
70-100mV

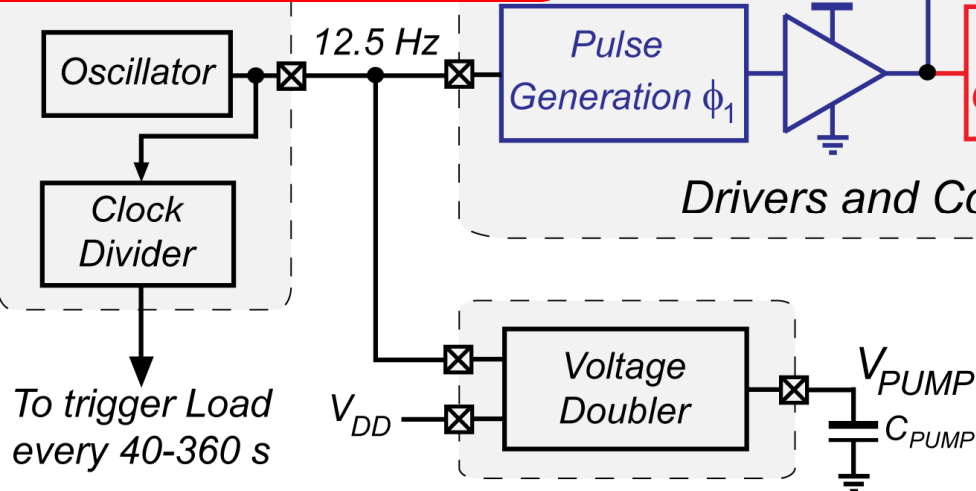
Boost Converter



**Maximum Extractable Power is 1.1-6.25nW With  $V_{IN}$  30-55mV**

**Efficient Boost Converter for 30-55mV to 1V conversion at nW levels**

Drivers and Control Circuits



To trigger Load every 40-360 s

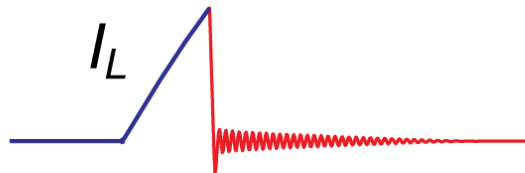
**10-100's of pW Quiescent Power of Controller for sustainability**

# Outline

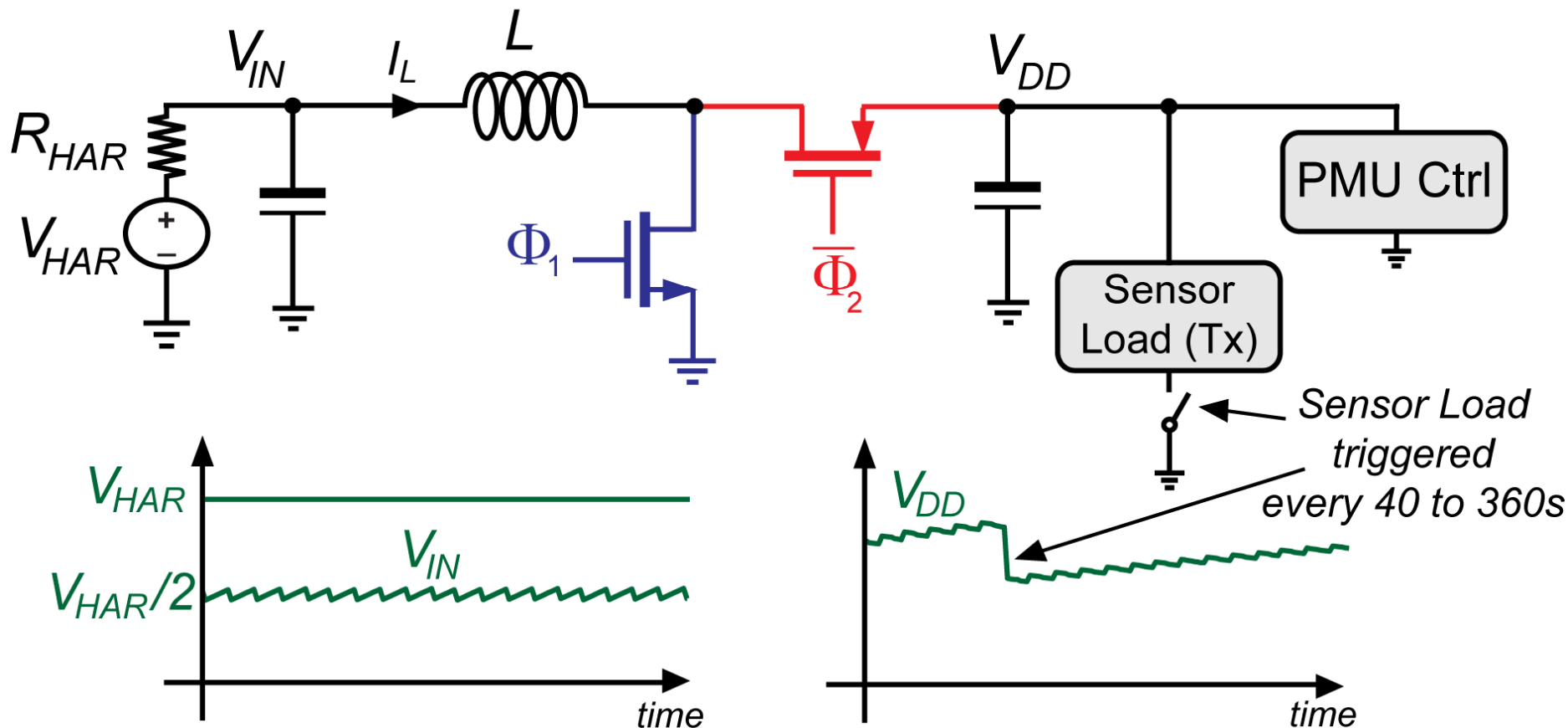
---

- Details of the nW Power Management Unit
  - Boost Converter- Design Considerations and Losses
  - Charge Pump for Leakage Reduction
  - pW Control Circuits
  
- Measured Results
  - Boost Converter Efficiency
  - Quiescent Power of Controller
  - Transient Measurements
  
- Comparison with state-of-art and Conclusions

# nW Boost Converter Operation

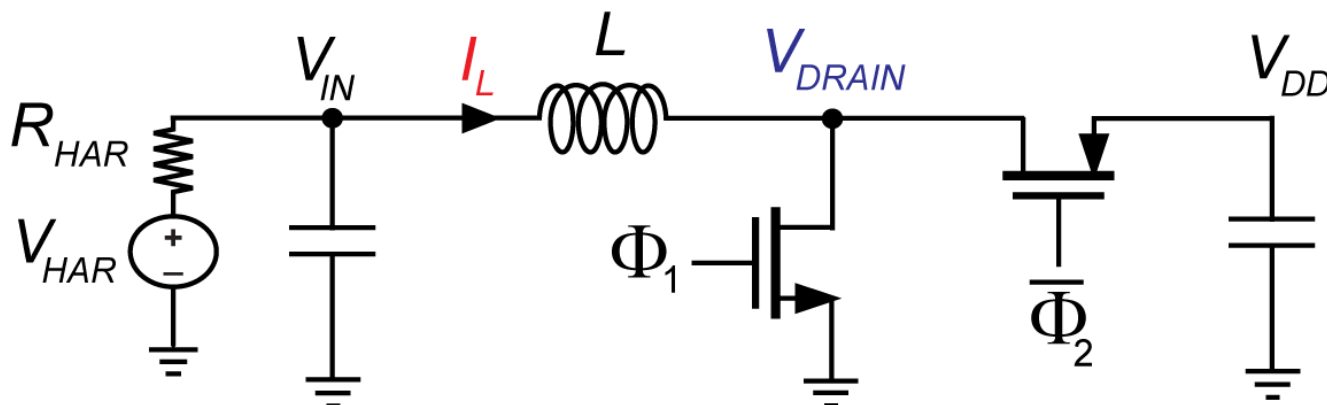
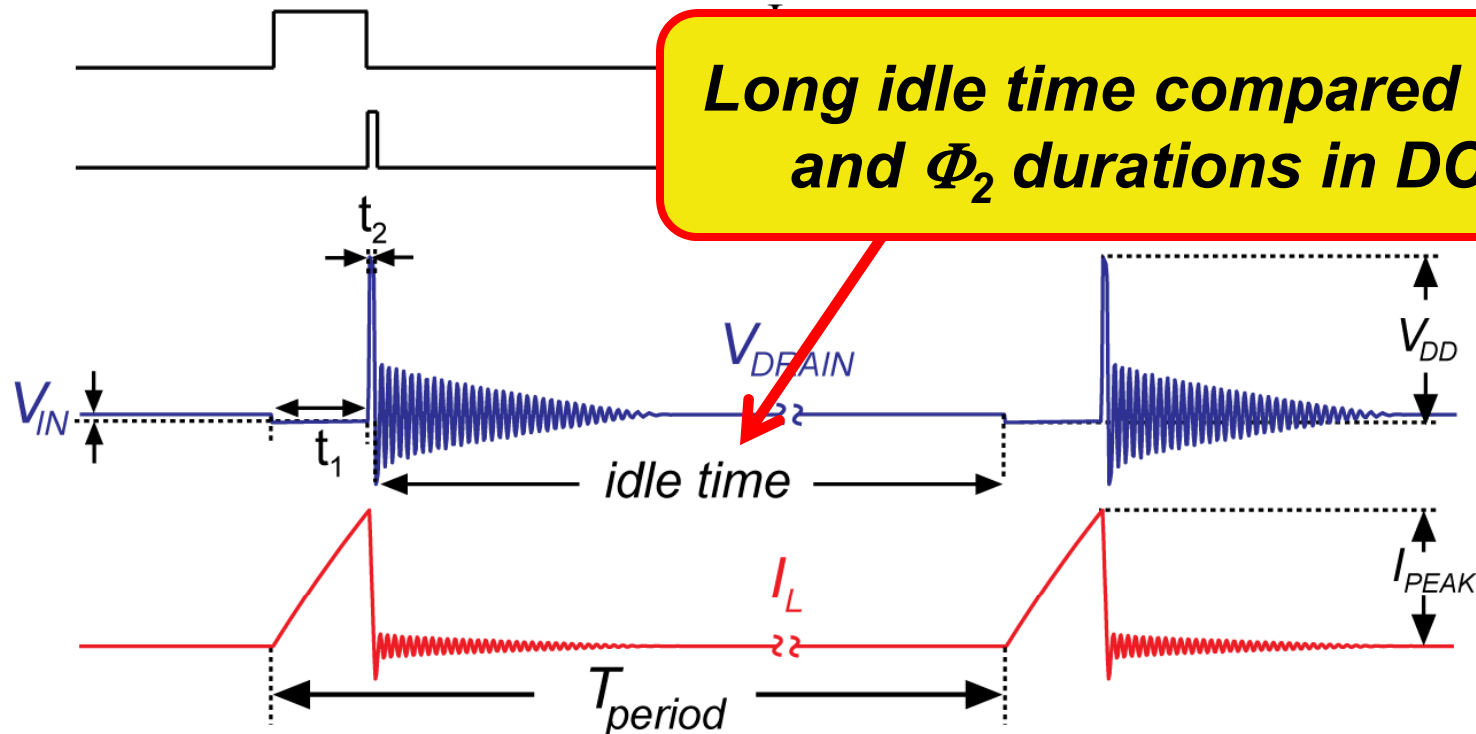


$$Z_{IN} = \frac{V_{IN}}{\bar{I}_L} \approx \frac{2L}{t_1^2 f_s} \approx R_{HAR}$$

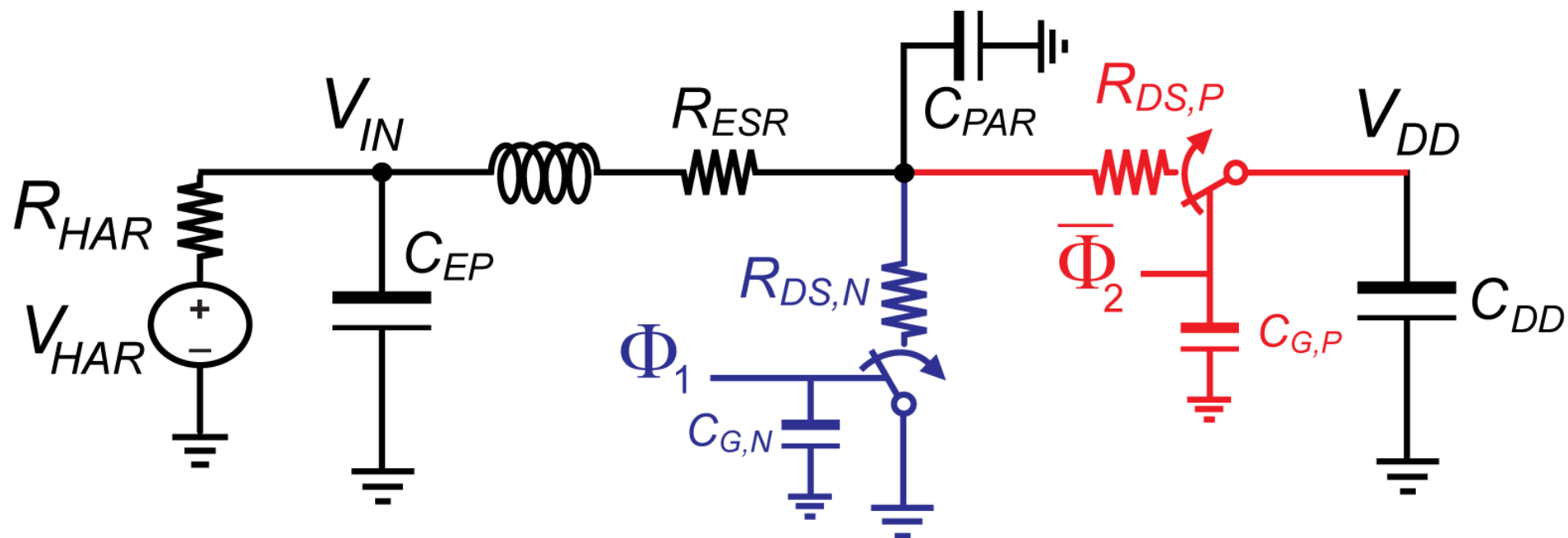


**Single Power Conversion Stage for increased efficiency**

# nW Boost Converter Operation



# Boost Converter Traditional Losses



$$\text{Conduction Loss} = I_{N,RMS}^2 R_{DS,N} + I_{P,RMS}^2 R_{DS,P} + I_{IN,RMS}^2 R_{ESR}$$

$$\text{Switching Loss} = C_{G,N} V_{GATE}^2 f_s + C_{G,P} V_{GATE}^2 f_s + 0.5 C_{PAR} V_{DD}^2 f_s$$



*From Power FETs*



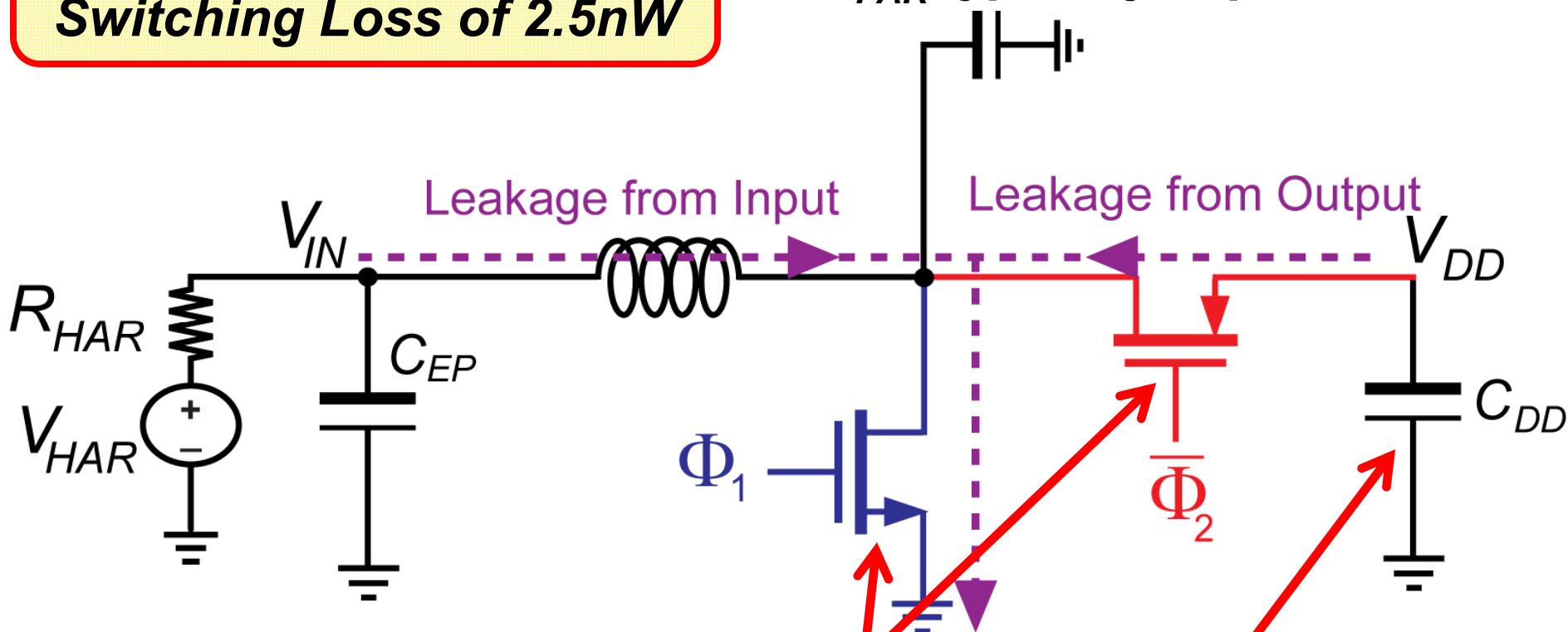
*From Parasitics*



# Additional Considerations for nW Operation

$f_s$  of 1KHz,  $V_{DD}$  of 1V  
Switching Loss of 2.5nW

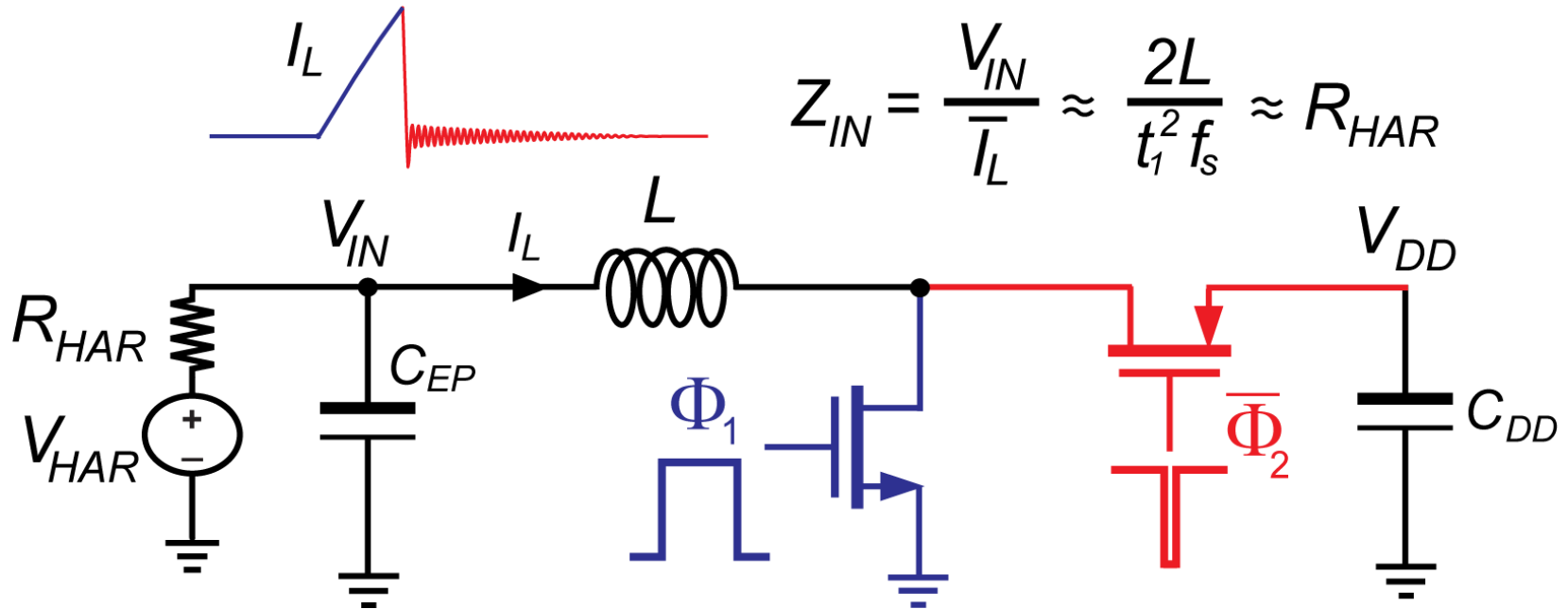
$C_{PAR}$  typically  $\sim 5pF$



Loss due to Power FET  
leakage of 243pW in typical  
and  $>1nW$  in the fast corner

Low Leakage Output  
Capacitor

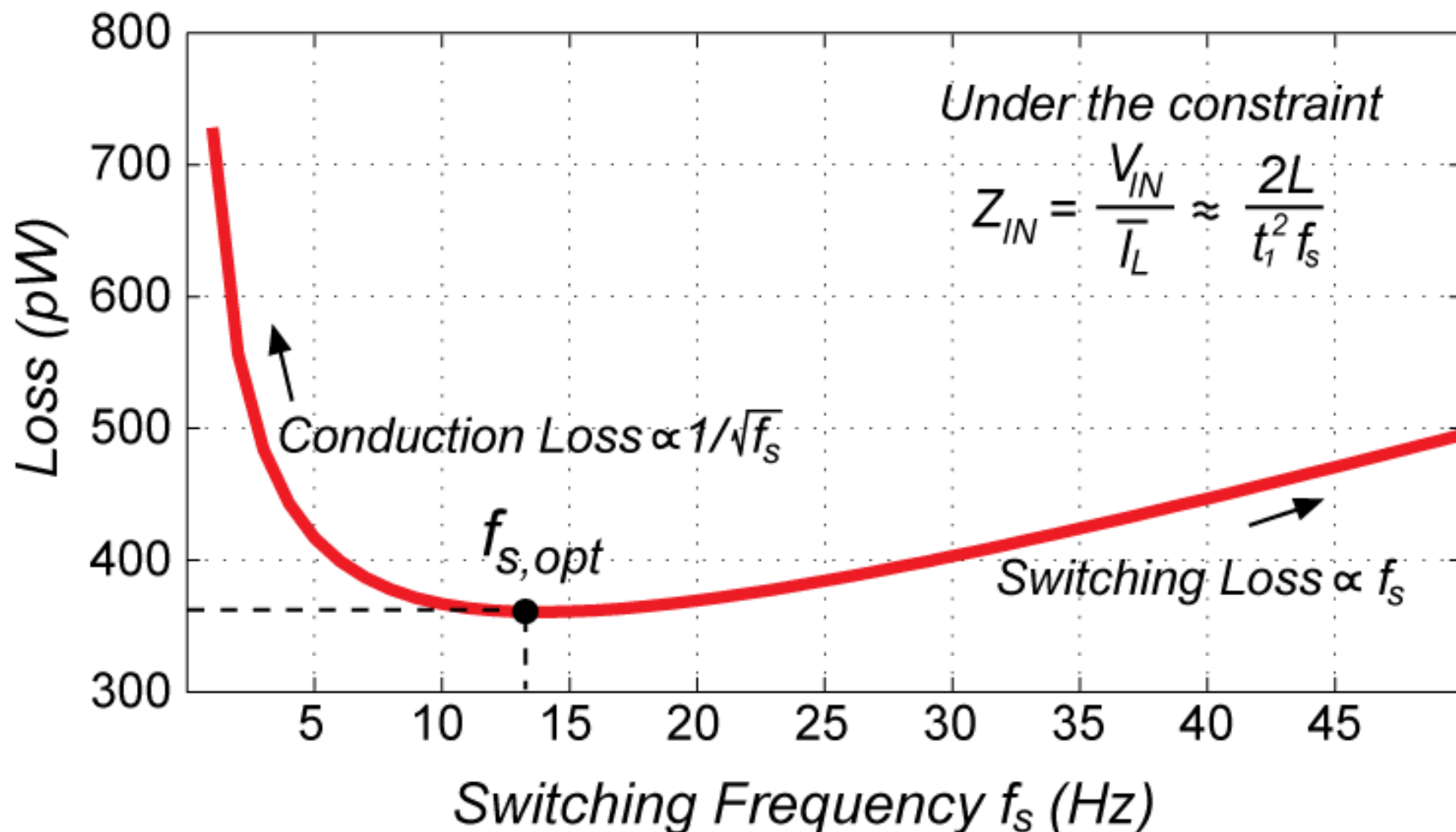
# Boost Converter Efficiency Optimization



**Overall Loss = Switching Losses ( $\propto CV^2 f_s$ ) +  
 Conduction Losses ( $I_{rms}^2 R$ ) + Leakage Losses**

**Optimization w.r.t  $f_s$ ,  $W_N$  and  $W_P$  under  $Z_{IN}$  constraint  
 with leakage considerations**

# Boost Converter Frequency Optimization

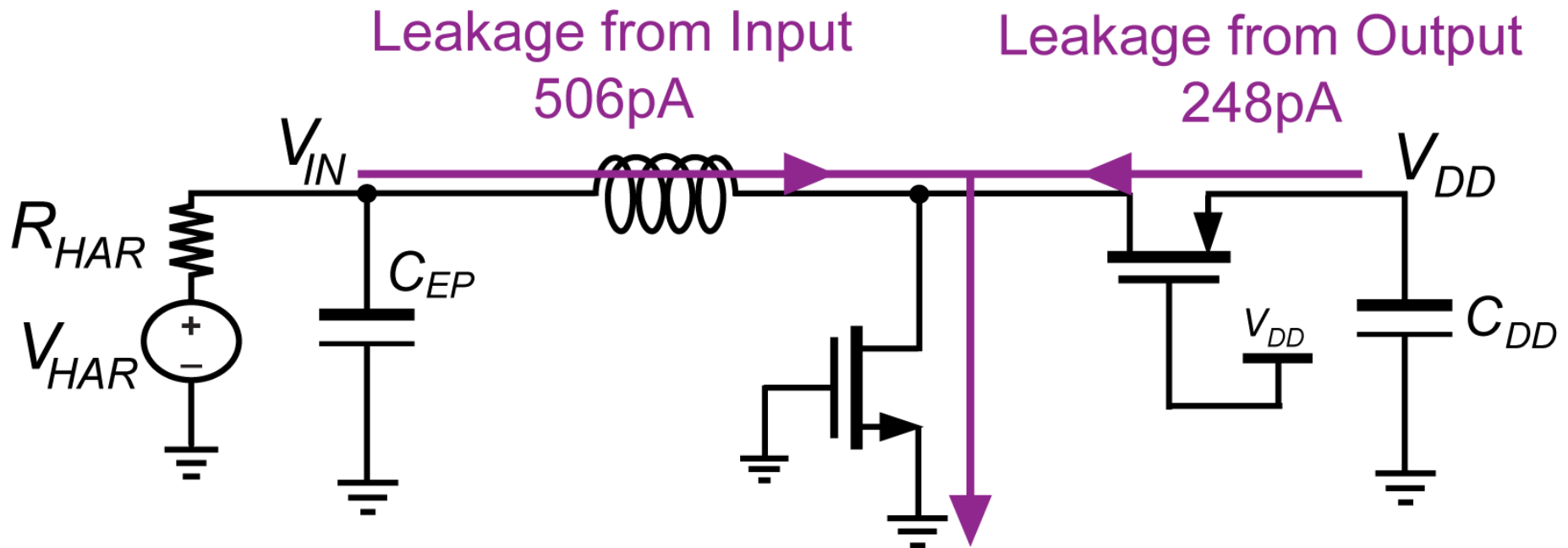


**Optimum Switching Frequency under  $Z_{IN}$  constraint**

# Leakage Paths

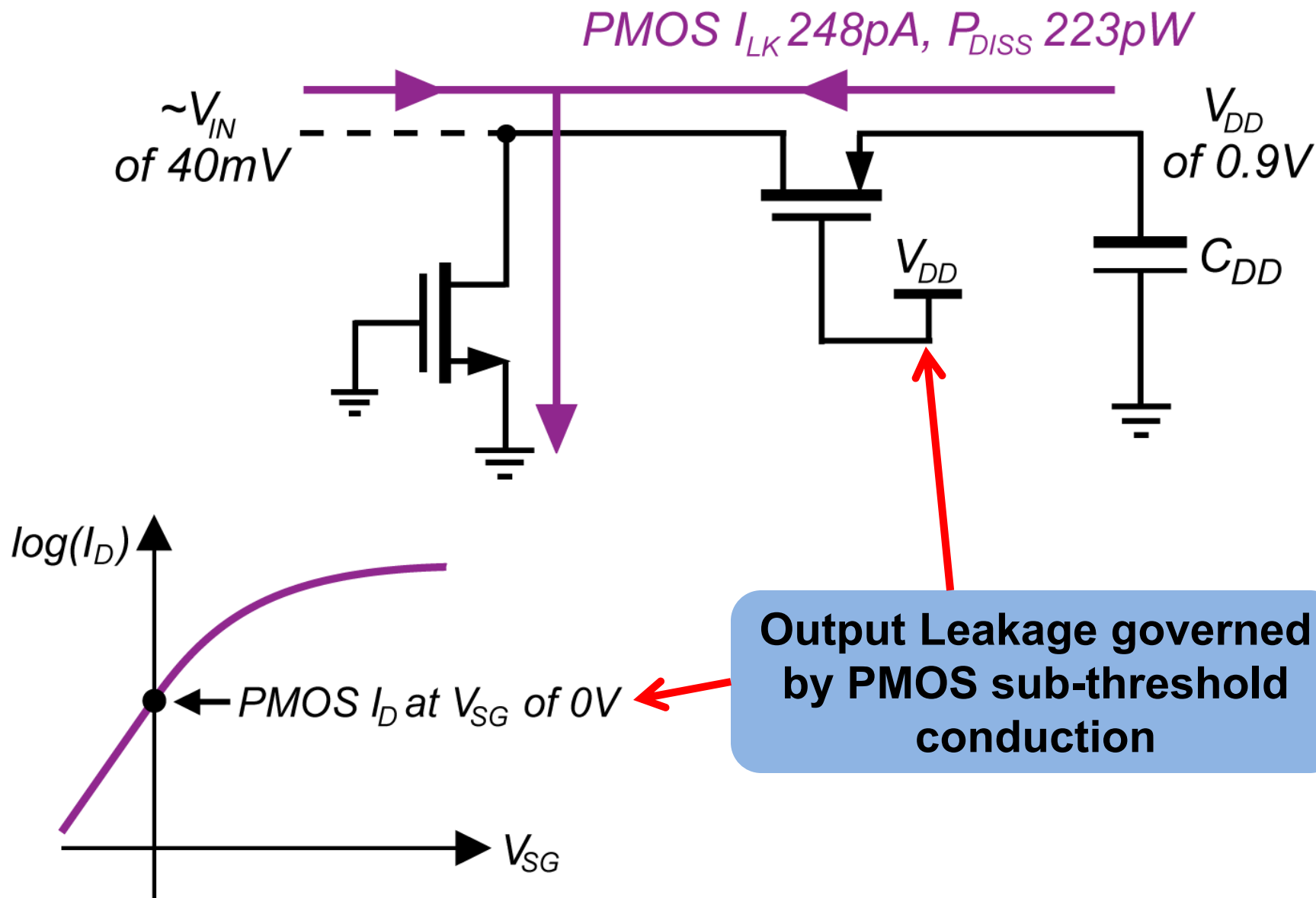
Loss due to Leakage from  
Input of 40mV: 20pW

Loss due to Leakage from  
Output of 0.9V: 223pW

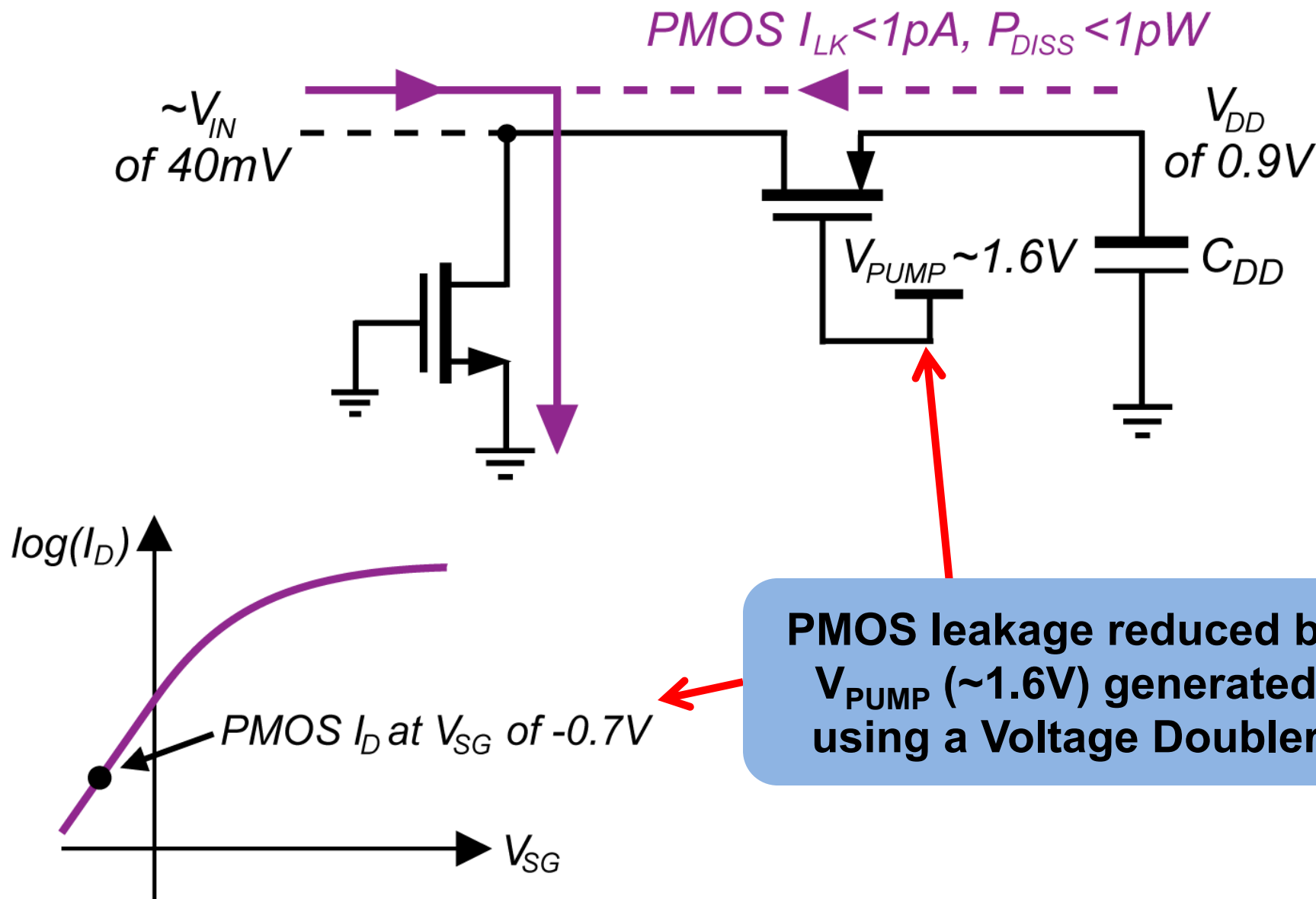


**Power Loss due to Leakage from Output Path more than  
from Input Path**

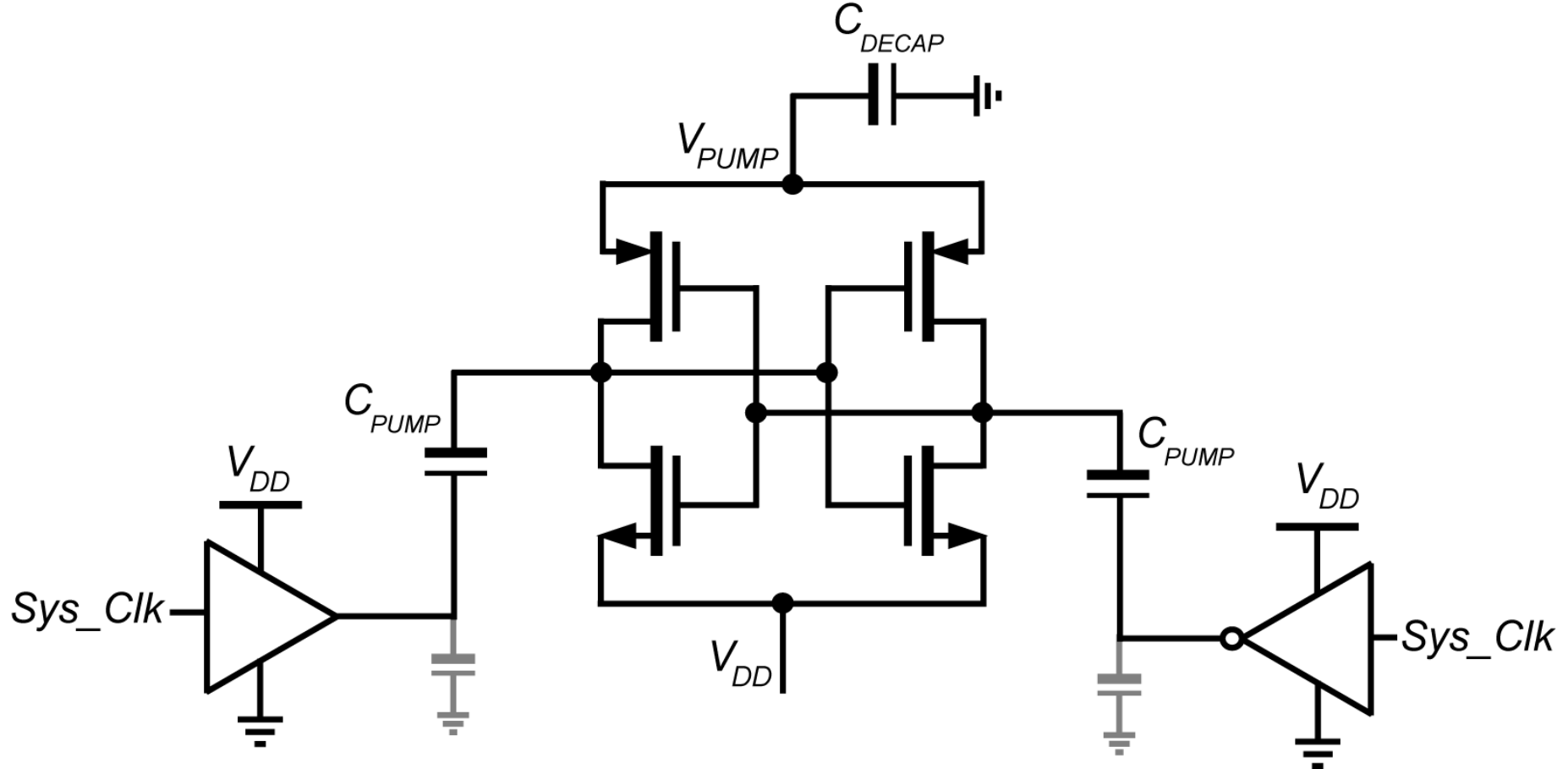
# Reducing Leakage Losses



# Reducing Leakage Losses



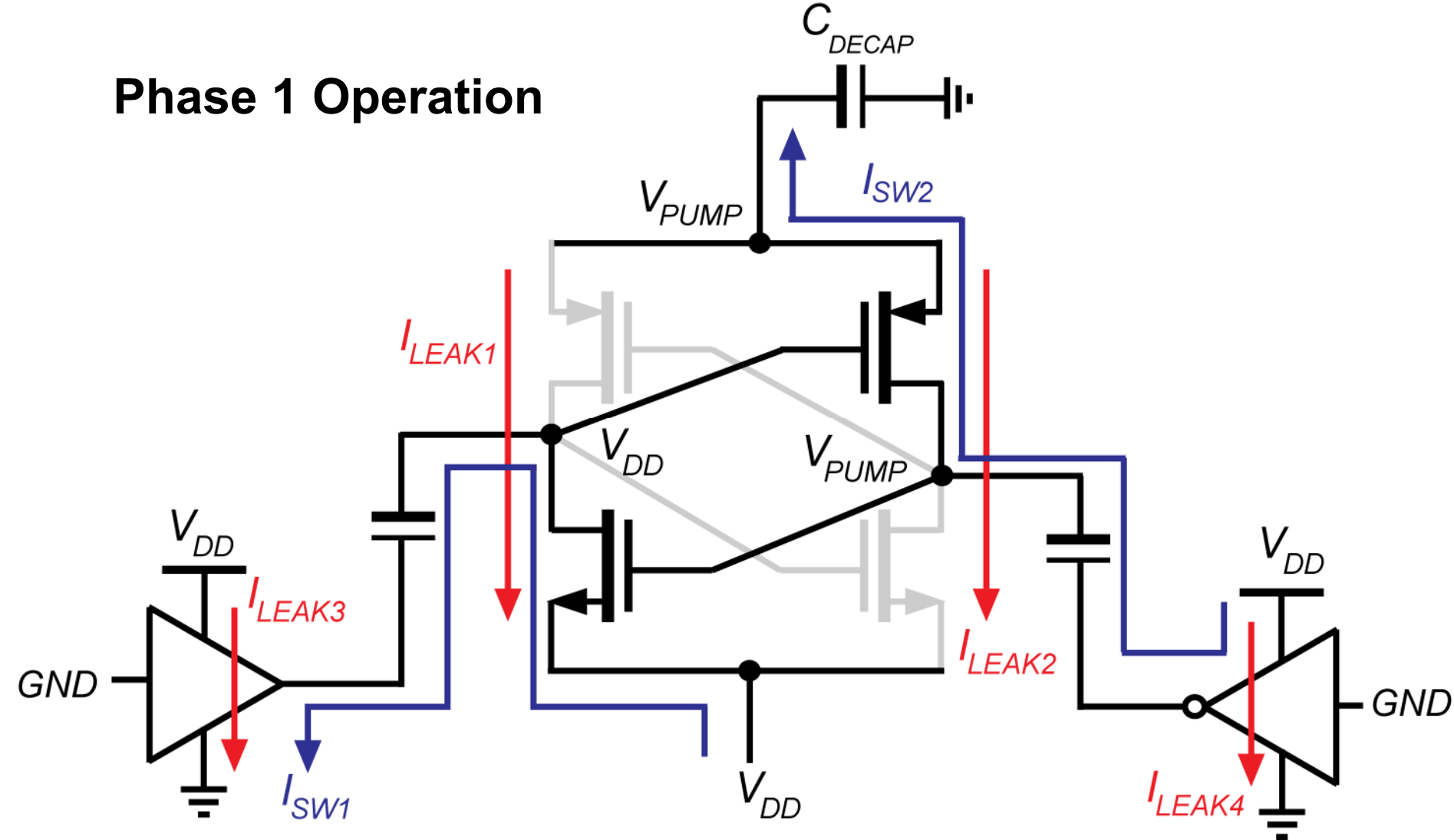
# Charge Pump



- $V_{DD}$  ( $\sim 0.9V$ ) converted to  $V_{PUMP}$  (1.6-1.7V) with 77% efficiency
- All capacitors-  $C_{PUMP}$  and  $C_{DECAP}$  integrated

# Charge Pump Operation

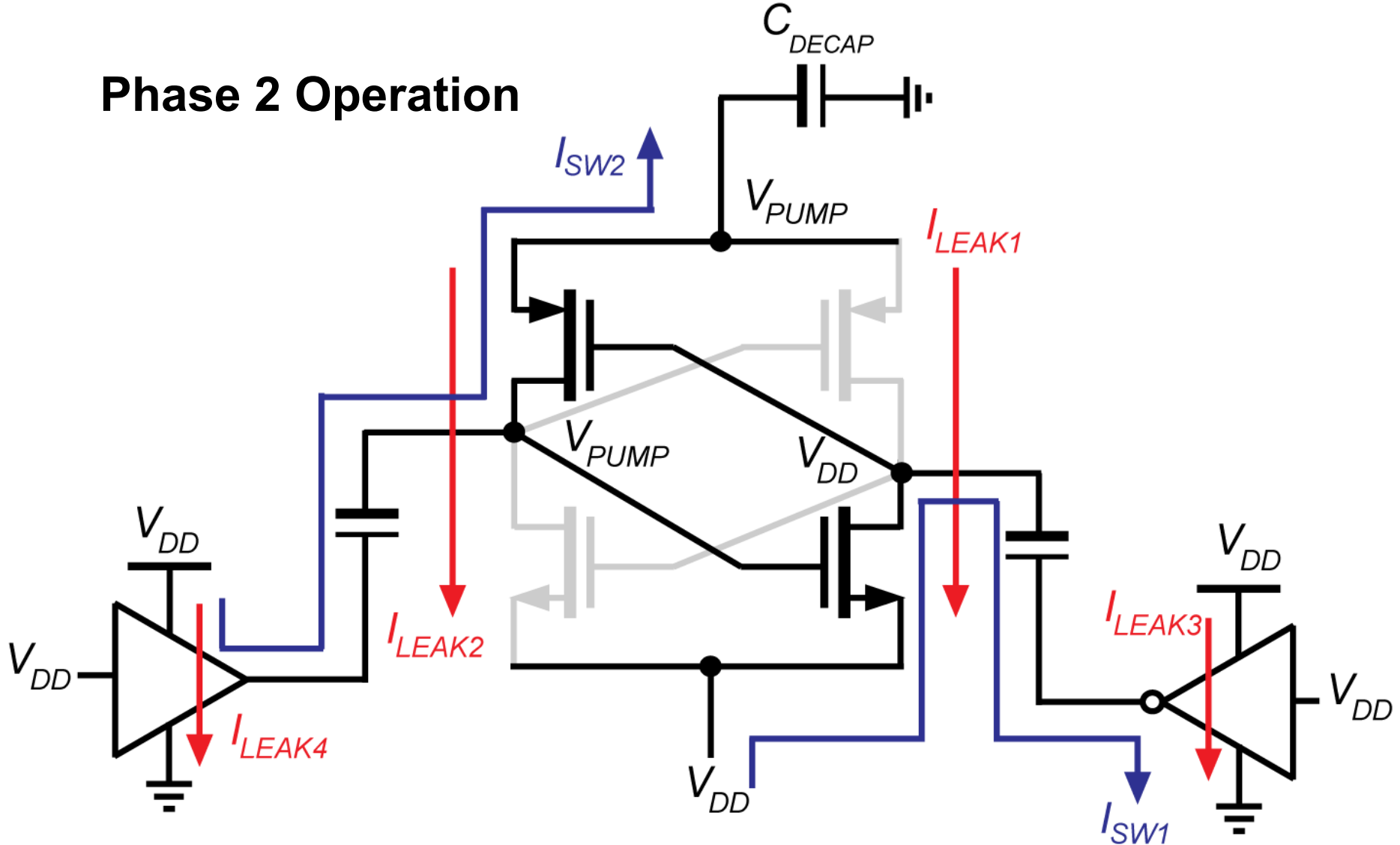
## Phase 1 Operation



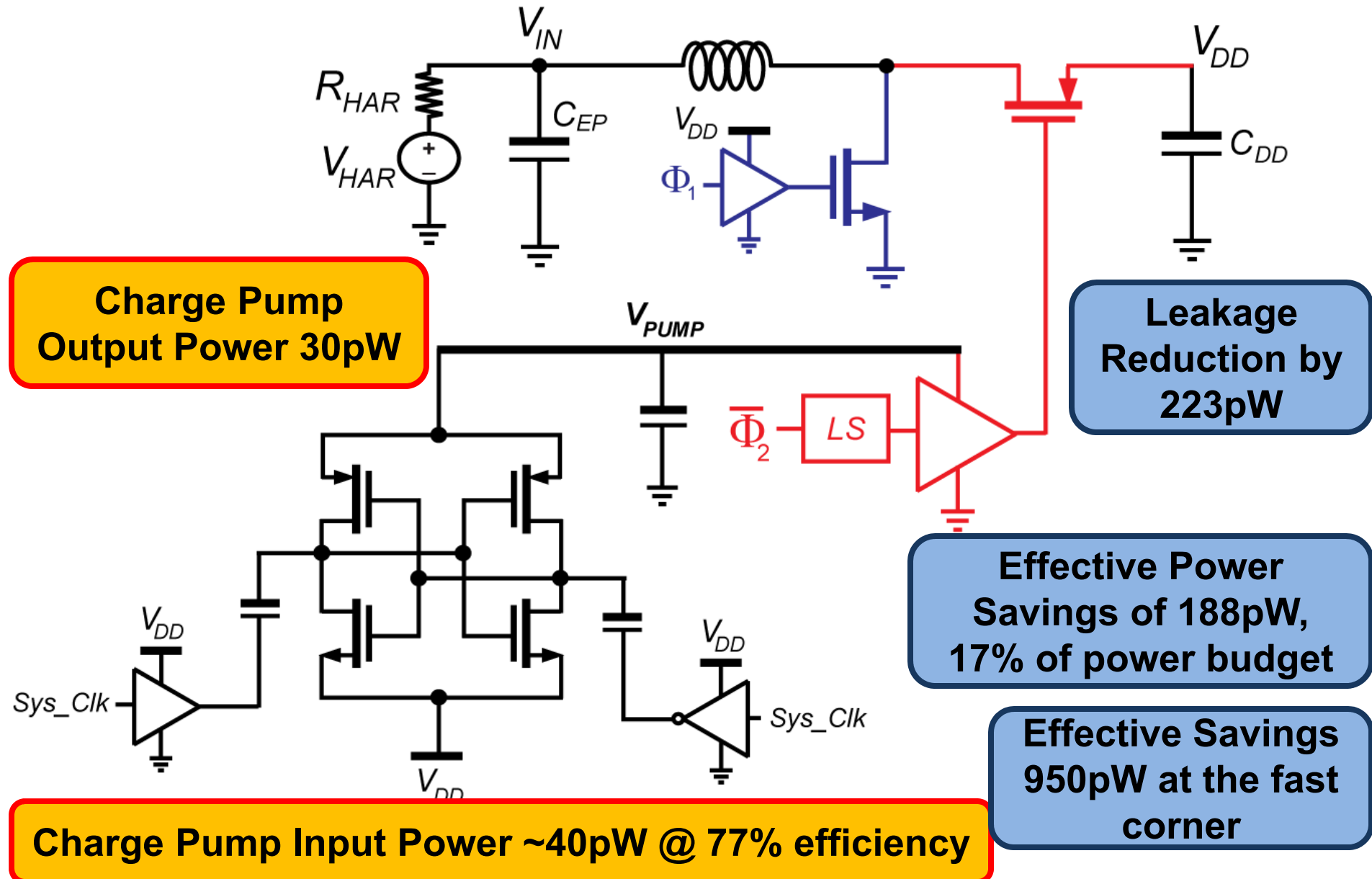


\_\_\_\_\_

## Phase 2 Operation



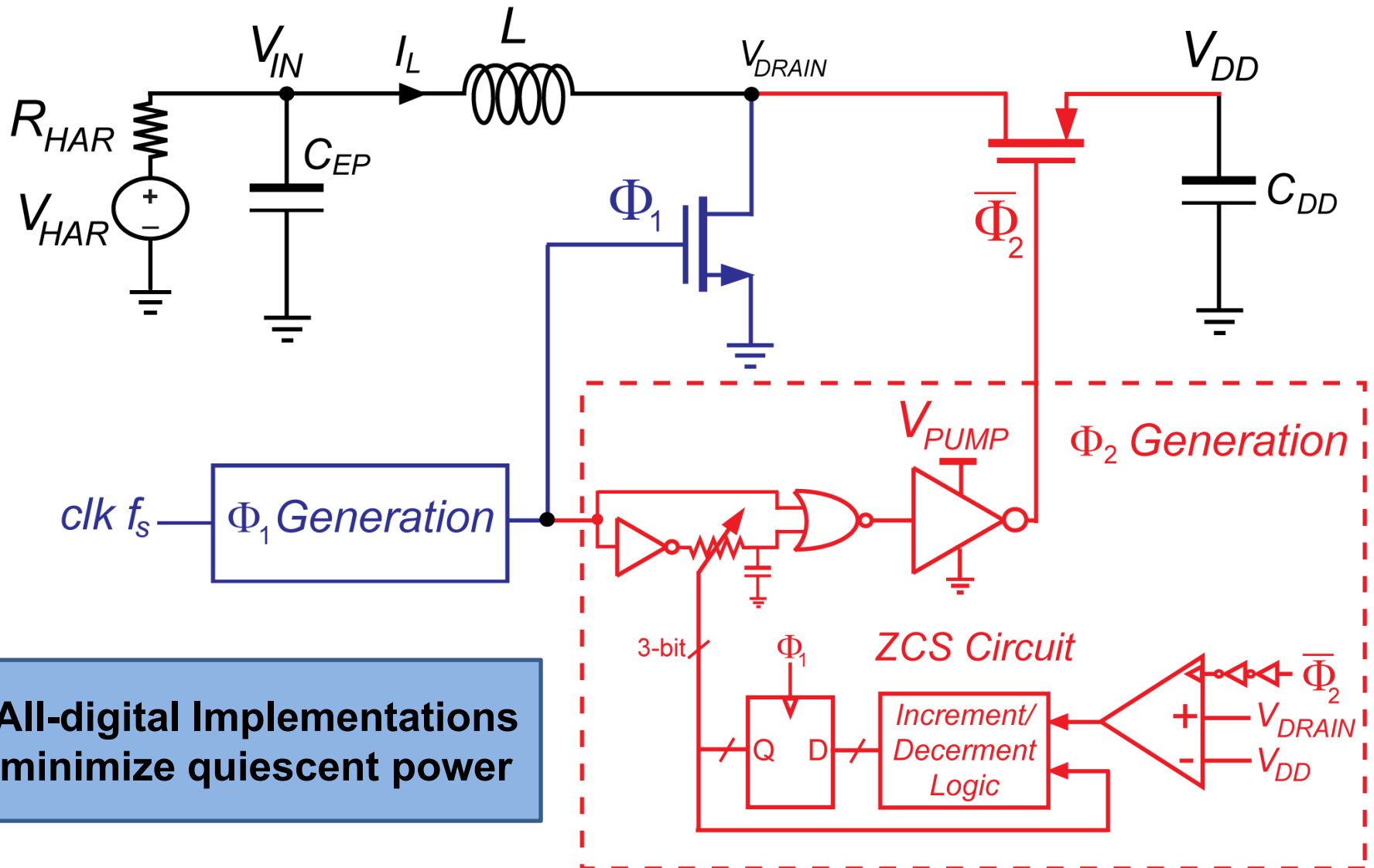
# pW Charge Pump Benefit



\_\_\_\_\_



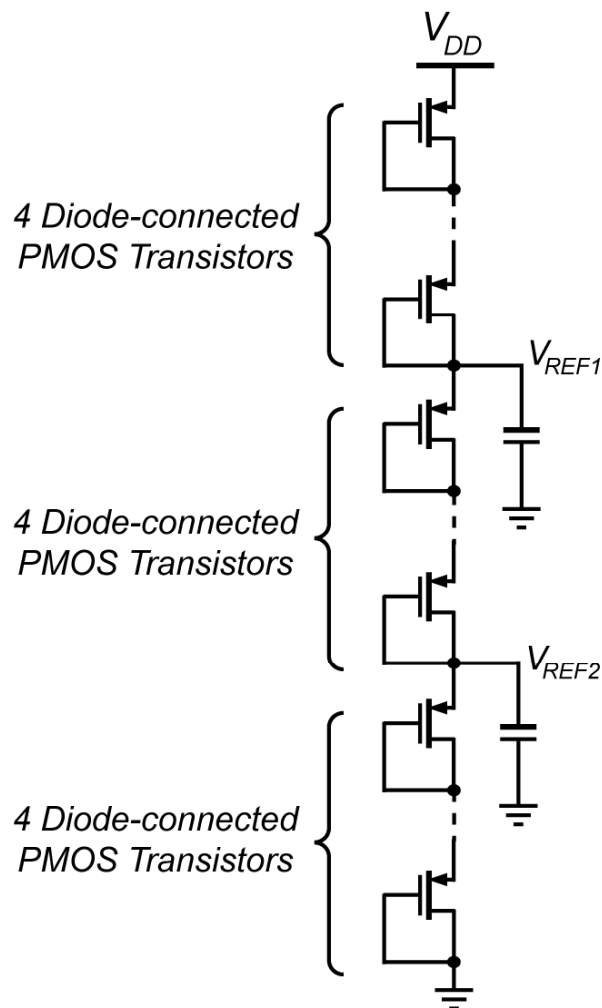
# $\Phi_2$ Pulse Generation



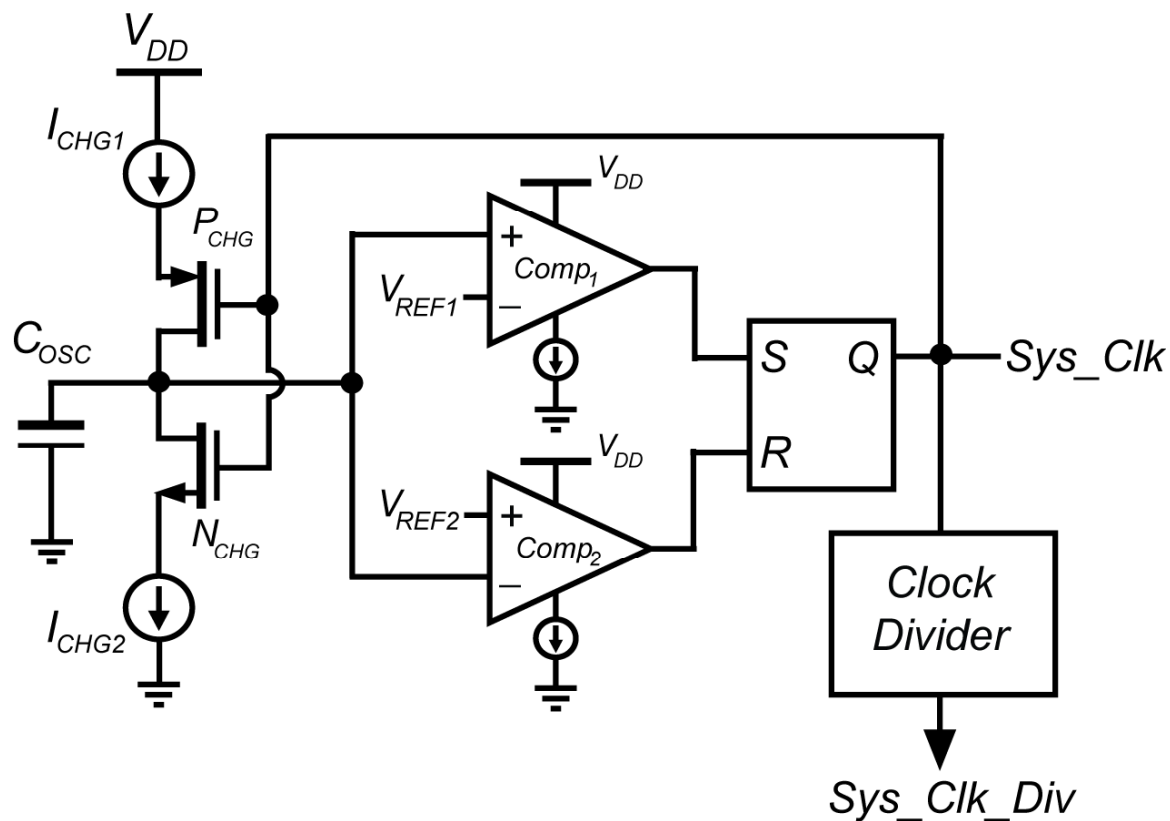
**All-digital Implementations  
minimize quiescent power**

# Ultra-low power Timer

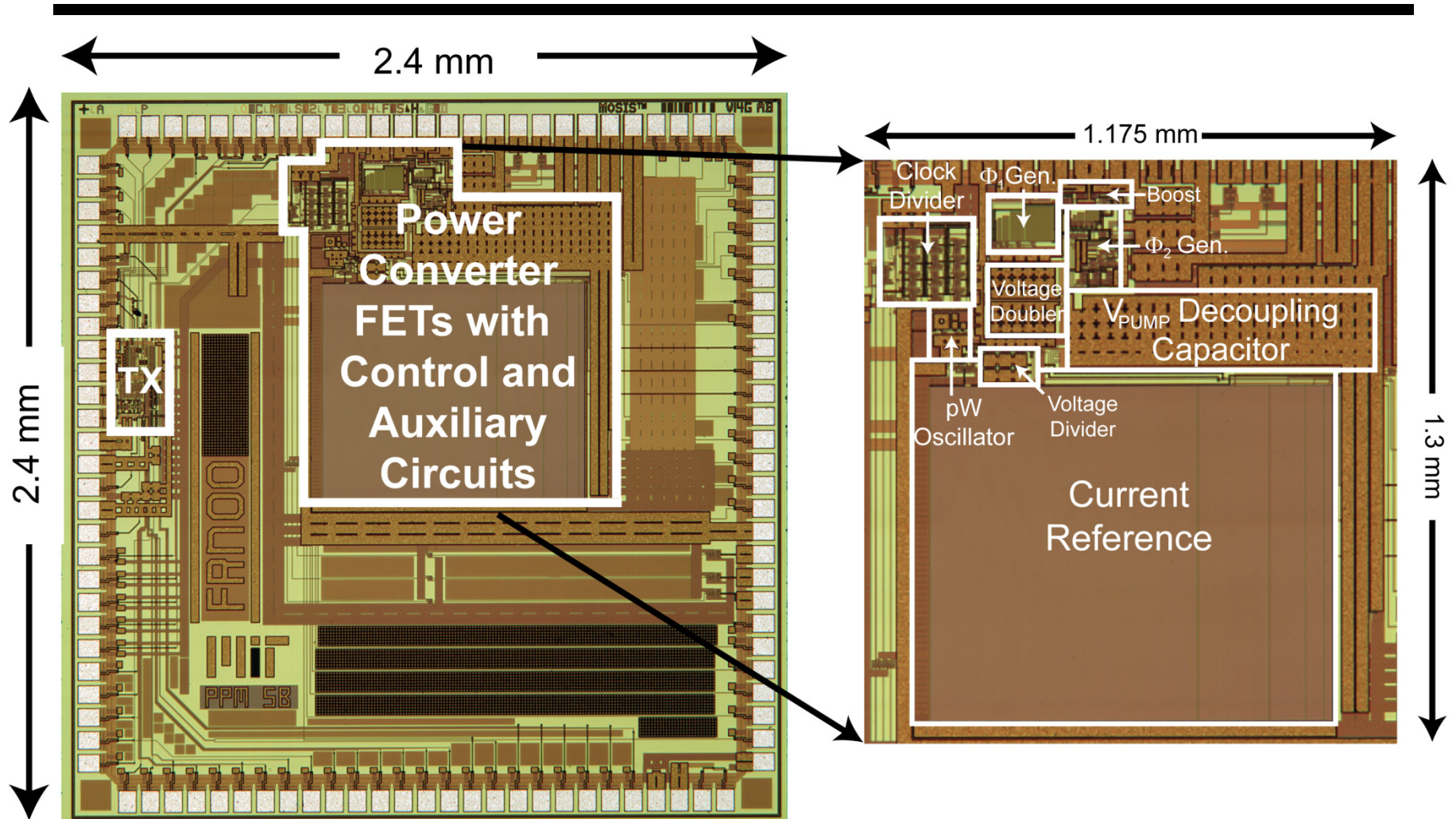
Voltage divider generating  
 $V_{REF1}$  and  $V_{REF2}$



Relaxation Oscillator with Clock  
Divider and Constant  $g_m$ -Current  
Reference for  $I_{CHG1}$  and  $I_{CHG2}$



# Die Micrograph

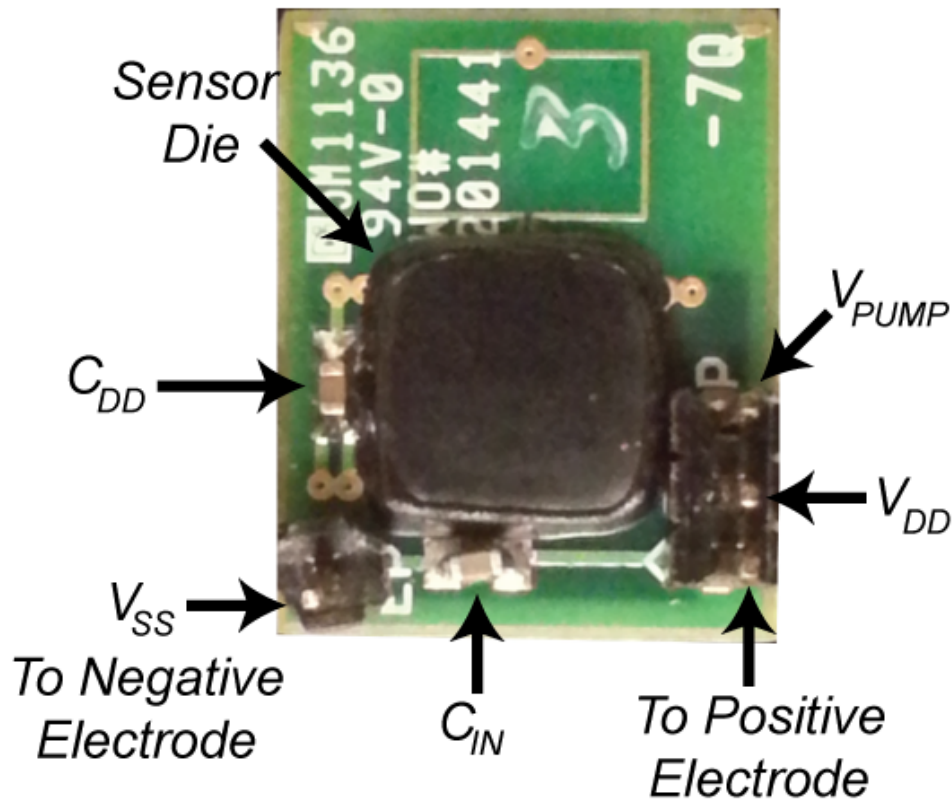


Sensor Implemented in a  $0.18\mu\text{m}$  CMOS Process

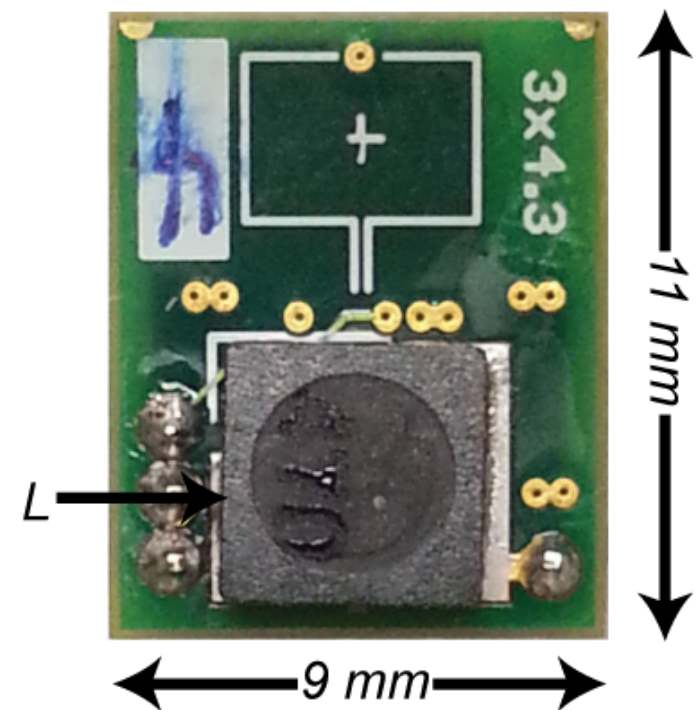


# Sensor PCB

Front



Back



# Outline

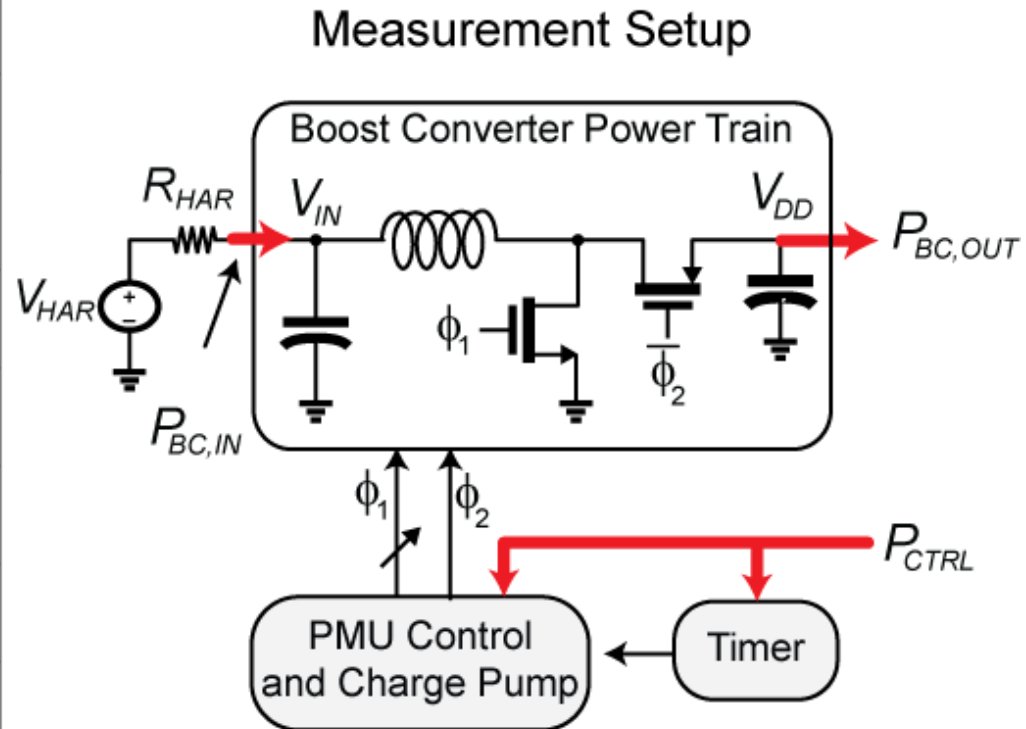
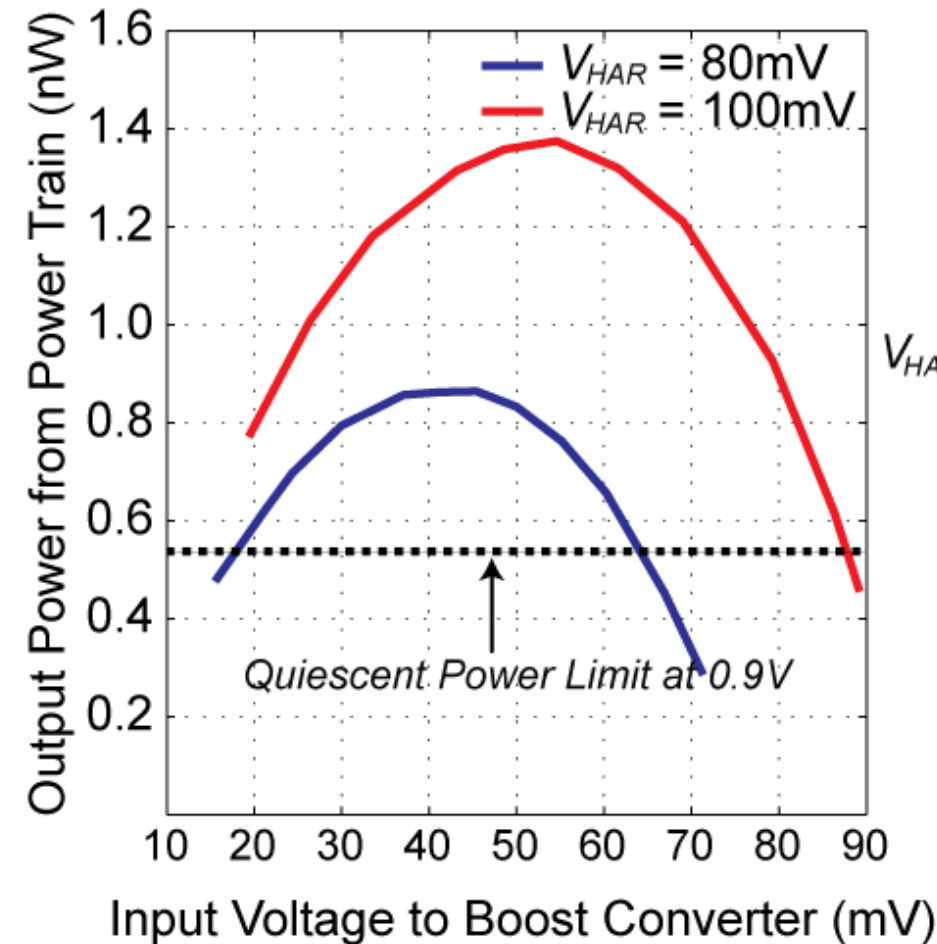
---

- Details of the nW Power Management Unit
  - Boost Converter- Design Considerations and Losses
  - Charge Pump for Leakage Reduction
  - pW Control Circuits
- Measured Results
  - Boost Converter Efficiency
  - Quiescent Power of Controller
  - Transient Measurements
- Comparison with state-of-art and Conclusions



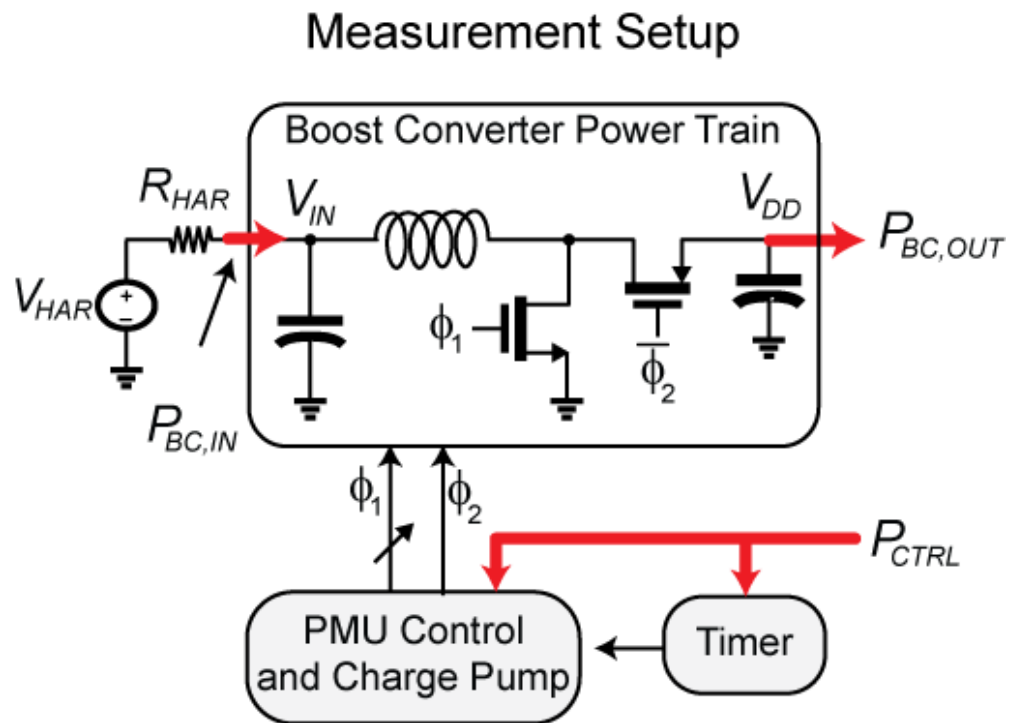
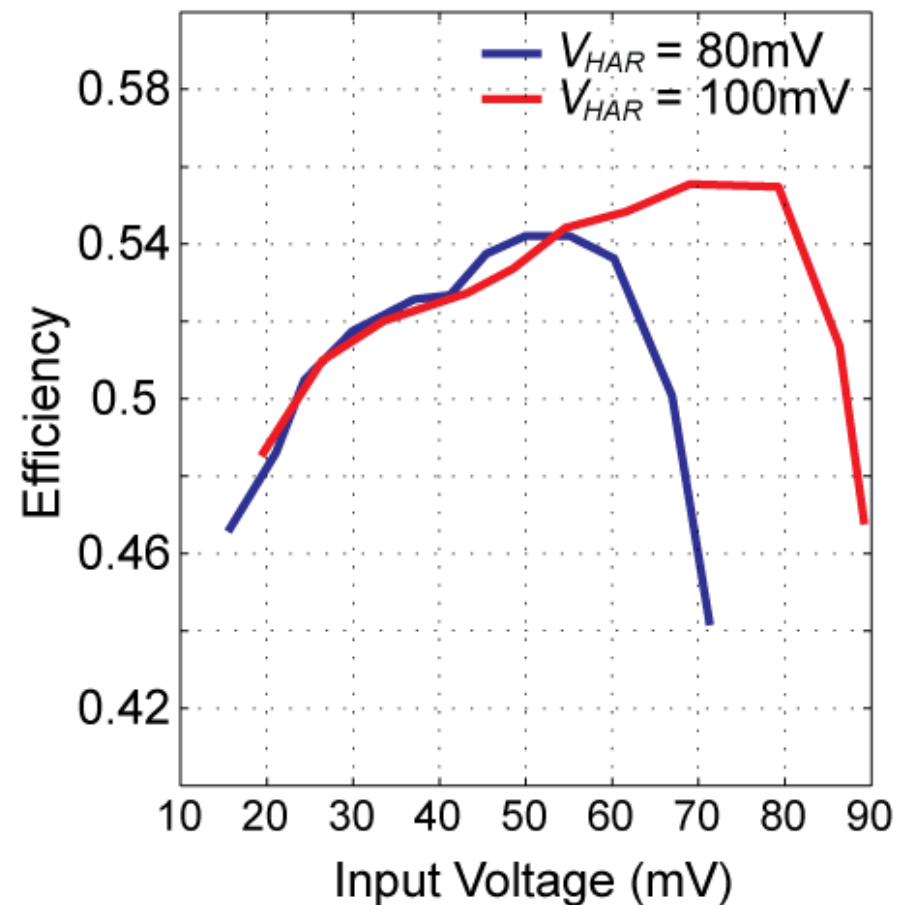
# Boost Converter Output Power

Boost Converter Output Power for  $R_{HAR}$  of  $1M\Omega$  and  $V_{DD}$  of  $0.9V$

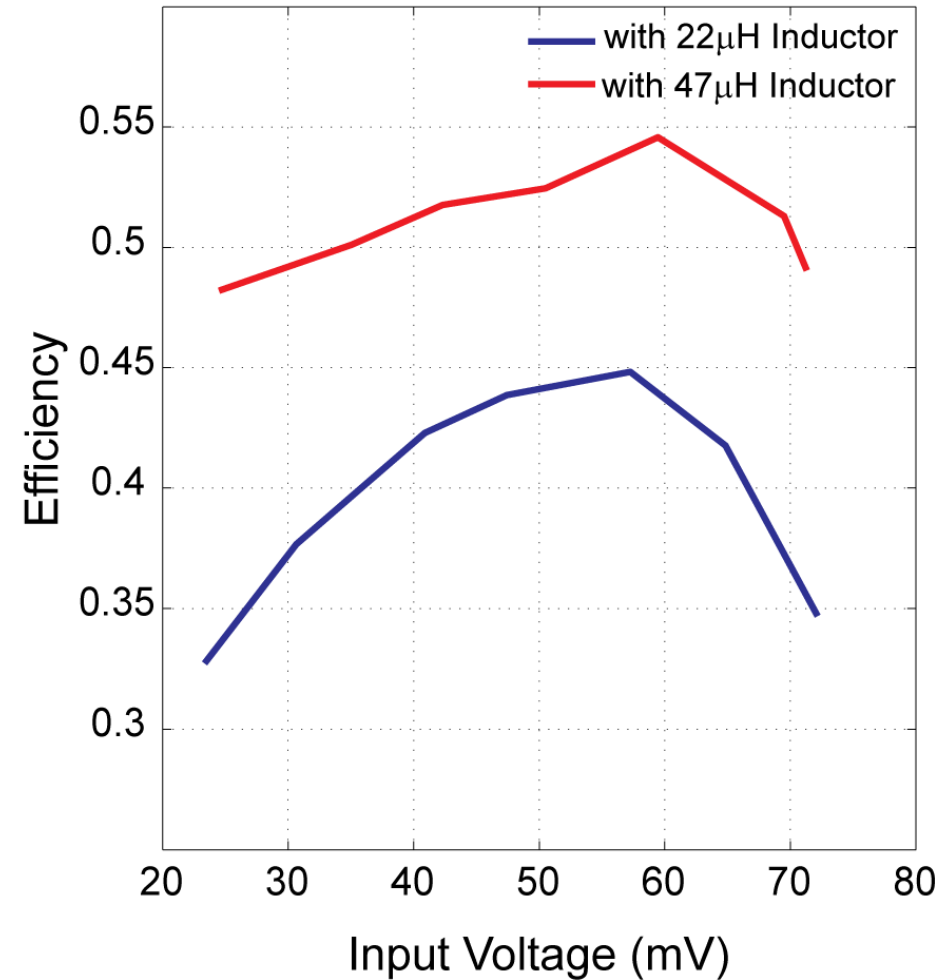
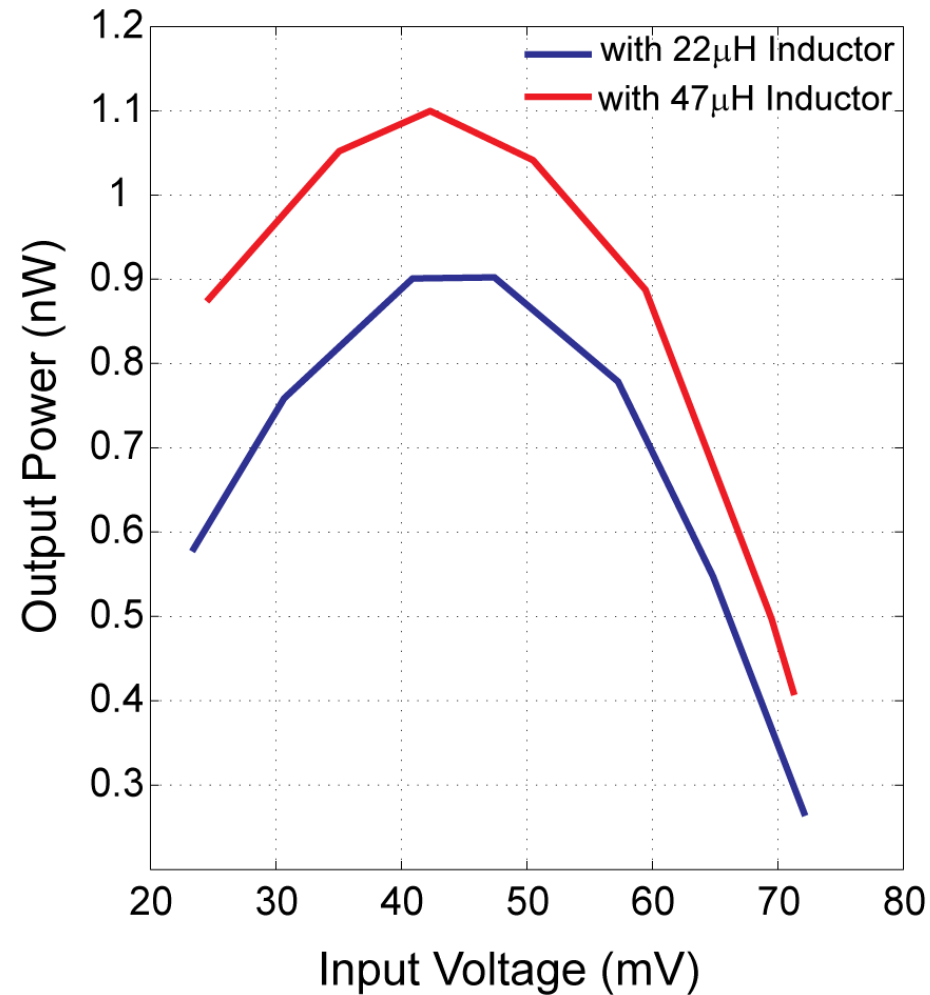


# Boost Converter Efficiency

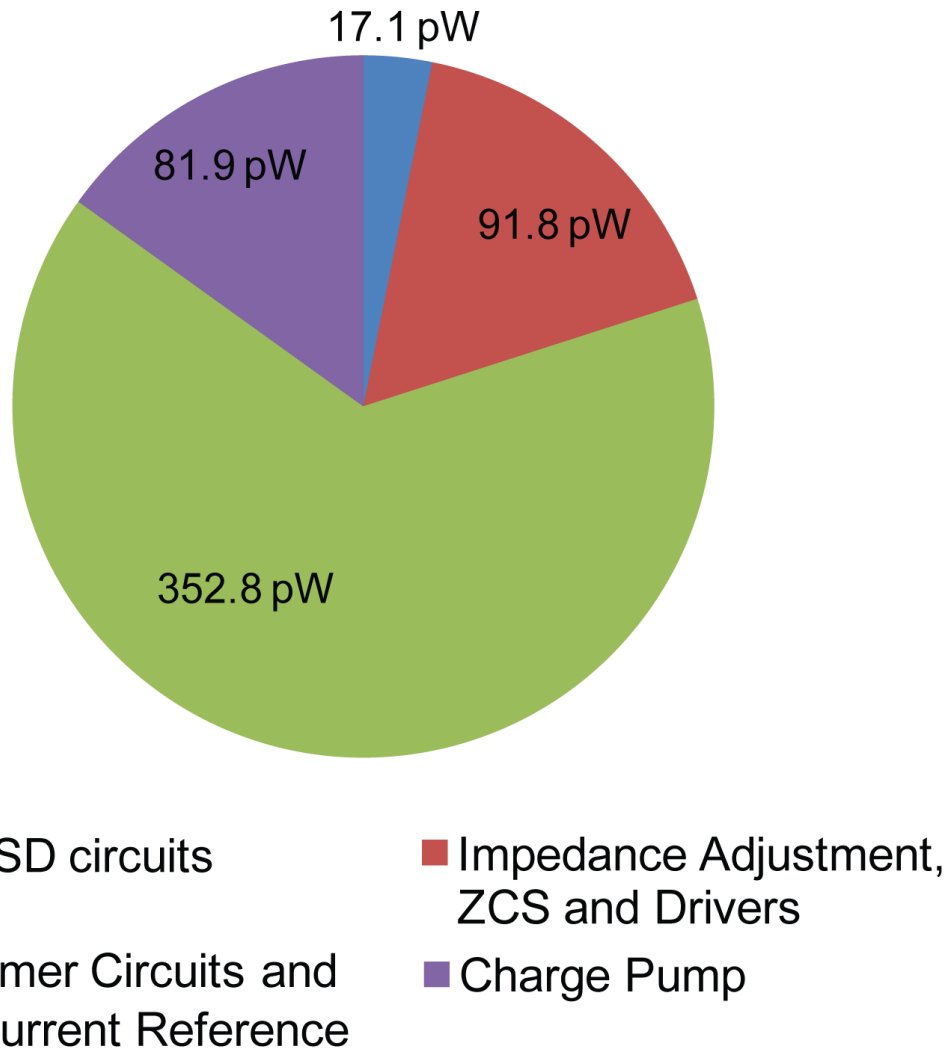
Boost Converter Efficiency for  $R_{HAR}$  of  $1\text{M}\Omega$  and  $V_{DD}$  of  $0.9\text{V}$



# Effect of Smaller Boost Converter Inductance



# Quiescent Power and Design Summary

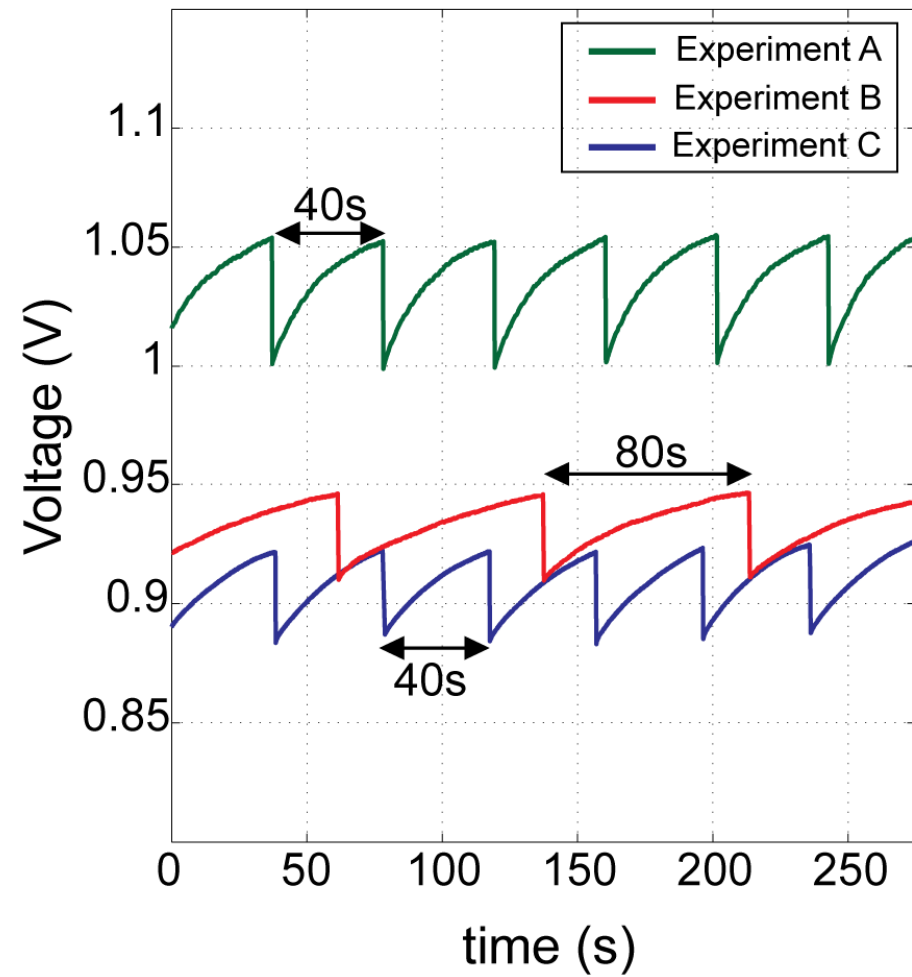


## PMU Design Summary

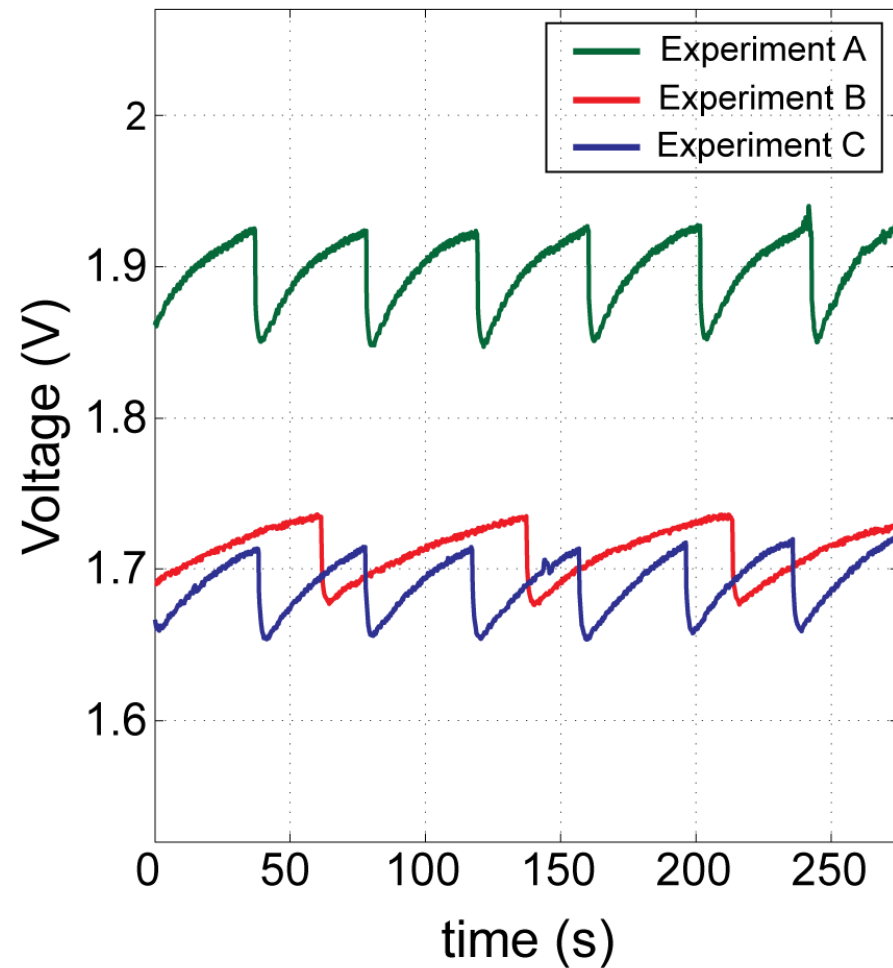
Technology	0.18μm CMOS
Input Voltage	20-70mV
Output Voltage	0.8-1.1V
Peak Efficiency	56%
Quiescent Power of Controller and Auxiliary Circuits	544pW

# Transient Results

$V_{DD}$  measurement



$V_{PUMP}$  measurement



# Comparison with State-of-Art

	ISSCC 2012	TPS62736	ISSCC 2011	This Work
Topology	Boost	Buck	Switched Capacitor Charge Pump (Boost)	Boost with Voltage Doubler
Voltage Conversion	80mV-2.5V boosted to 3-5V	2-5.5V step down to 1.3-5V	450mV boosted to 3.6V	Inductive Boost:- 20-70mV boosted to 0.8-1.1V Charge Pump:- 0.8-1.1V boosted to 1.5-1.9V
Converter Output Power	1 $\mu$ W-30mW	2.5 $\mu$ W-125mW	10nW to 160nW	544pW-4nW
Converter Efficiency at Ultra-Low Power	20% at 1 $\mu$ W	55% at 2.5 $\mu$ W	35% at 10nW	53% at 1.2nW (1.1nW in PMU)
Quiescent Power	9.9nW	760nW	7.3nW	544pW

# Conclusions

---

- Power Management Unit of a sensor with an overall power budget of 1.1nW
- Ultra-low power boost converter with peak 56% efficiency for ultra-low energy harvesters
- pW Charge Pump for leakage reduction in boost converter
- Always on Circuits (Control and Bias) with 544pW quiescent power for system sustainability

## ***Acknowledgements:-***

This work is funded by the C2S2, IFC, US National Institutes of Health grants K08 DC010419 and T32 DC00038 and the Bertarelli Foundation.

# **A 3nW Fully Integrated Energy Harvester Based on Self-Oscillating Switched- Capacitor DC-DC Converter**

Wanyeong Jung, Sechang Oh, Suyoung Bang,  
Yoonmyung Lee, Dennis Sylvester, David Blaauw

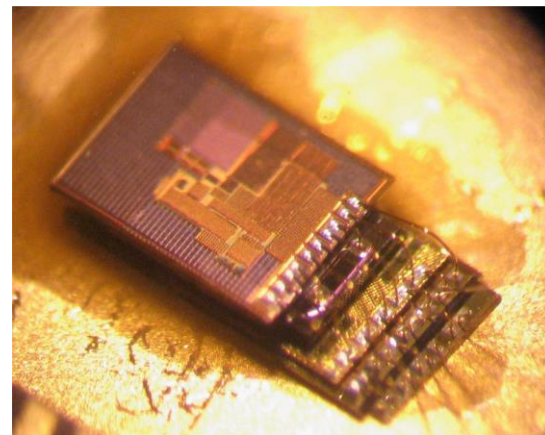
University of Michigan, Ann Arbor, MI



# Motivation

- Powering small wireless systems

- Limited battery capacity due to small size
- Harvested power is also limited by small form factor



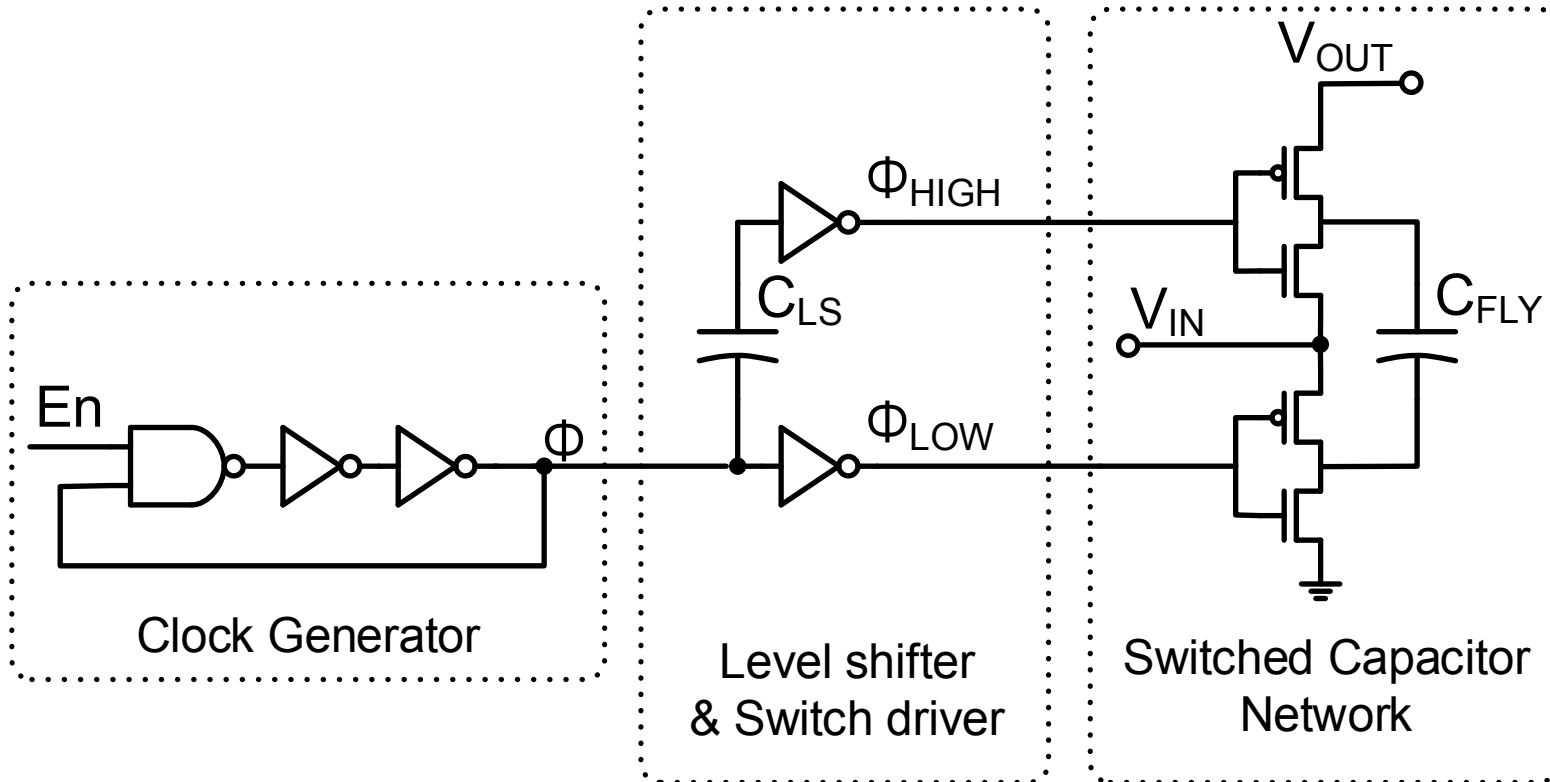
1 mm<sup>3</sup> Die-Stacked Sensing system  
[ Y. Lee et al., JSSC 2013 ]

- Efficient DC-DC up-conversion at low power level is required

- Boost converters require a large inductor
- Switched-capacitor DC-DC converters can be made small

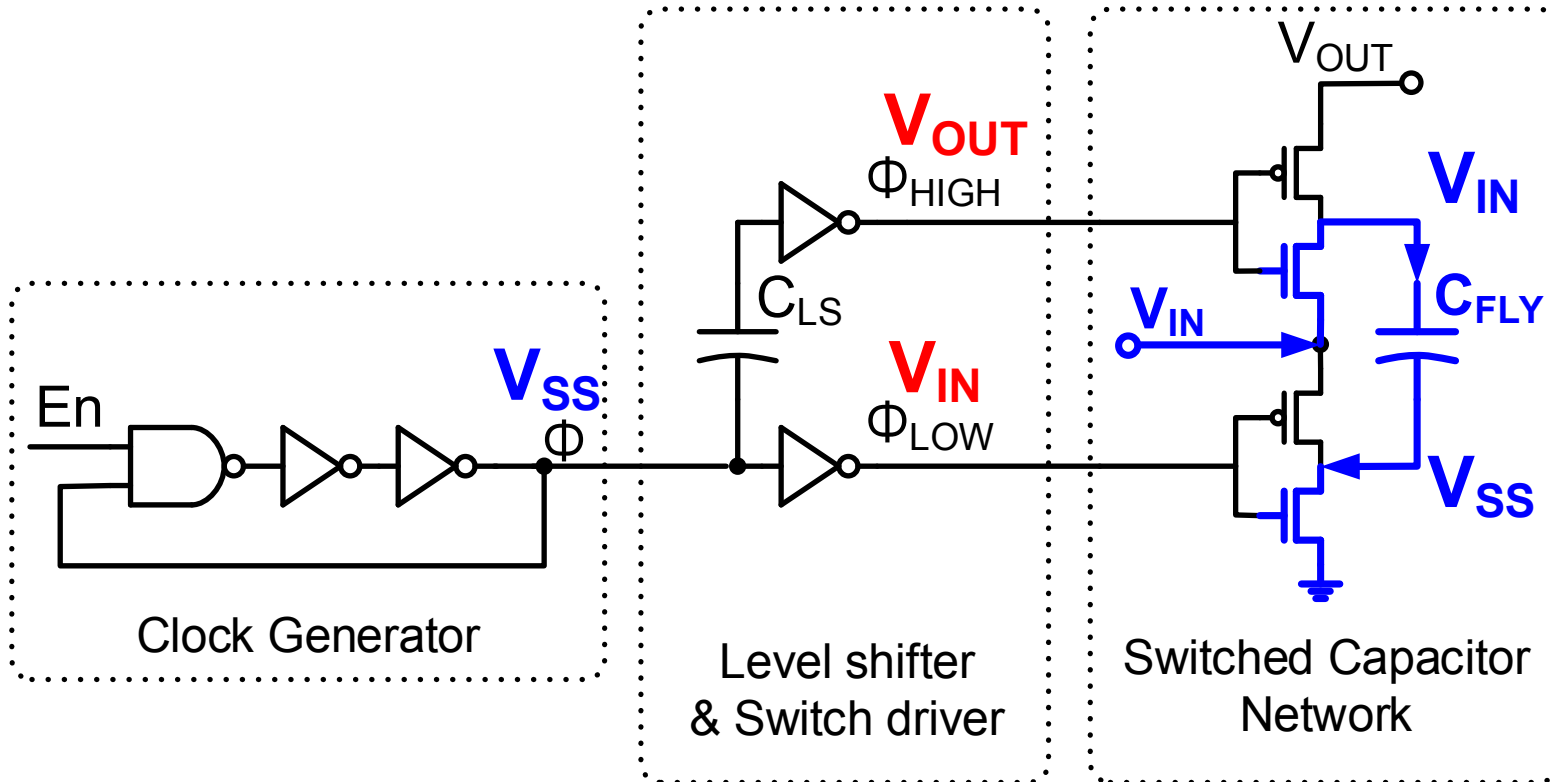
# Conventional Voltage Doubler

- Clock generator + Level shifter + SCN



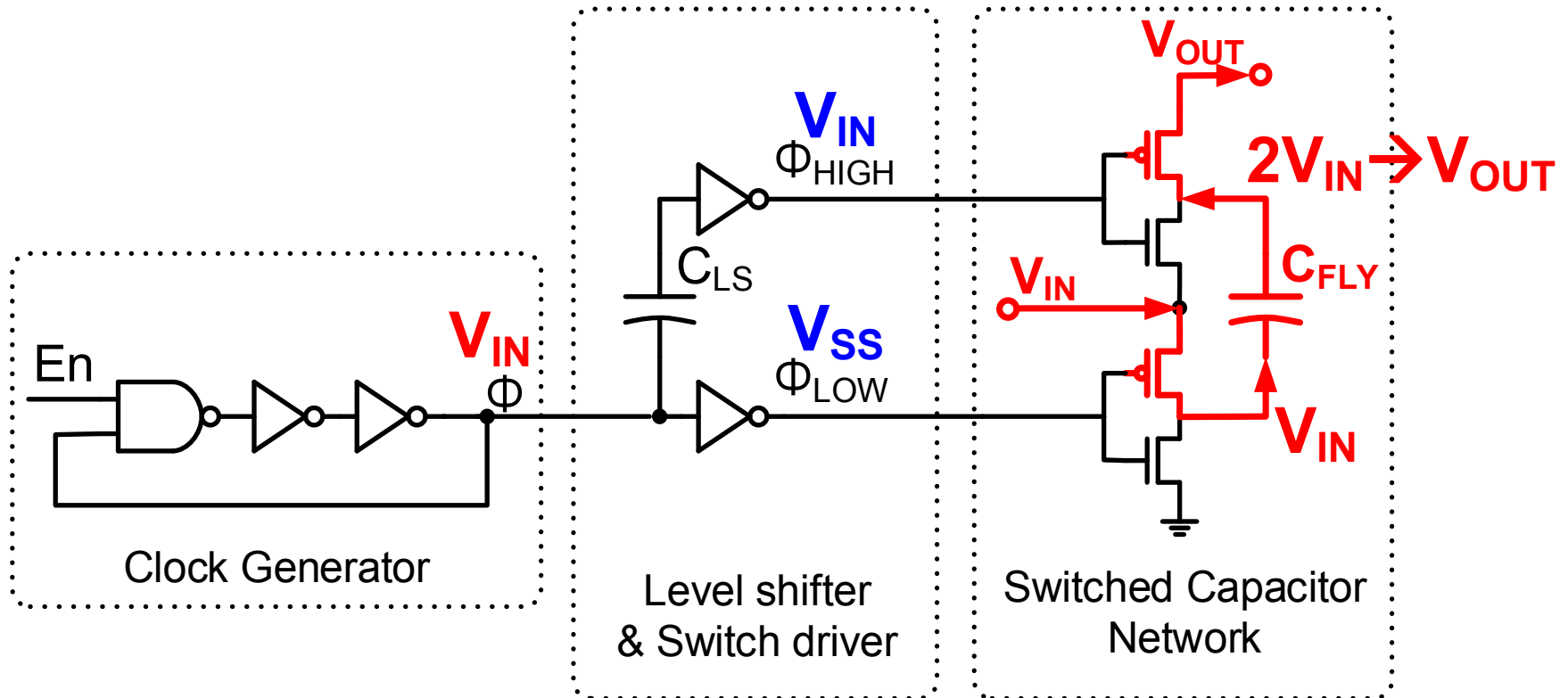
# Conventional Voltage Doubler

- Clock generator + Level shifter + SCN
- Clock makes flying caps oscillate between  $V_{IN} - V_{SS}$  and  $V_{OUT} - V_{IN}$



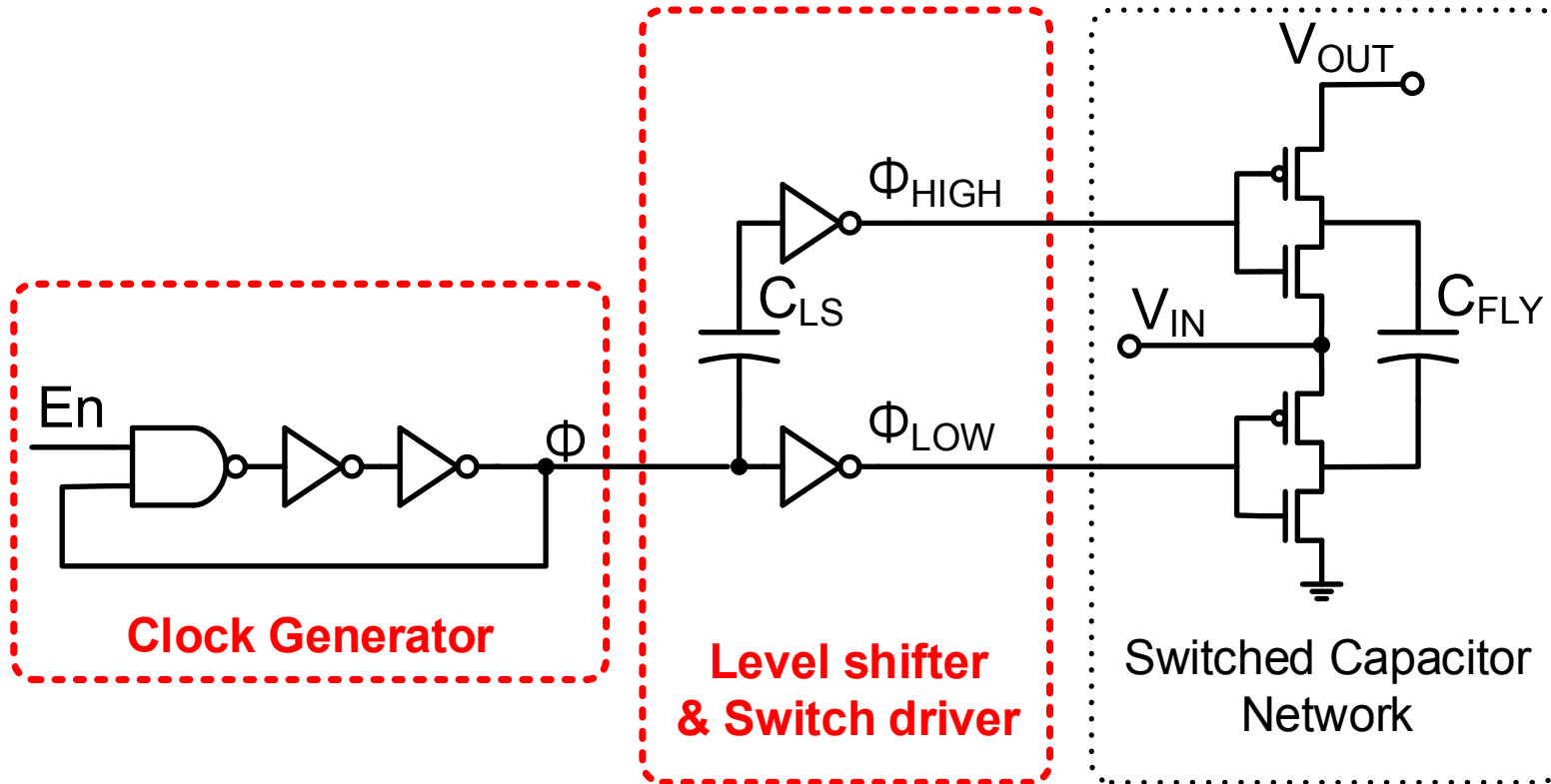
# Conventional Voltage Doubler

- Clock generator + Level shifter + SCN
- Clock makes flying caps oscillate between  $V_{IN} - V_{SS}$  and  $V_{OUT} - V_{IN}$



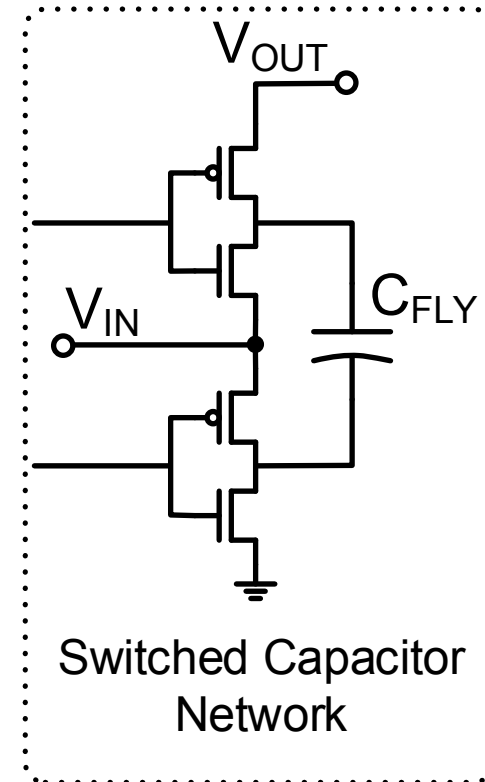
# Conventional Voltage Doubler

- Clock generator + Level shifter + SCN
- Extra power overhead for **clock generation** and **level shifting**



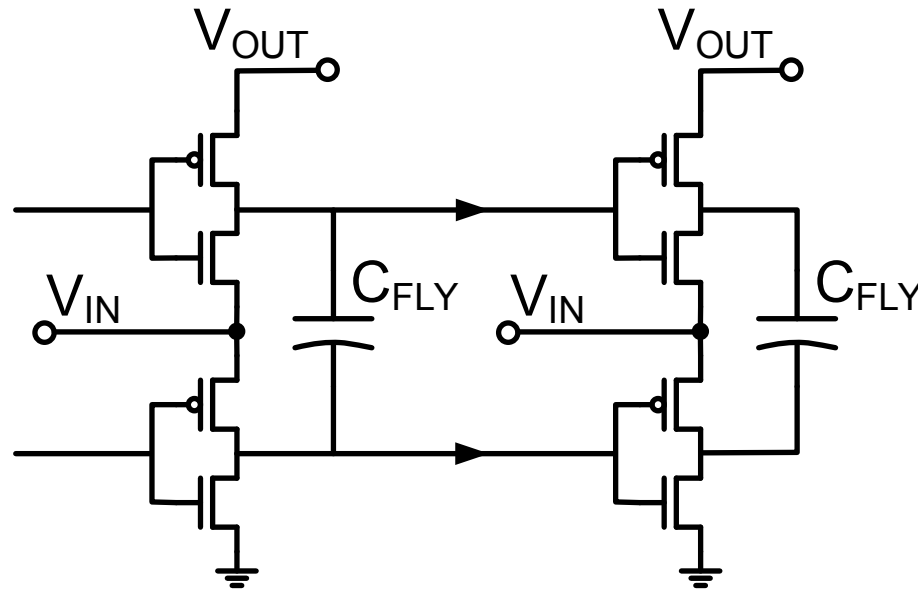
# Proposed Voltage Doubler

- To reduce power overhead, **clock generator** and **level shifter** are **removed**
- How to make SCN operate by itself?



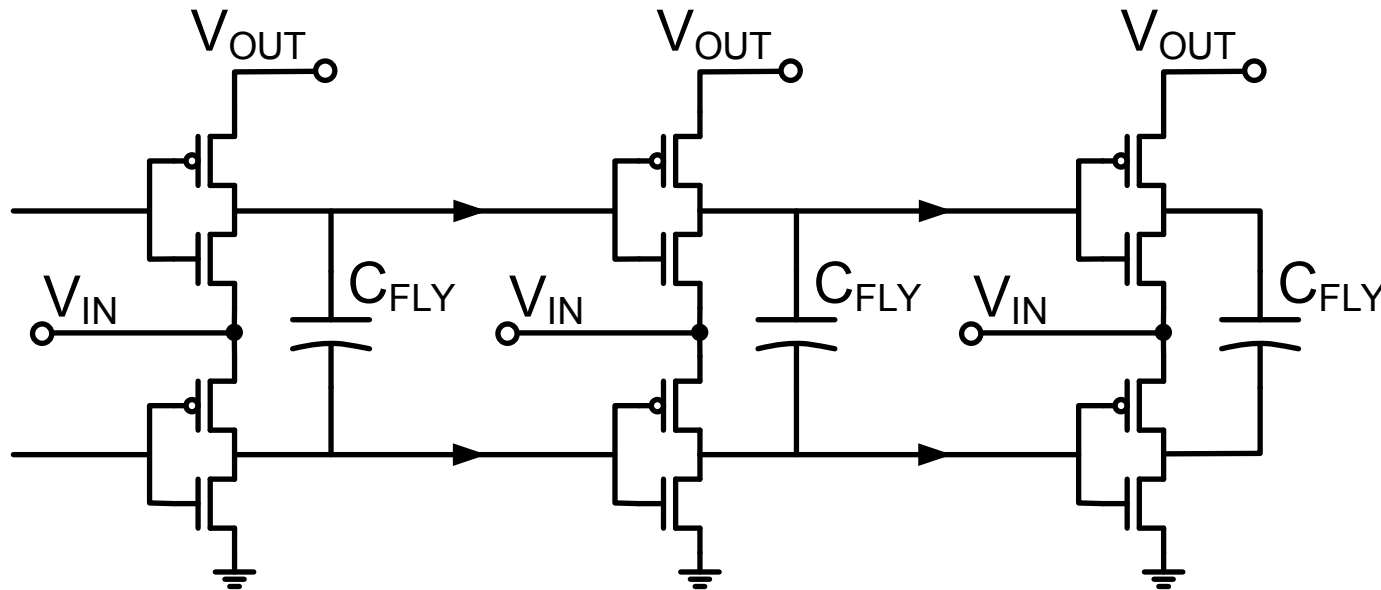
# Proposed Voltage Doubler

- How to make SCN operate by itself?
  - Add another SCN stage to drive the next



# Proposed Voltage Doubler

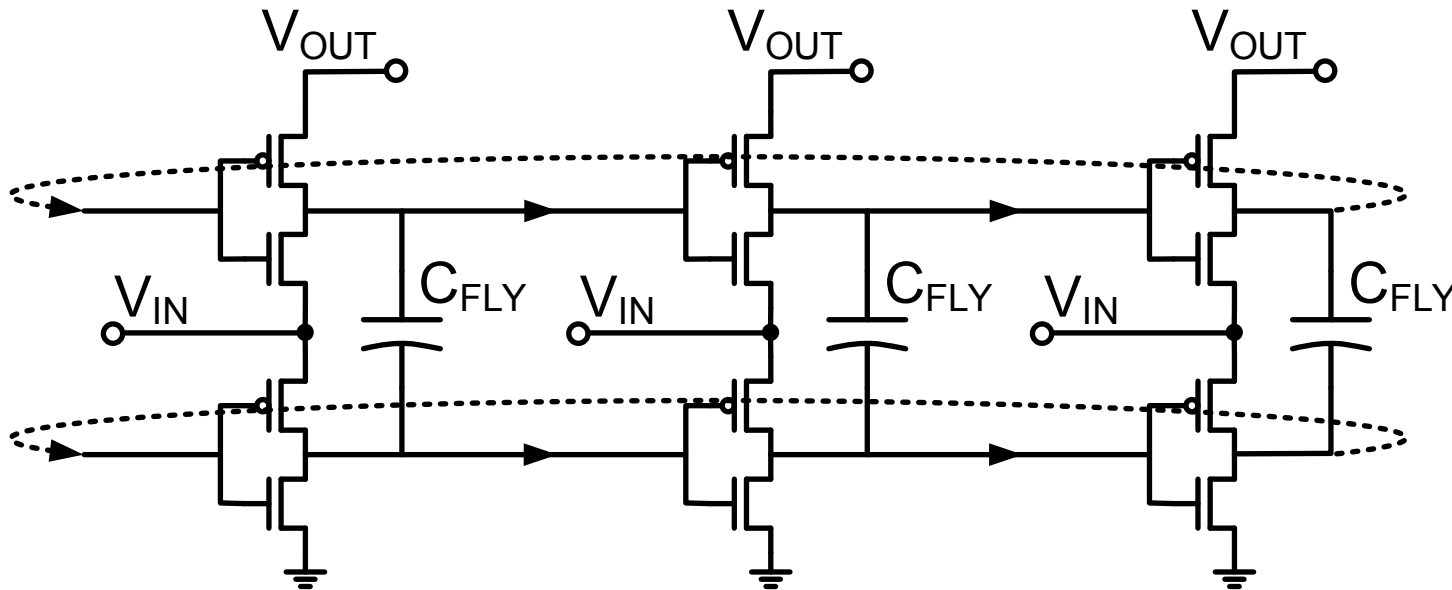
- How to make SCN operate by itself?
  - Add another SCN stage to drive the next



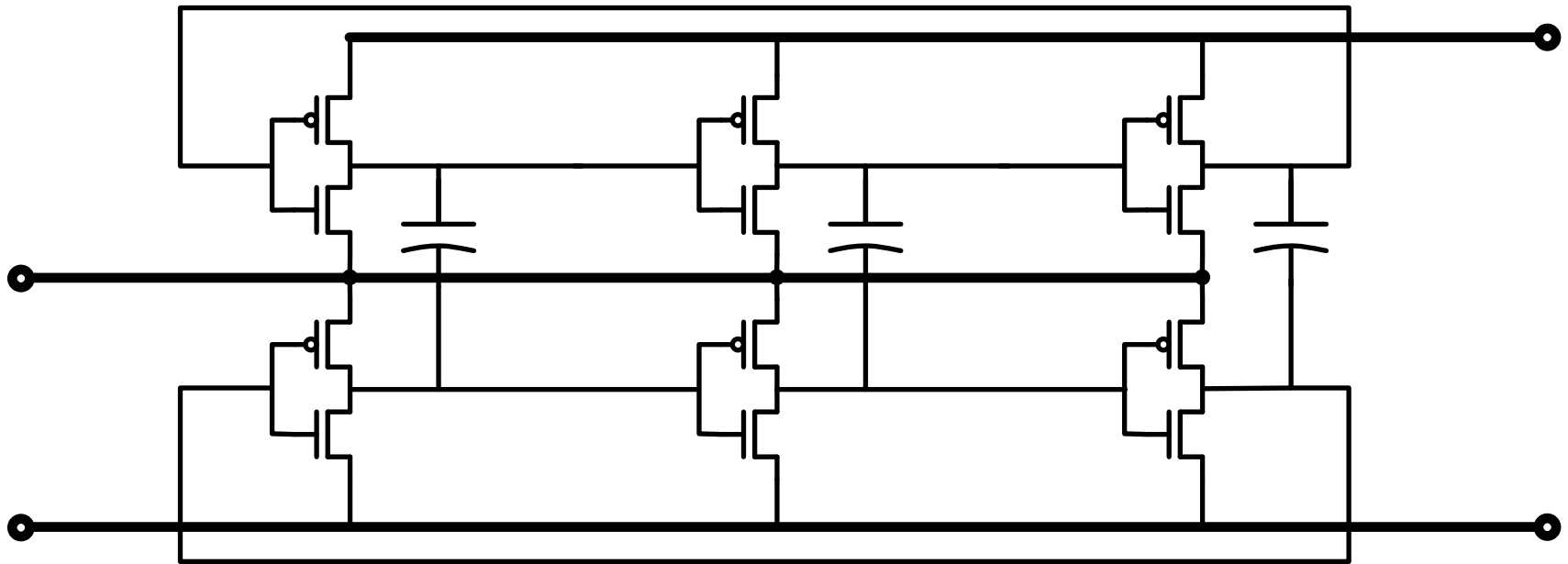


# Proposed Voltage Doubler

- How to make SCN operate by itself?
  - The first stage is driven by the last
  - **SCNs oscillate by themselves**

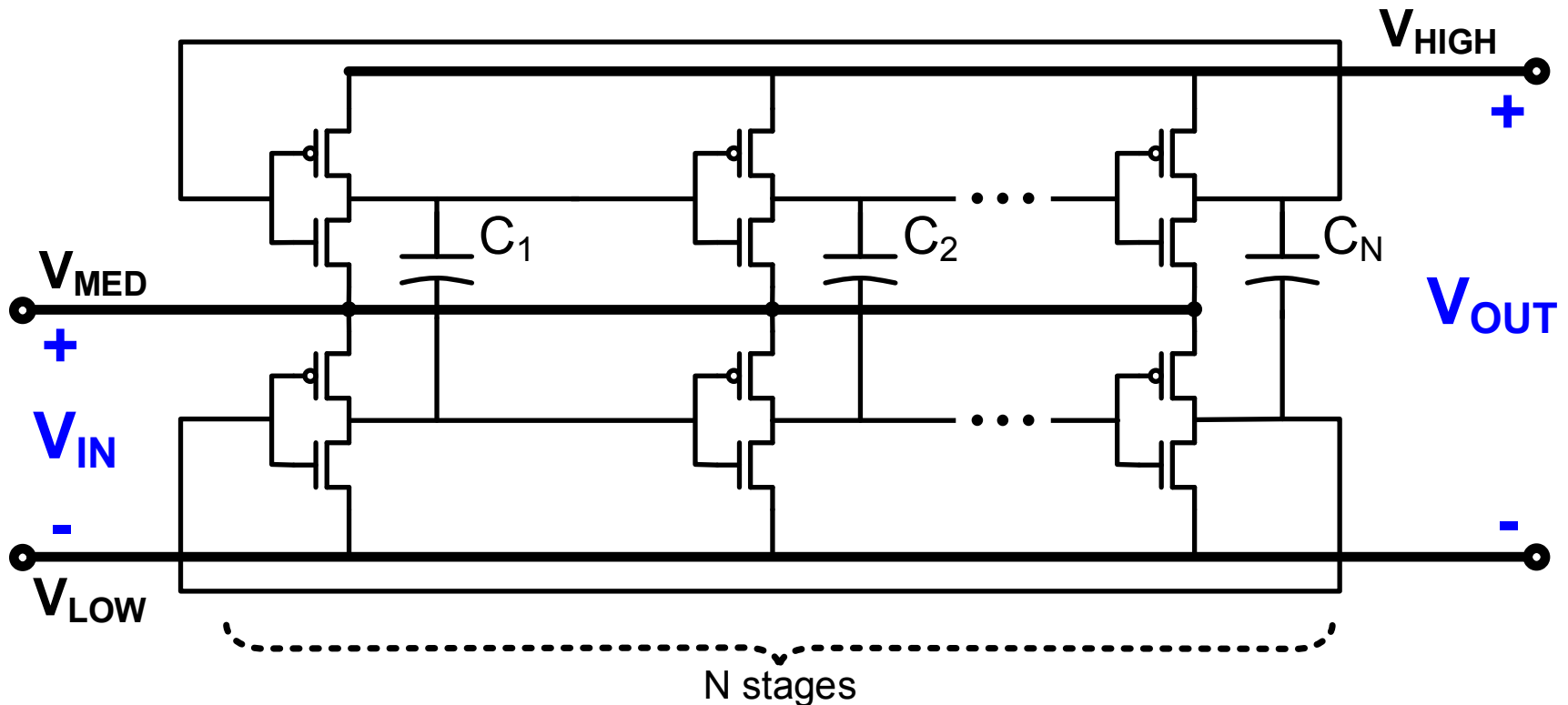


# Self-Oscillating Voltage Doubler



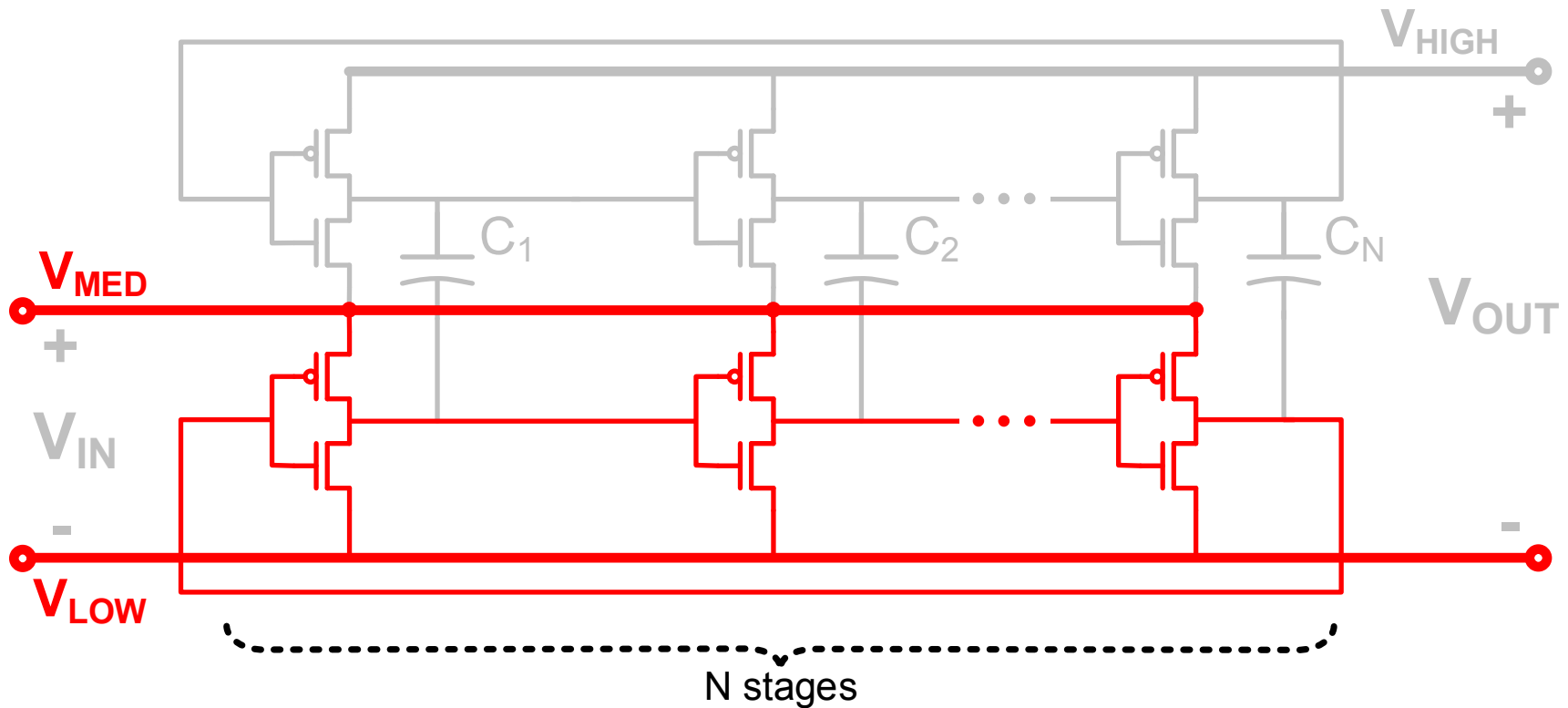
# Self-Oscillating Voltage Doubler

- N stages (N is odd,  $\geq 3$ )
- 3 Power terminals -  $V_{\text{LOW}}$ ,  $V_{\text{MED}}$ ,  $V_{\text{HIGH}}$



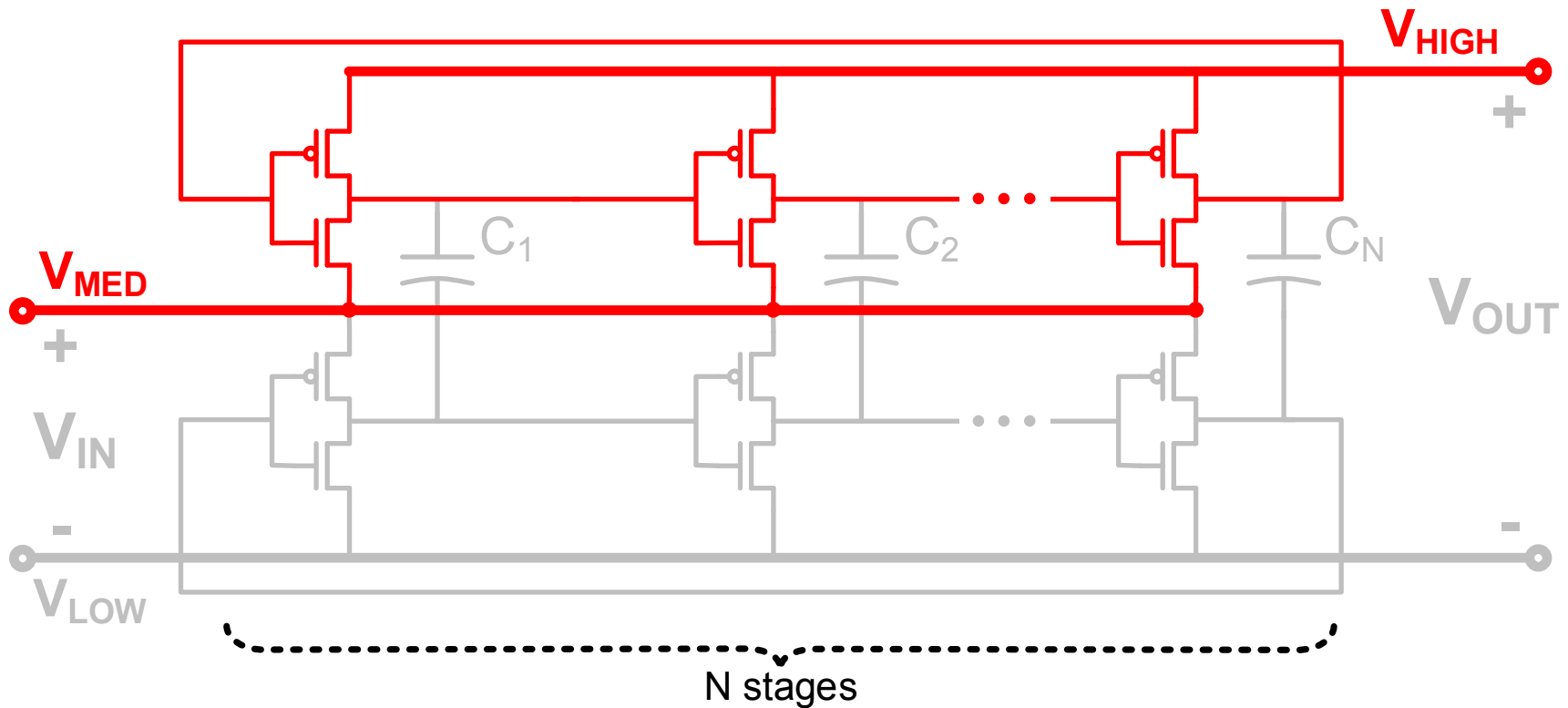
# Self-Oscillating Voltage Doubler

- Bottom ring oscillator operates between  $V_{\text{MED}}$  and  $V_{\text{LOW}}$



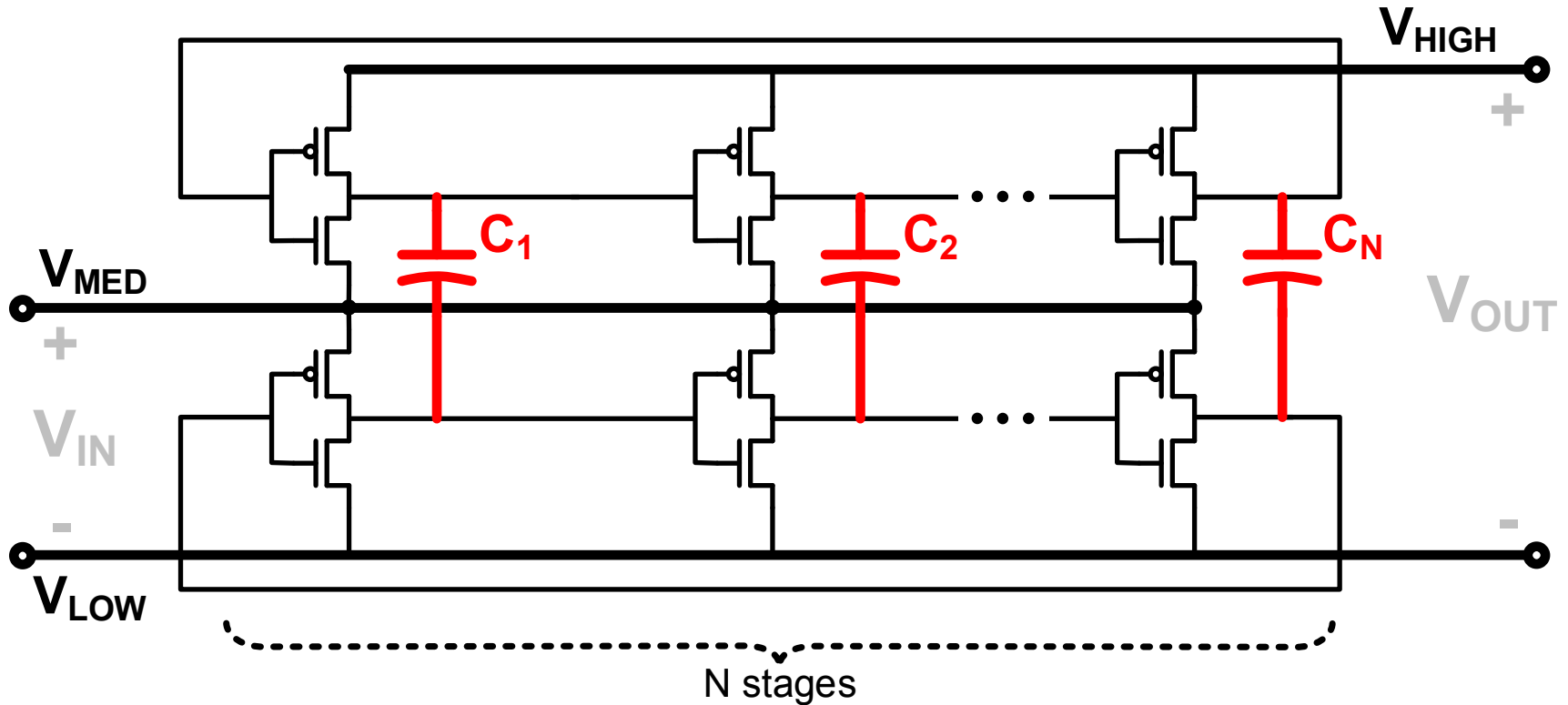
# Self-Oscillating Voltage Doubler

- Top ring oscillator operates between  $V_{\text{HIGH}}$  and  $V_{\text{MED}}$



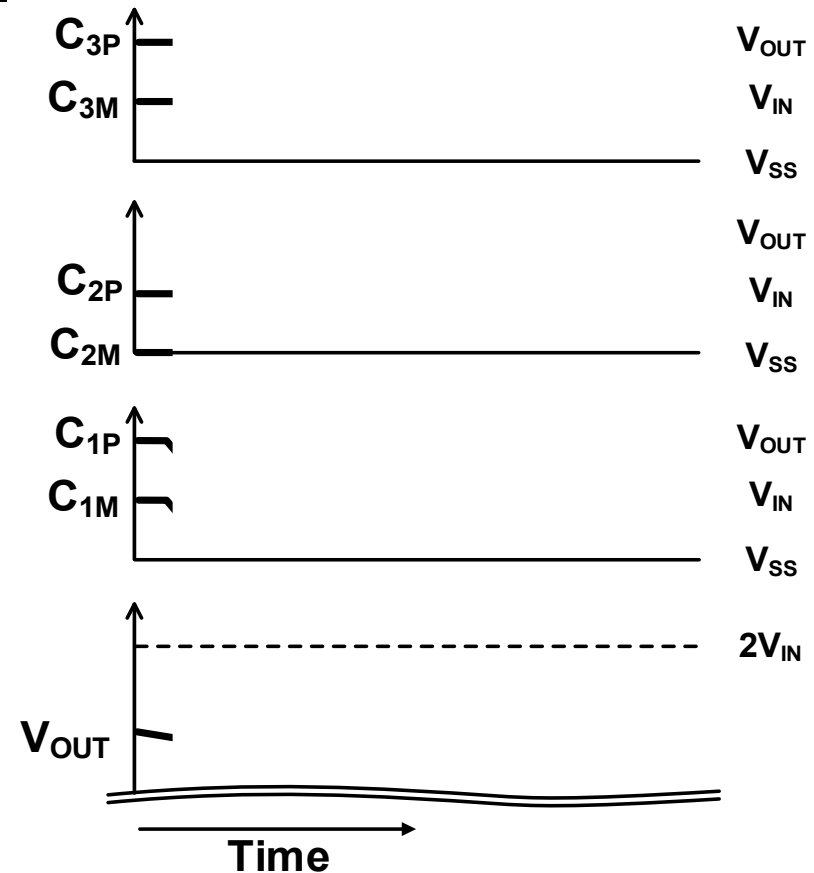
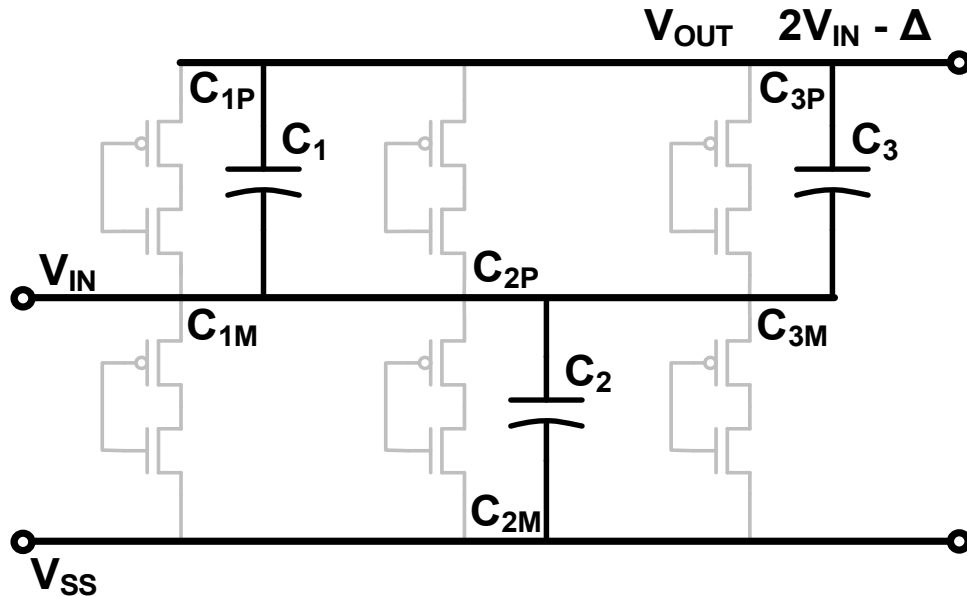
# Self-Oscillating Voltage Doubler

- Top and bottom oscillations are coupled through flying caps
- Two oscillations become matched in clock **amplitude** as well as frequency



# Operation Example (N = 3)

- Simplified operation snapshot
  - Cap connections not shown
  - $C_1$ ,  $C_3$  are at the higher rail
  - $C_2$  is at the lower rail

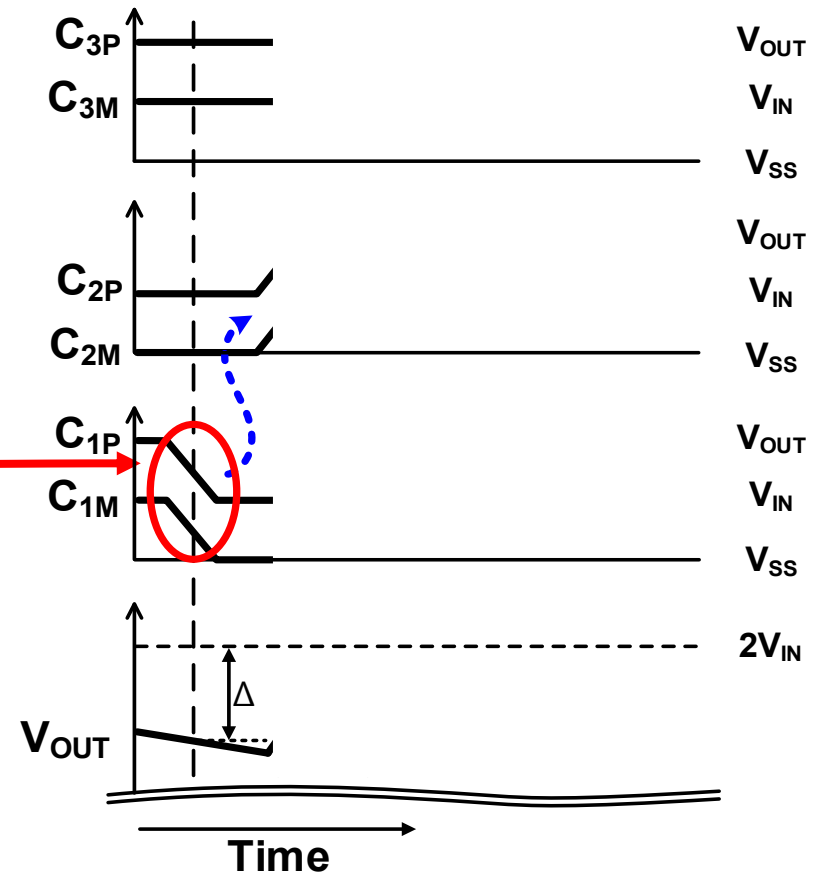
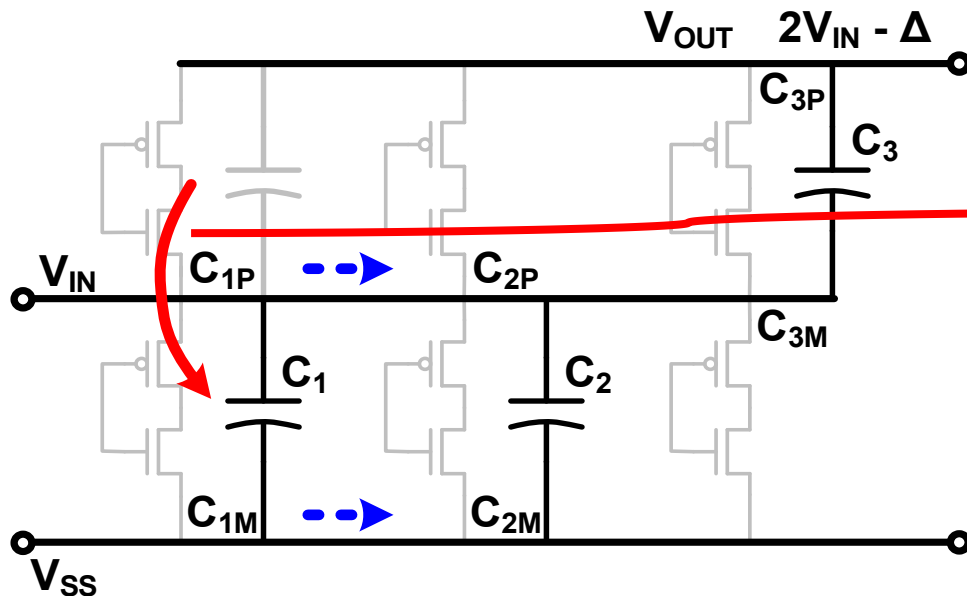


# Operation Example (N = 3)

- $C_1$  is driven low and **charged**

$C_1$ :  $V_{DD} - \Delta \rightarrow V_{DD}$

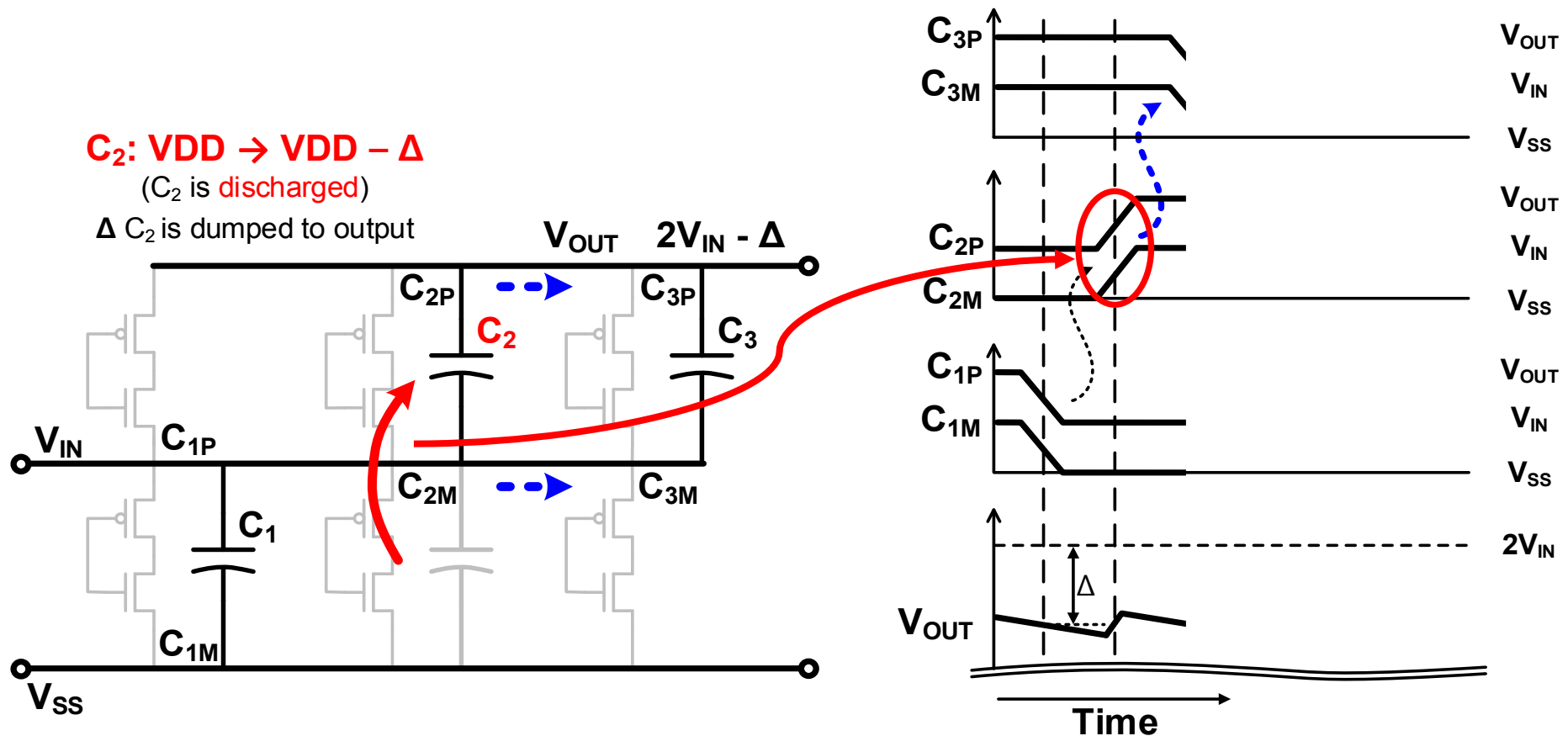
( $C_1$  is **charged**)



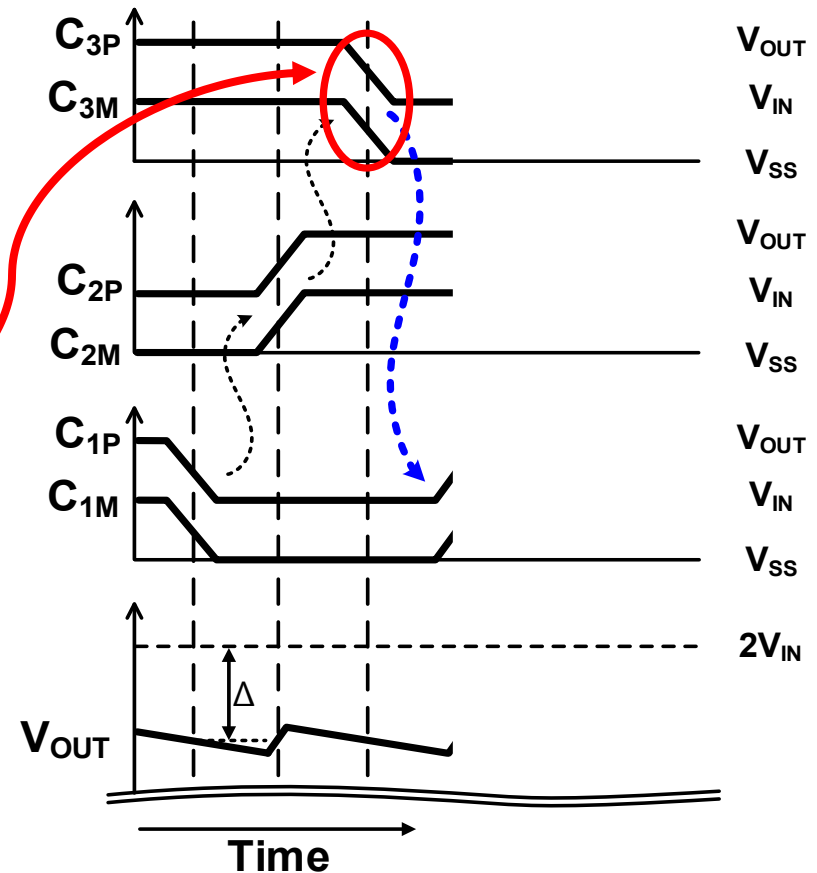


# Operation Example (N = 3)

- $C_2$  is driven high and **discharged**, dumping charge  $\Delta \cdot C_2$  to  $V_{OUT}$



- $C_3$  is driven low and charged



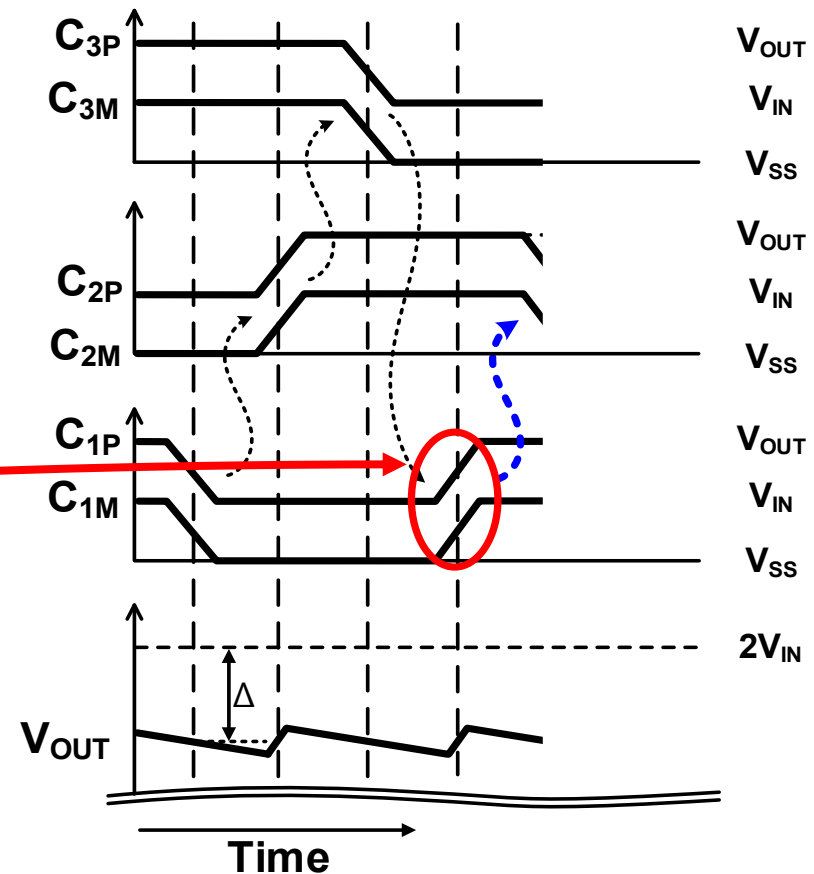
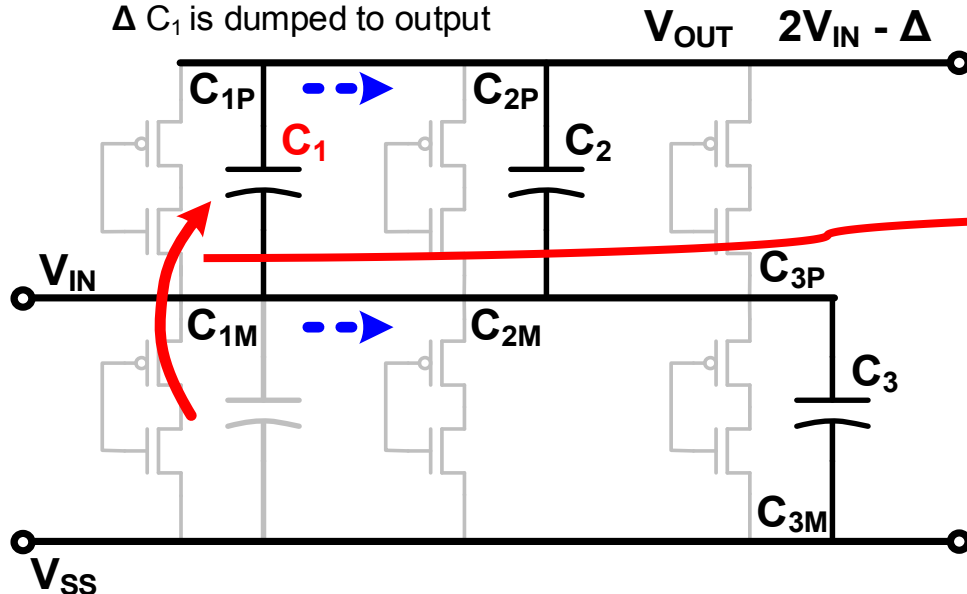
# Operation Example (N = 3)

- $C_1$  is driven high and **discharged**, dumping charge  $\Delta \cdot C_1$  to  $V_{OUT}$

$C_1$ :  $V_{DD} \rightarrow V_{DD} - \Delta$

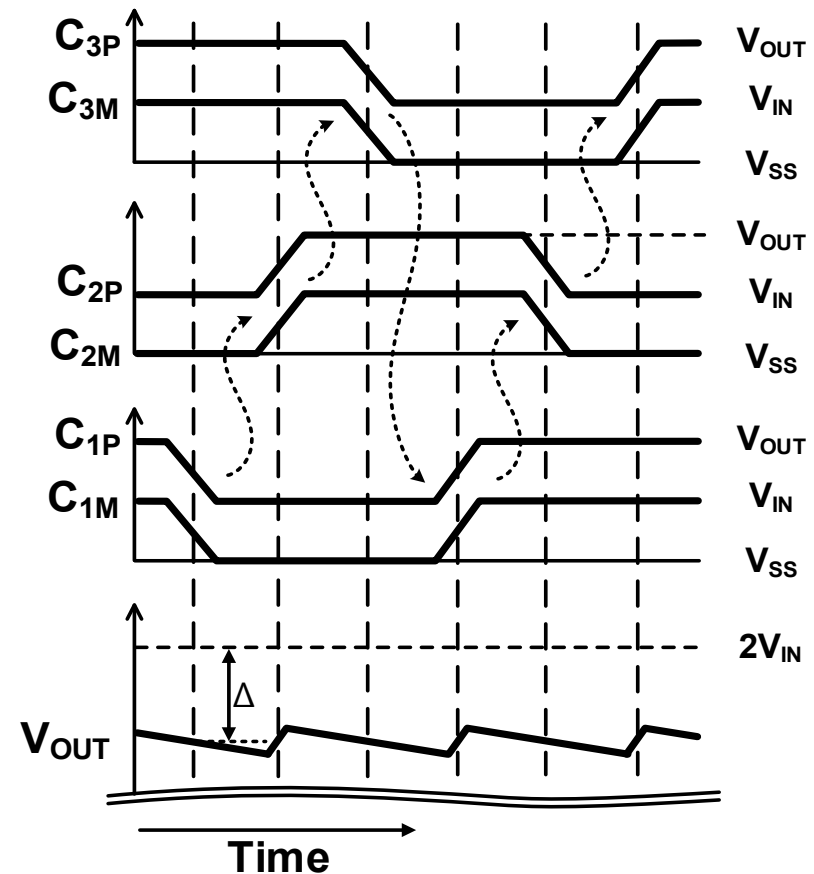
( $C_1$  is **discharged**)

$\Delta C_1$  is dumped to output



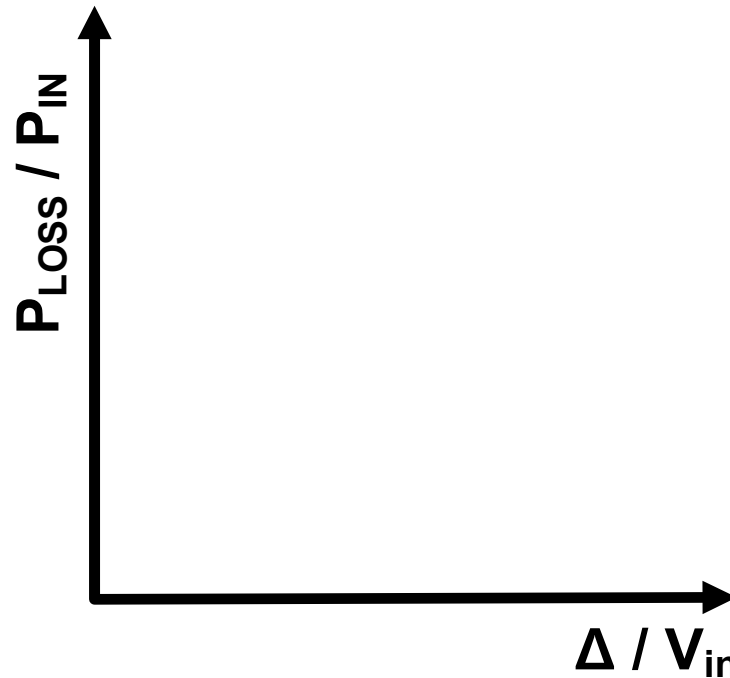
# Self-Oscillating Voltage Doubler

- No overhead for **clock** and **level shifting**
- **Negligible** efficiency loss from **phase mismatch** and **contention loss**
- Naturally multi-phased  
→ **Low  $V_{OUT}$  ripple**
- Capable of **self-startup**



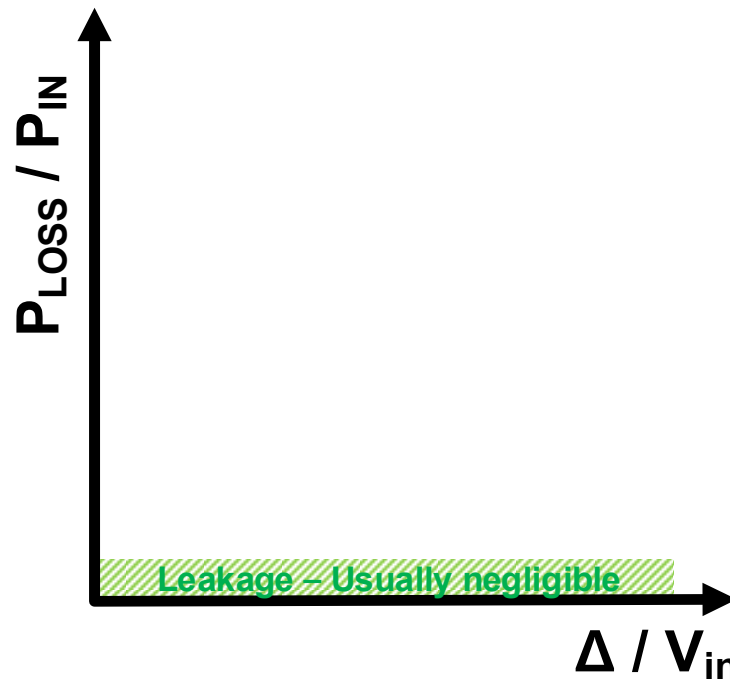
# Doubler Efficiency Optimization

- Efficiency =  $1 - (P_{\text{Loss}} / P_{\text{IN}})$
- Analyze  $P_{\text{Loss}} / P_{\text{IN}}$  in terms of  $\Delta / V_{\text{IN}}$ 
  - $\Delta$  is voltage drop at  $V_{\text{OUT}}$  ( $V_{\text{OUT}} = 2V_{\text{IN}} - \Delta$ )
  - Multi-phase operation makes  $V_{\text{OUT}}$  and  $\Delta$  near DC



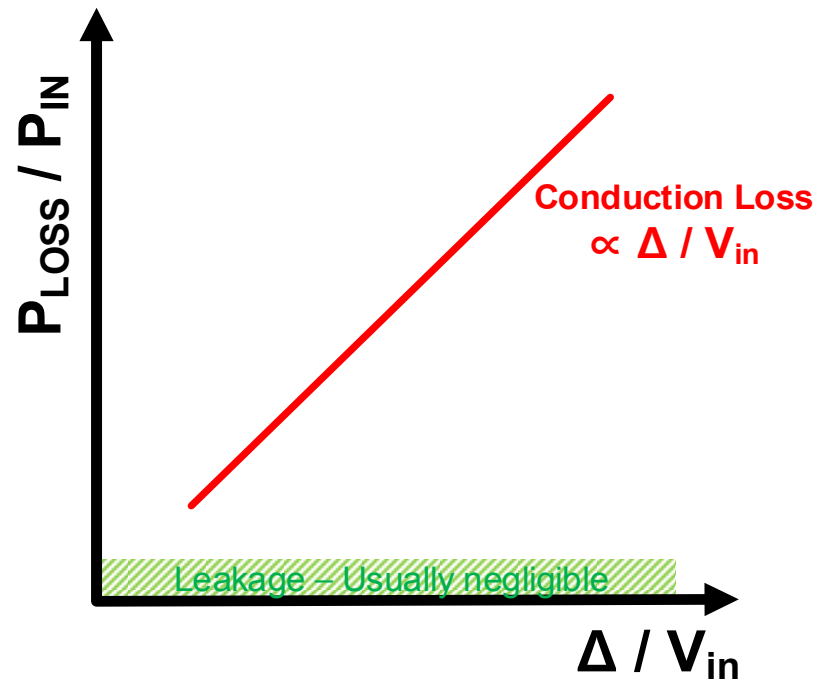
# Doubler Efficiency Optimization

- Total loss  $\approx$  Conduction loss + Switching loss
- Loss from **leakage** is usually **negligible**



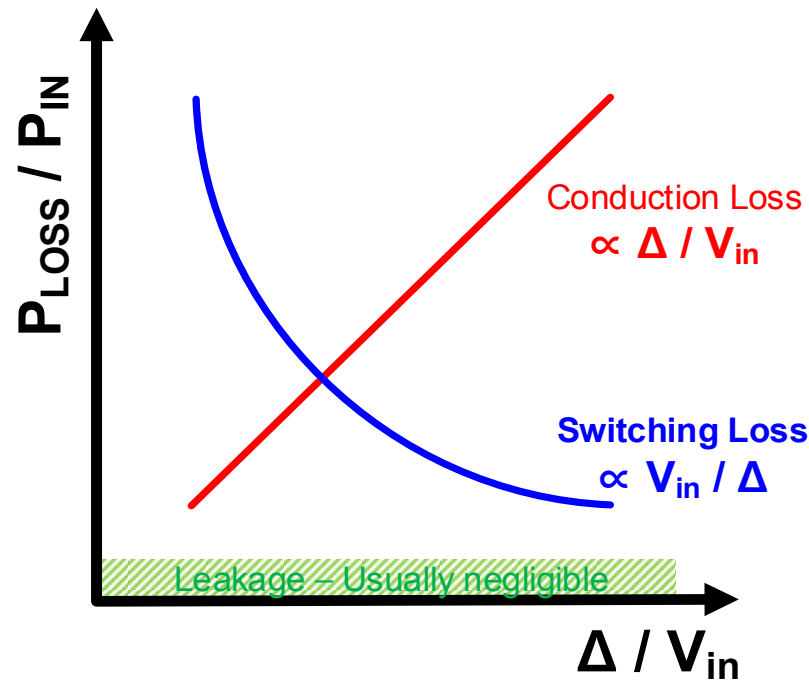
# Doubler Efficiency Optimization

- Total loss  $\approx$  **Conduction loss** + Switching loss
- Conduction loss comes from  $V_{OUT}$  drop
  - $P_{LOSS\_CONDUCTION} / P_{IN} \propto \Delta / V_{IN}$



# Doubler Efficiency Optimization

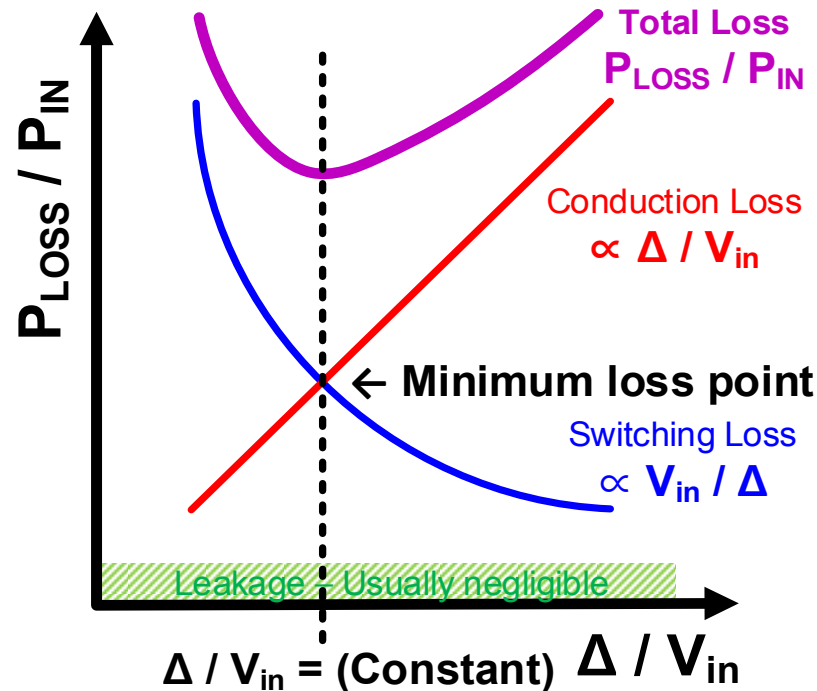
- Total loss  $\approx$  Conduction loss + Switching loss
- Switching loss comes from dynamic power
  - Larger  $\Delta$  increases transferred energy per clock
  - $P_{\text{LOSS\_SWITCHING}} / P_{\text{IN}} \propto V_{\text{IN}} / \Delta$





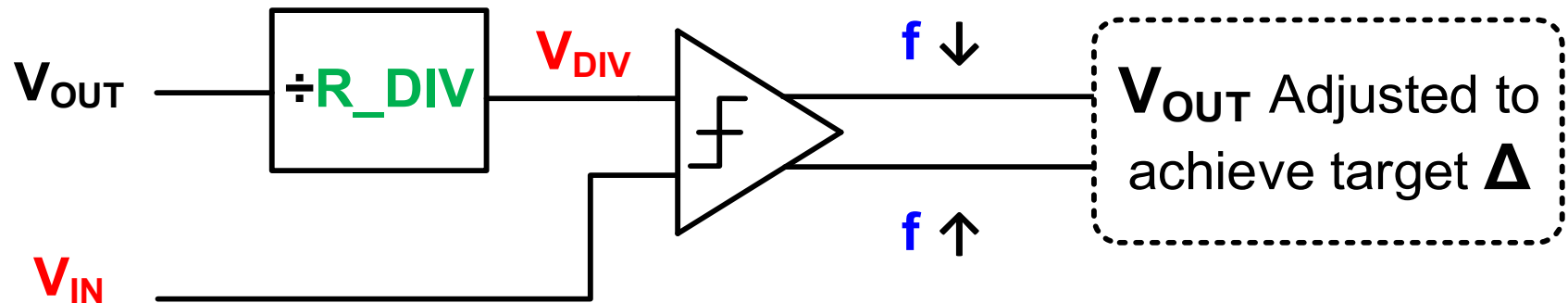
# Doubler Efficiency Optimization

- Total loss  $\approx$  Conduction loss + Switching loss
- At minimum loss point,  $\Delta / V_{IN}$  is at fixed point
  - Independent of  $V_{IN}$ , Frequency, Load current

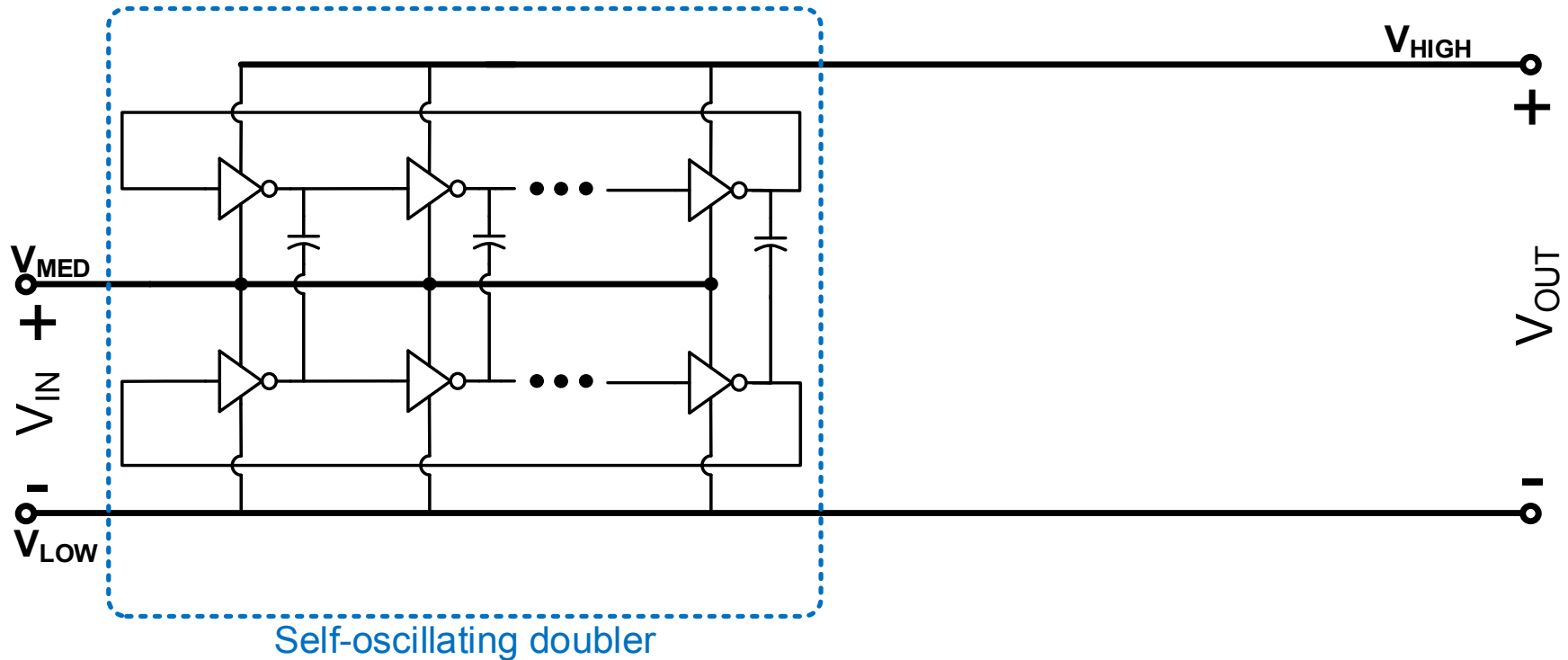


# Frequency Modulation for Optimum $\Delta$

- For desired  $\Delta / V_{IN}$ ,  $V_{OUT}$  is compared to  $V_{IN}$   
 $\Delta = 2V_{IN} - V_{OUT}$ ,  
 $V_{IN} = V_{OUT} / (2 - \Delta / V_{IN}) = V_{OUT} / R\_DIV$
- Feedback control of oscillation frequency to keep  $V_{DIV} = V_{OUT} / R\_DIV$  at the same level as  $V_{IN}$

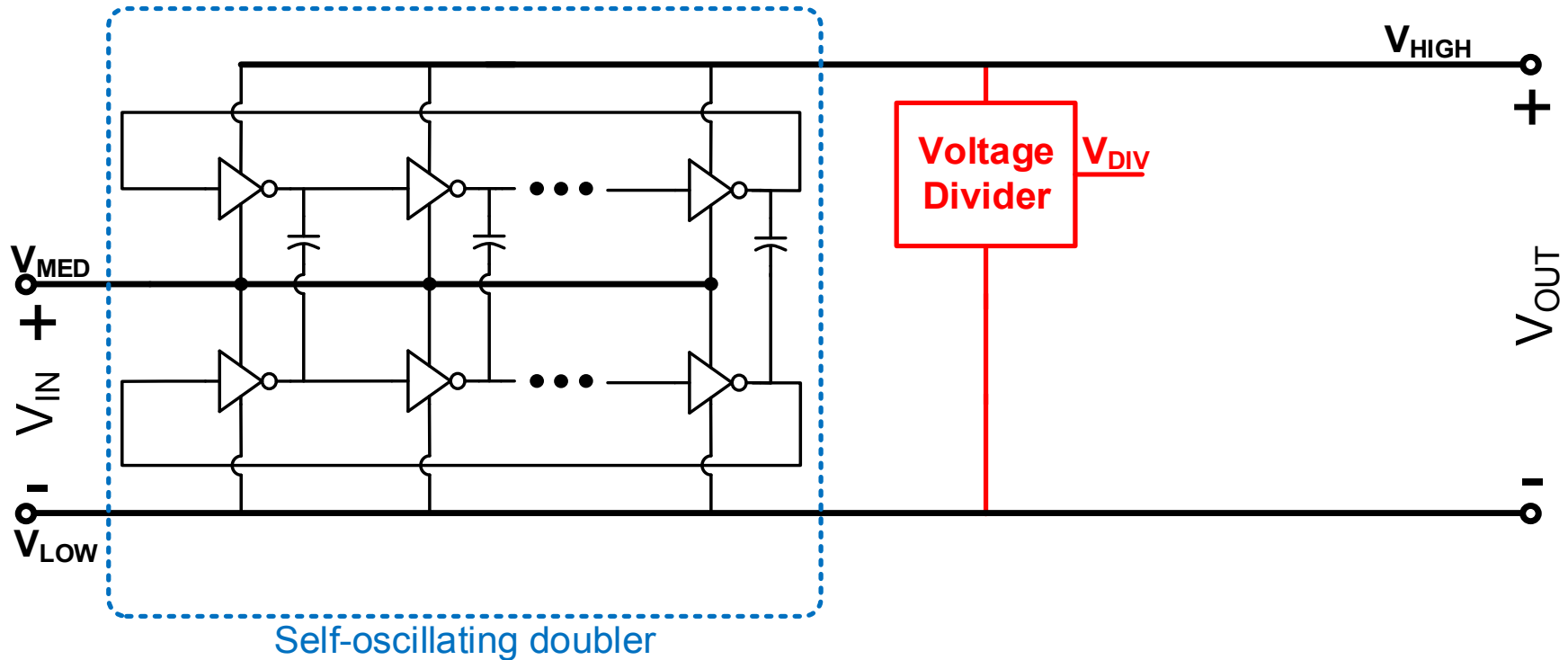


# Frequency Modulation for Optimum $\Delta$



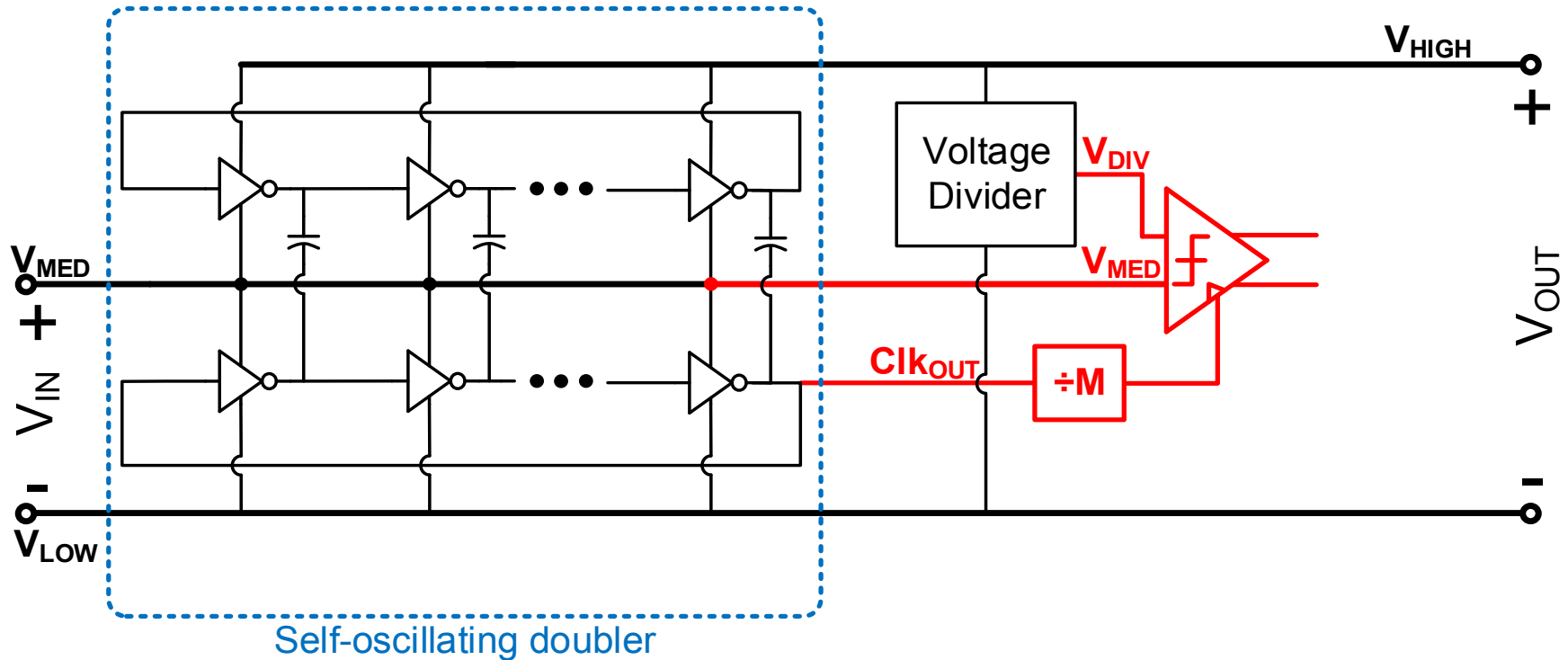
# Frequency Modulation for Optimum $\Delta$

- $V_{\text{DIV}} = V_{\text{OUT}} / R_{\text{DIV}}$       ( $R_{\text{DIV}} \equiv 2 - \Delta / V_{\text{IN}}$ )



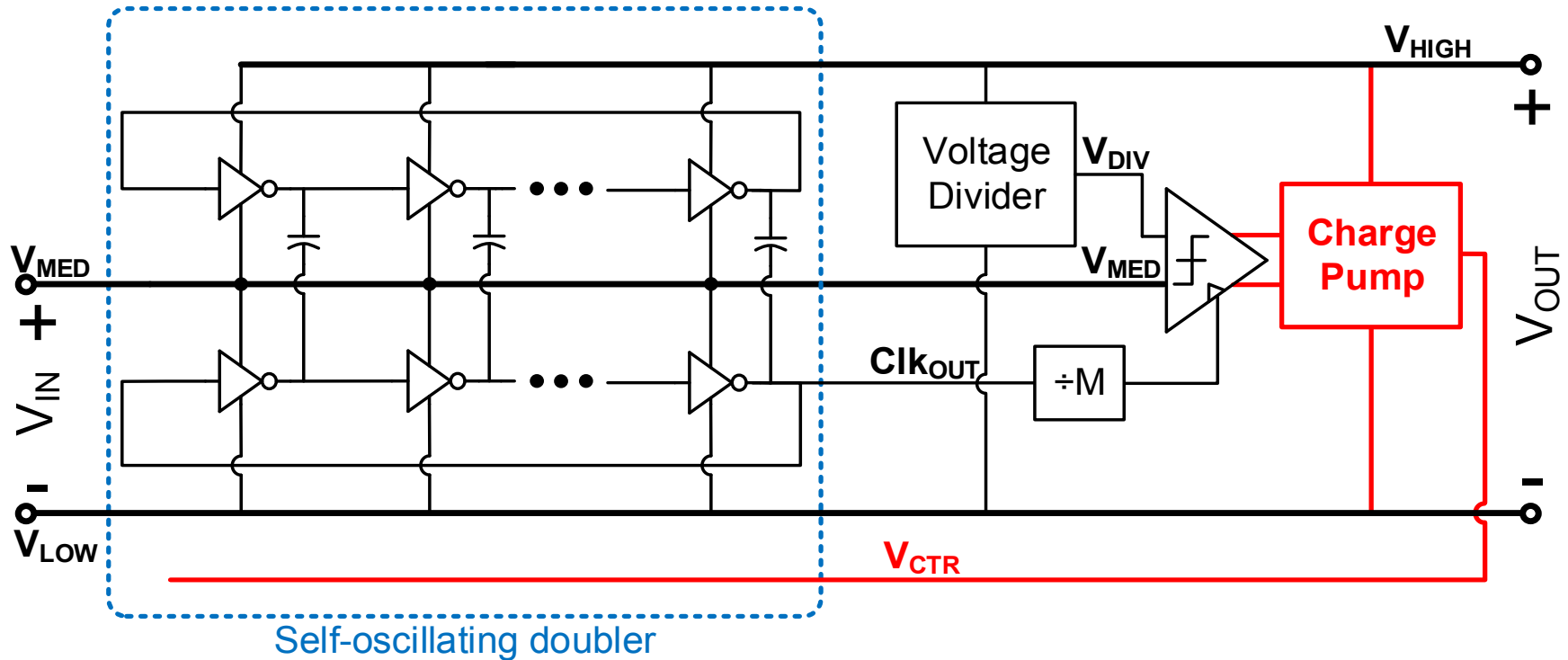
# Frequency Modulation for Optimum $\Delta$

- $V_{DIV} = V_{OUT} / R_{DIV}$  ( $R_{DIV} \equiv 2 - \Delta / V_{IN}$ )
- $V_{DIV}$  is periodically compared to  $V_{IN}$



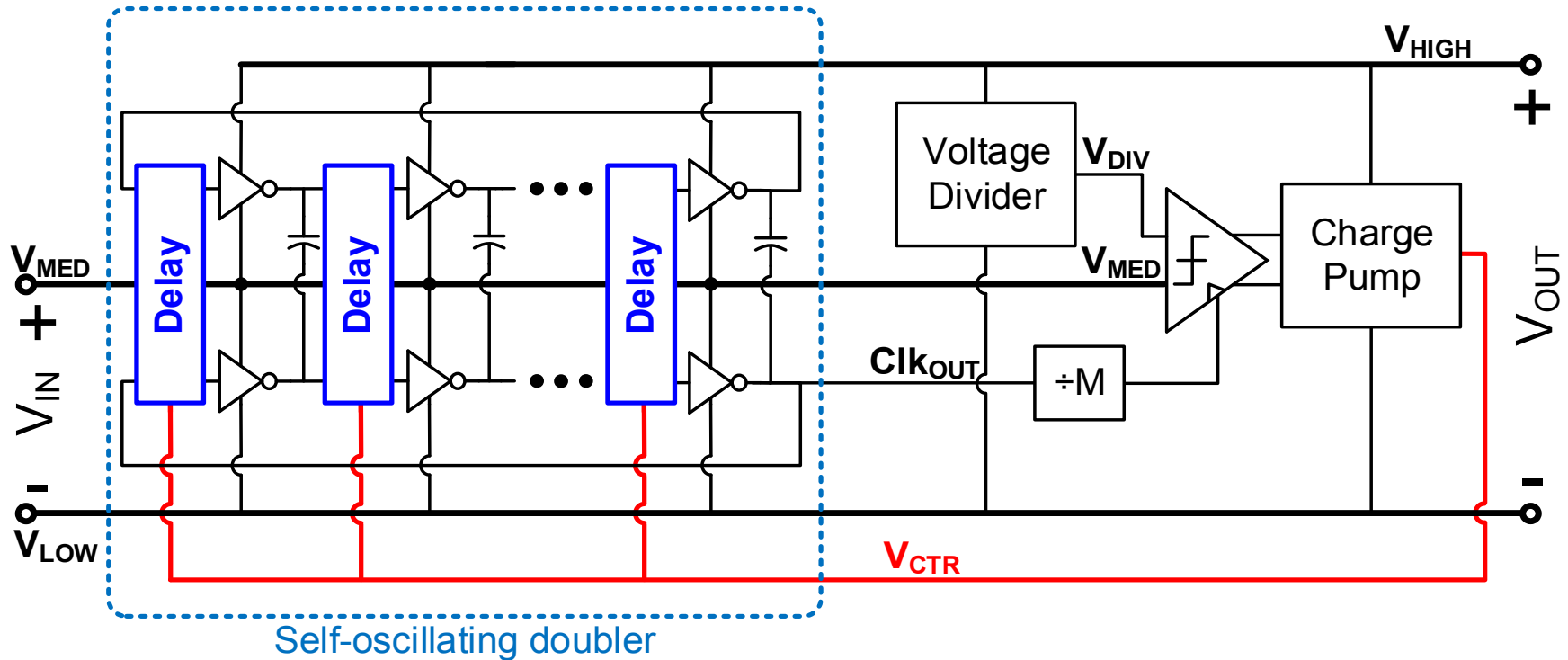
# Frequency Modulation for Optimum $\Delta$

- $V_{DIV} = V_{OUT} / R_{DIV}$  ( $R_{DIV} \equiv 2 - \Delta / V_{IN}$ )
- $V_{DIV}$  is periodically compared to  $V_{IN}$  to adjust  $V_{CTR}$



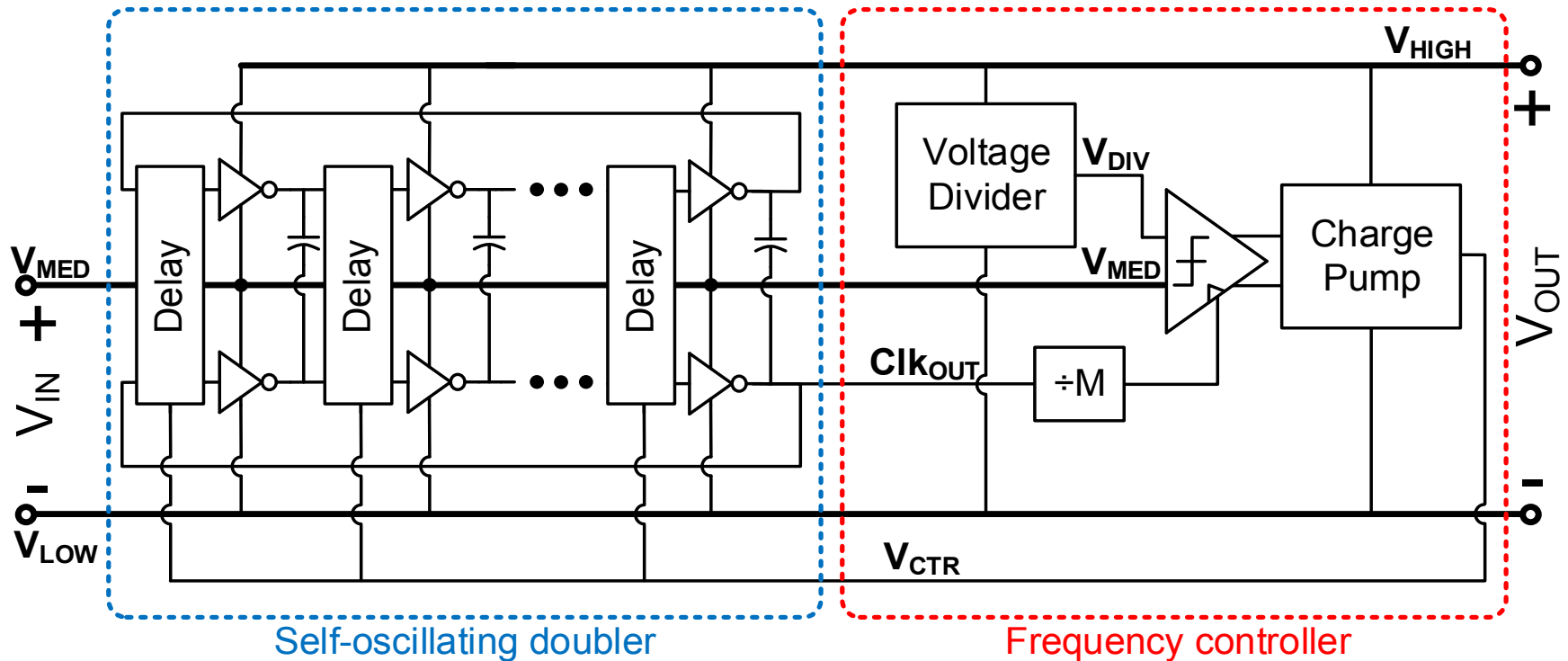
# Frequency Modulation for Optimum $\Delta$

- $V_{DIV} = V_{OUT} / R_{DIV}$  ( $R_{DIV} \equiv 2 - \Delta / V_{IN}$ )
- $V_{DIV}$  is periodically compared to  $V_{IN}$  to adjust  $V_{CTR}$
- Feedback control of **stage delay** through  $V_{CTR}$



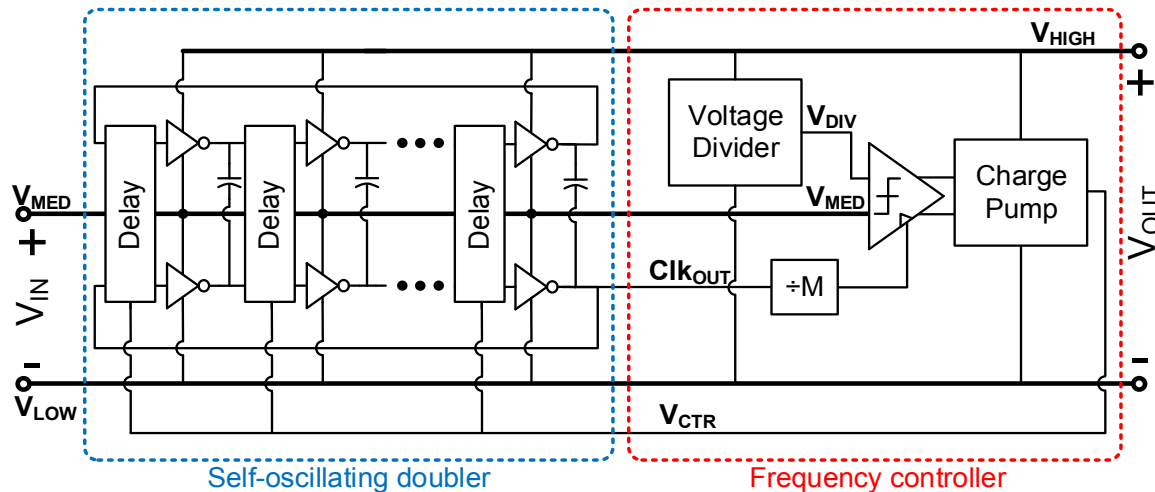
# Frequency Modulation for Optimum $\Delta$

- Oscillator operates regardless of initial  $V_{CTR}$  value
  - Capable of **self-startup**
- $V_{CTR}$  goes to minimum when input power unavailable
  - **Low idle power** consumption at output



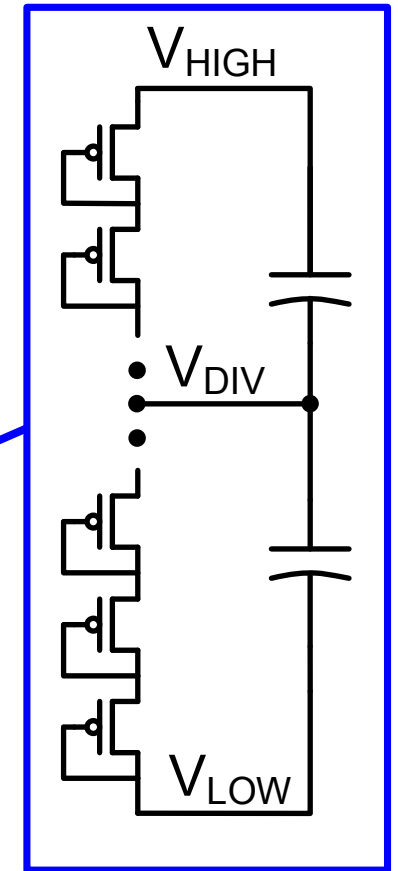
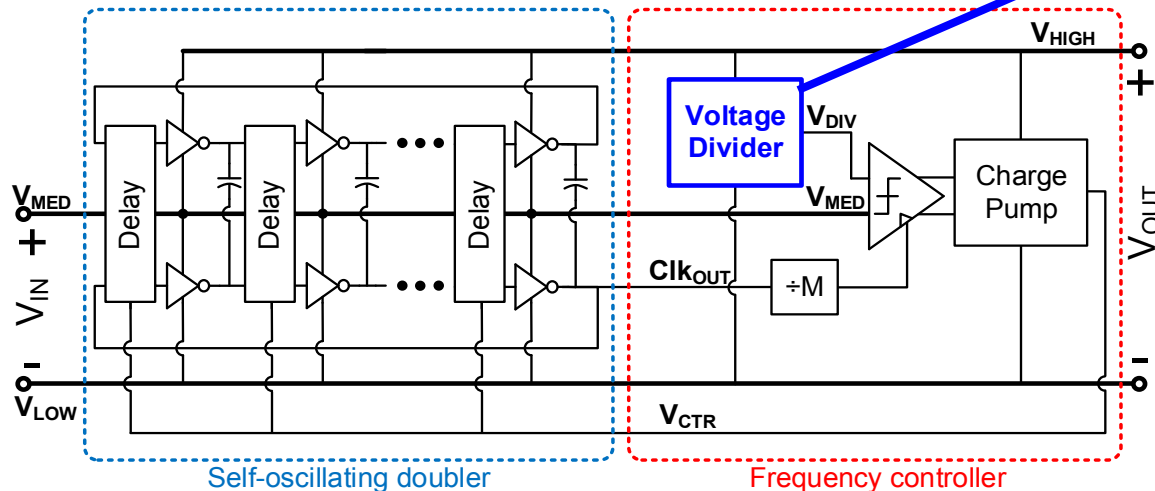


# Blocks for Frequency Modulation



# Blocks for Frequency Modulation

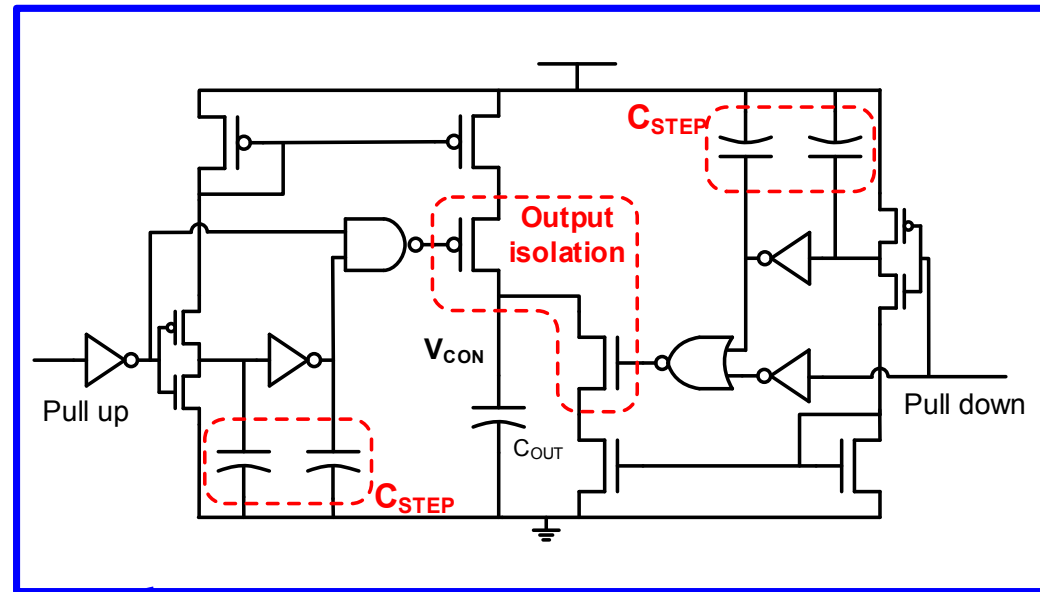
- Voltage divider
  - Slow diode stack for DC division
  - Fast capacitive voltage division



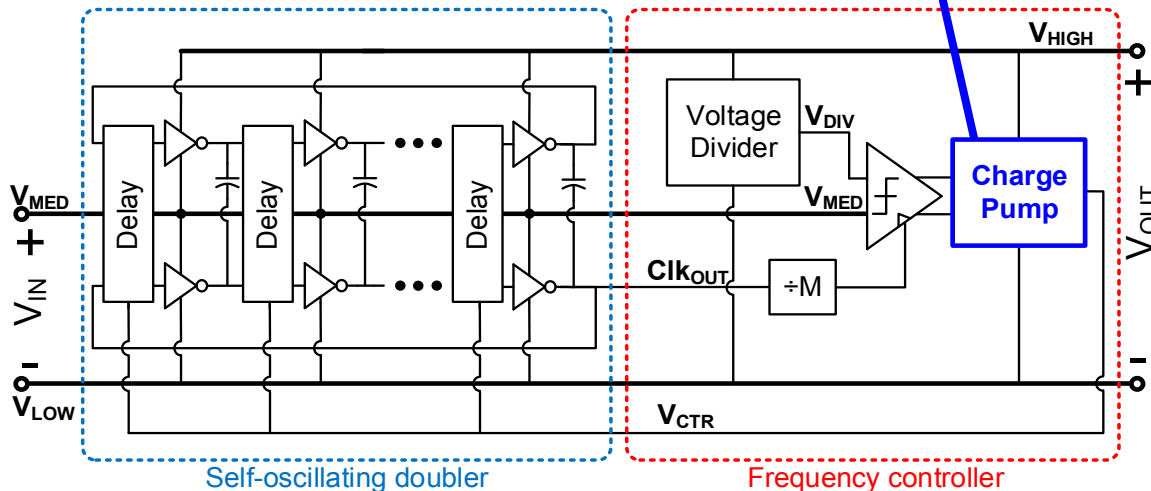
**Voltage divider**

# Blocks for Frequency Modulation

- Charge pump
  - $C_{STEP}$  determines the amount of charge flow per cycle
  - Output is isolated when idle to sustain  $V_{CTR}$  for long period

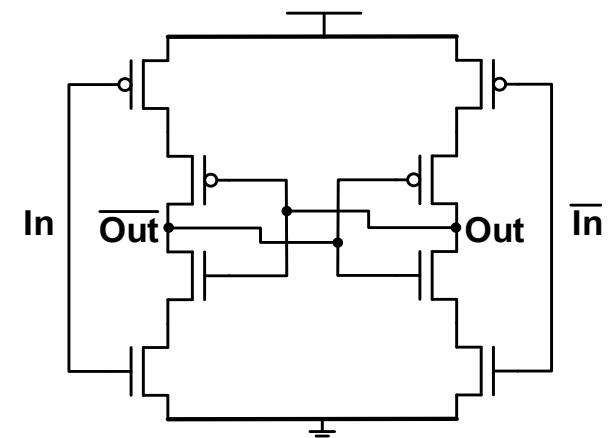
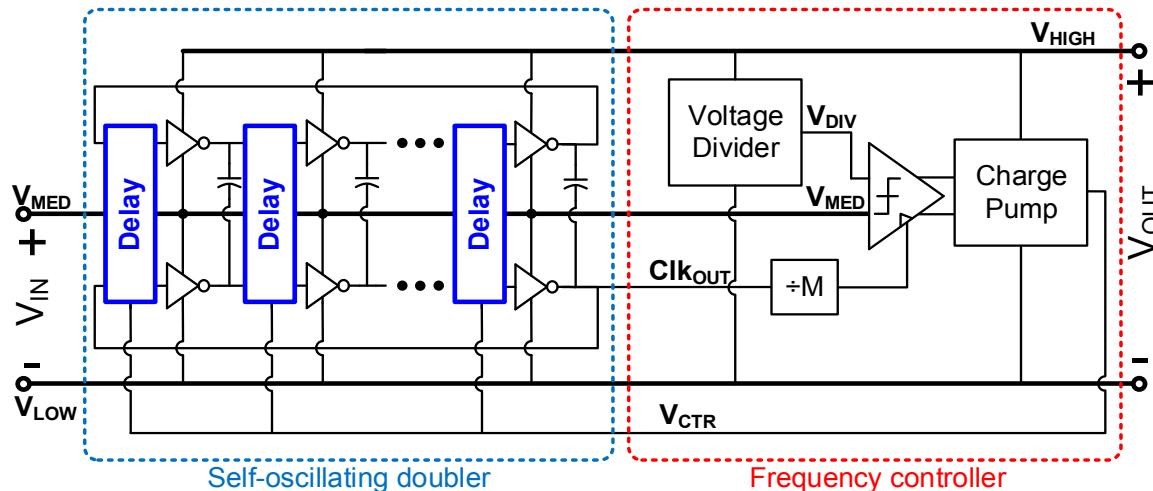


Charge pump



# Blocks for Frequency Modulation

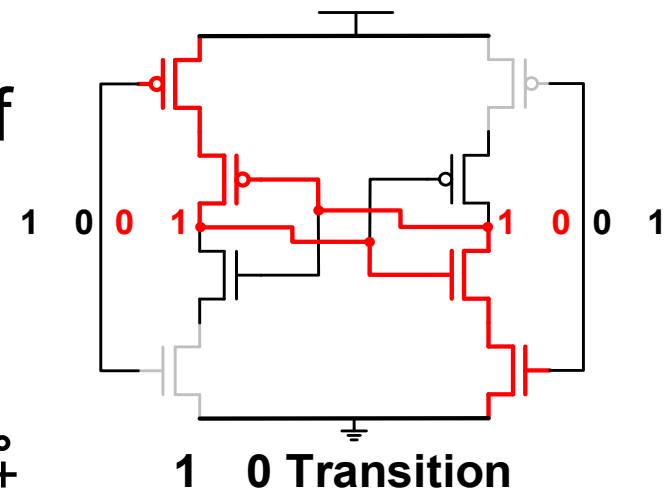
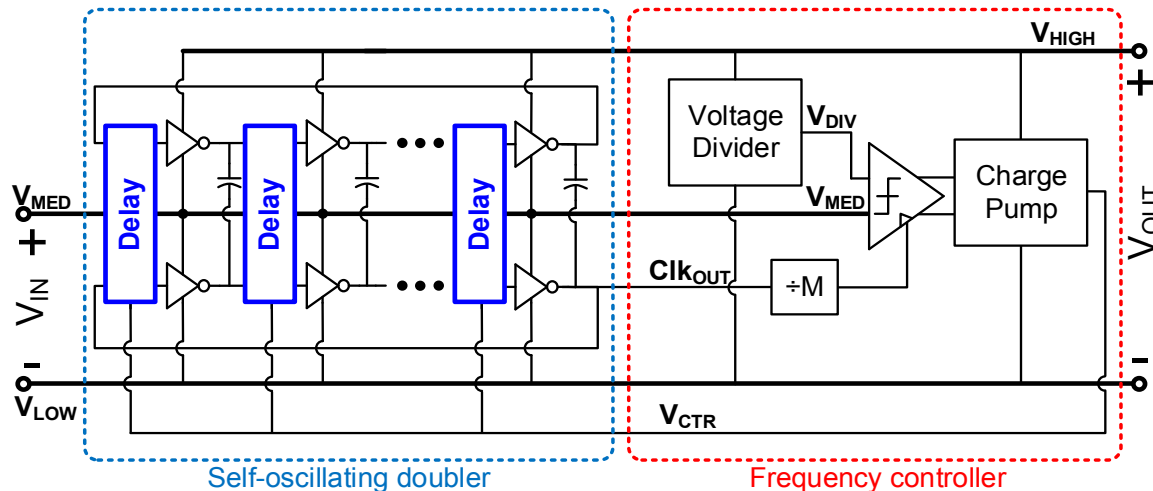
- Voltage controlled synchronized delay
  - Leakage-based delay element provides long delay with low energy consumption
- [G. Chen, ISSCC 2010]



Leakage-based delay element  
[G. Chen, ISSCC 2010]

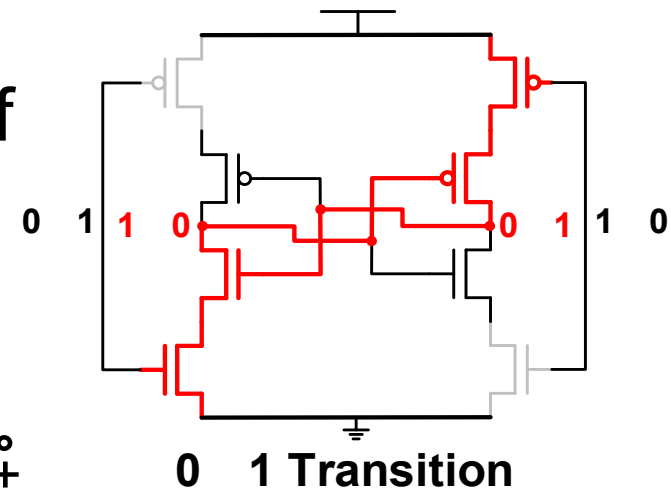
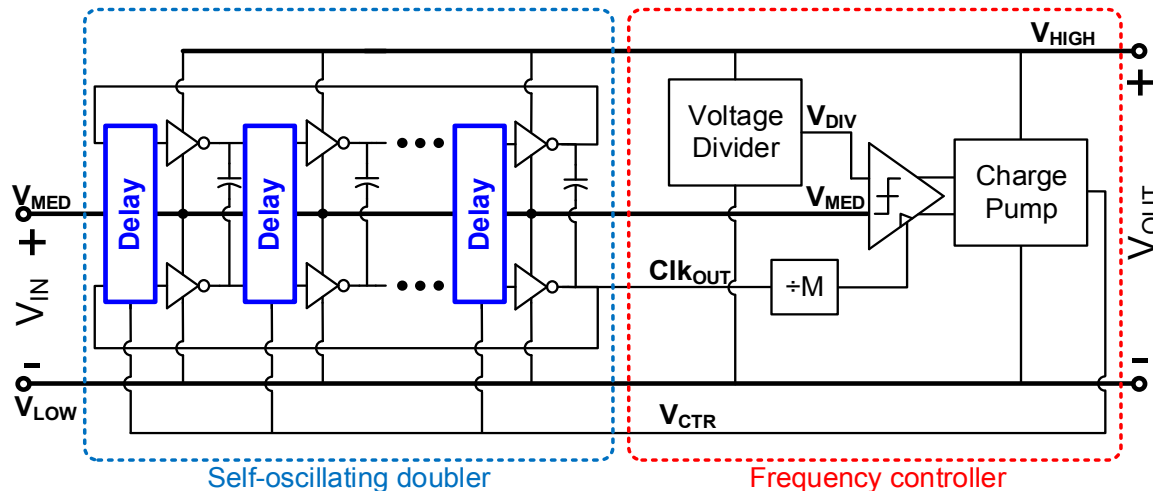
# Blocks for Frequency Modulation

- Voltage controlled synchronized delay
- Leakage-based delay element provides long delay with low energy consumption  
[G. Chen, ISSCC 2010]
- Isolation transistors are turned off to operate it as a 2-way thyristor, providing long, sharp delay



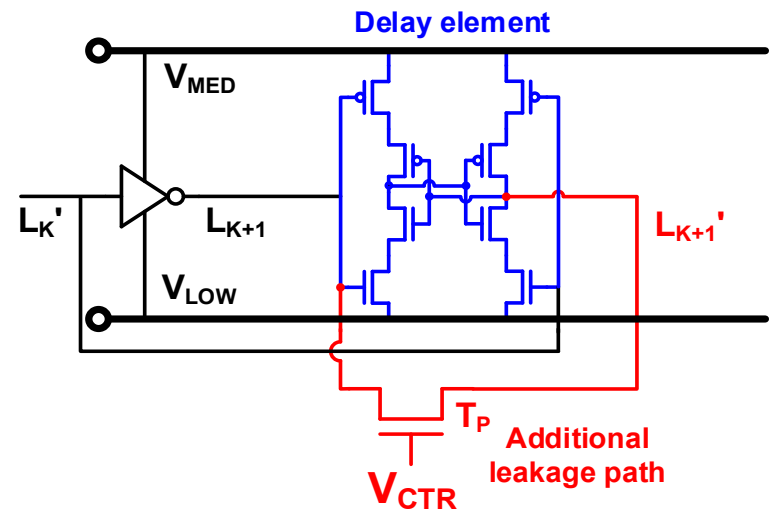
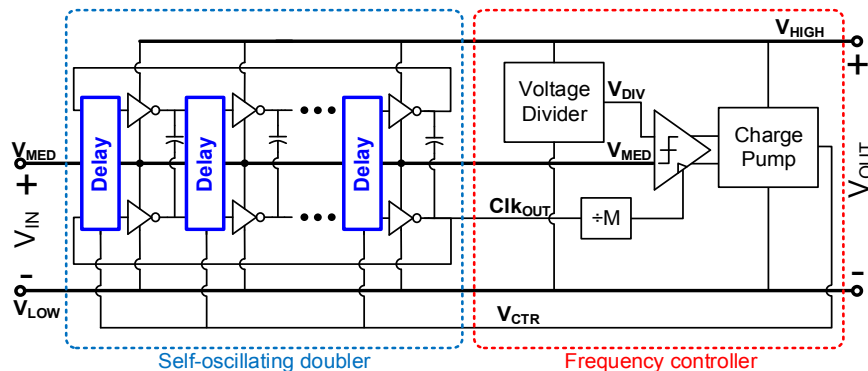
# Blocks for Frequency Modulation

- Voltage controlled synchronized delay
- Leakage-based delay element provides long delay with low energy consumption  
[G. Chen, ISSCC 2010]
- Isolation transistors are turned off to operate it as a 2-way thyristor, providing long, sharp delay



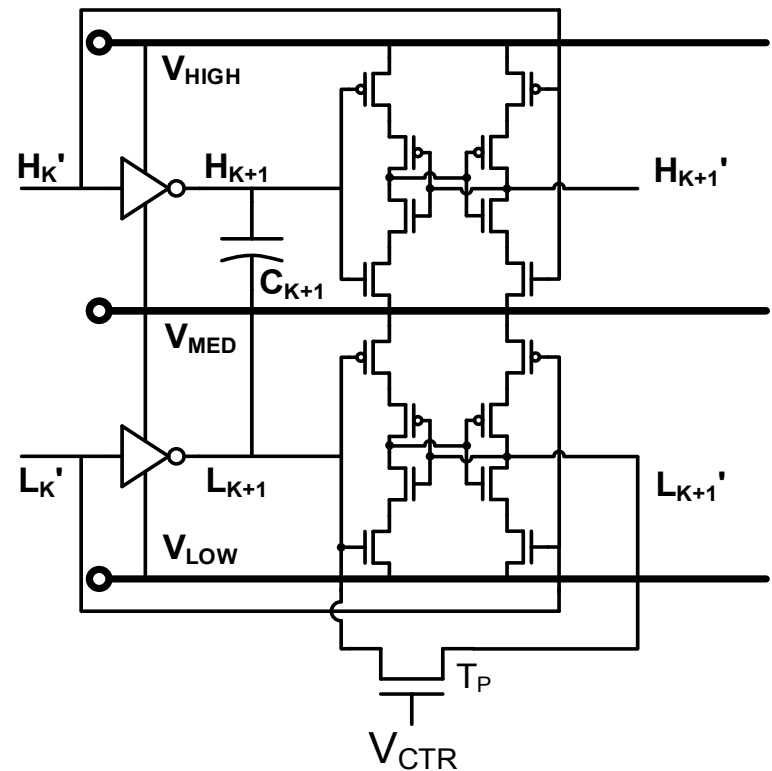
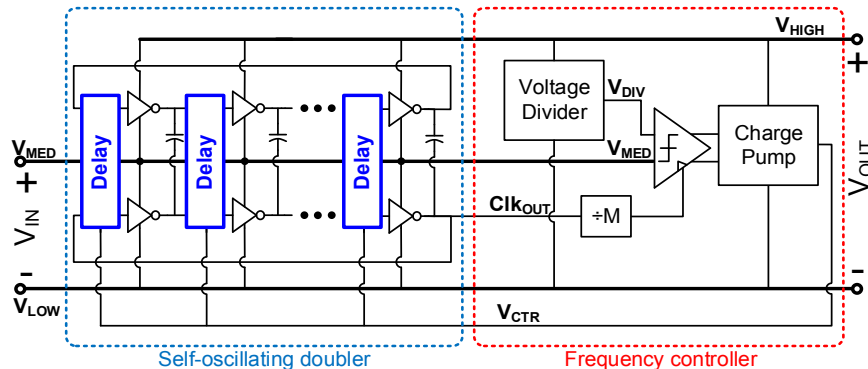
# Blocks for Frequency Modulation

- Voltage controlled synchronized delay
  - Leakage-based delay element provides long delay
- Pass transistor controlled by  $V_{CTR}$  provides additional leakage path to output, controlling delay



# Blocks for Frequency Modulation

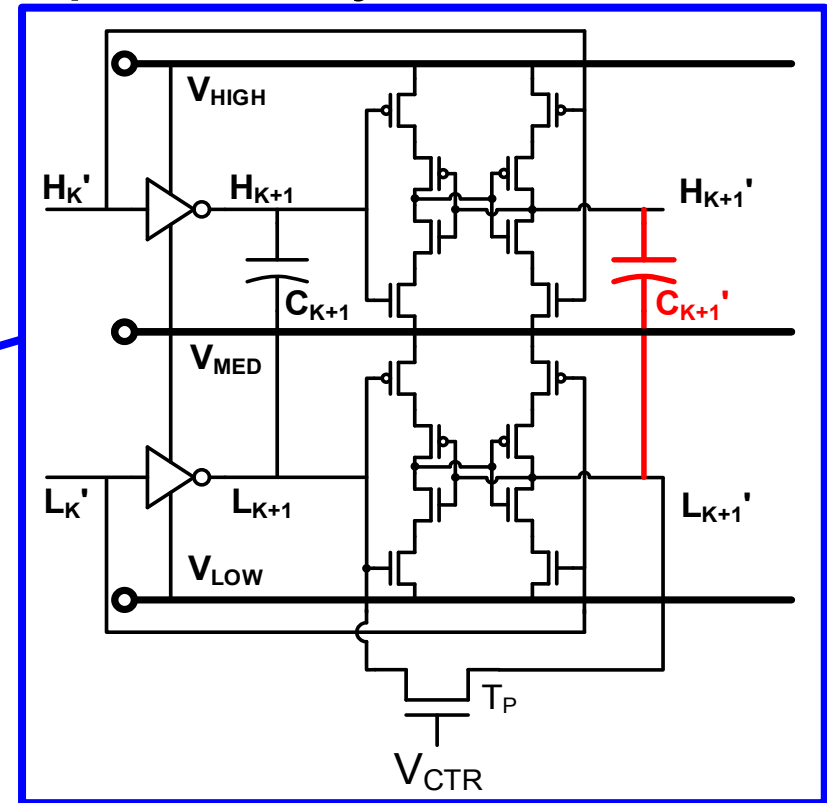
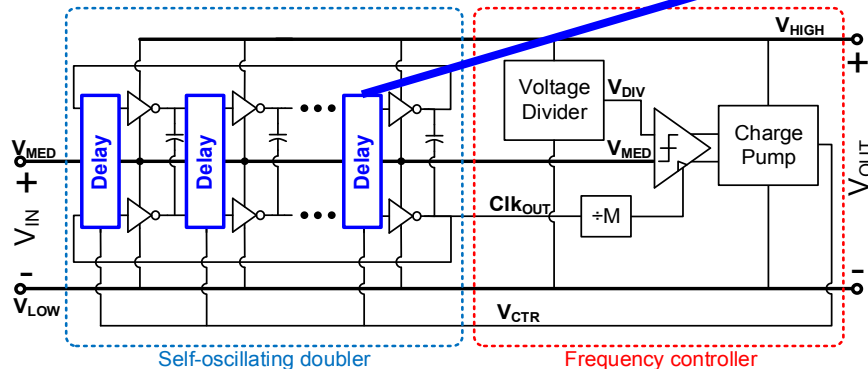
- Voltage controlled synchronized delay
  - Leakage-based delay element provides long delay
  - Delay is controlled by  $V_{CTR}$
- Top oscillation is also delayed





# Blocks for Frequency Modulation

- Voltage controlled synchronized delay
  - Leakage-based delay element provides long delay
  - Delay is controlled by  $V_{CTR}$
- Delayed output nodes are coupled to synchronize delays of two oscillations

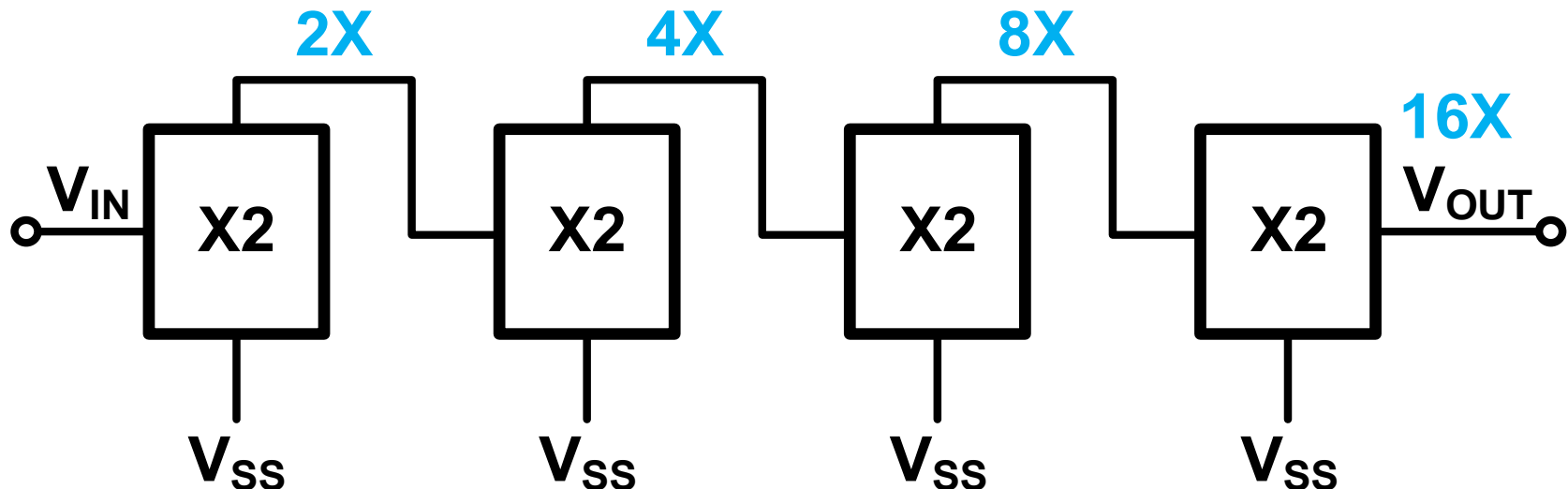


# Achieving Higher Conversion Ratios

- Cascading voltage doublers
  - Each doubler oscillates in its own clock domain to maintain optimum efficiency
  - Base conversion ratio:  $2^N$

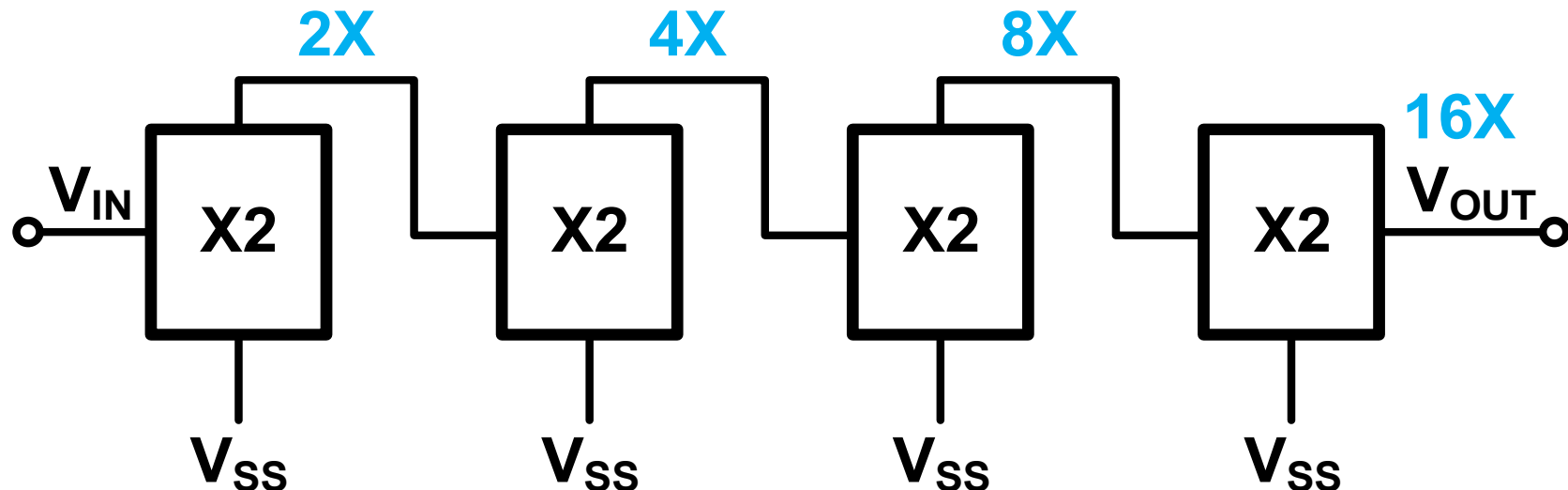
# Achieving higher ratios

- Cascading voltage doublers
  - Each doubler oscillates in its own clock domain to maintain optimum efficiency
  - Base conversion ratio:  $2^N$
  - Example: 4 stages –  $2^4 = 16X$  base ratio



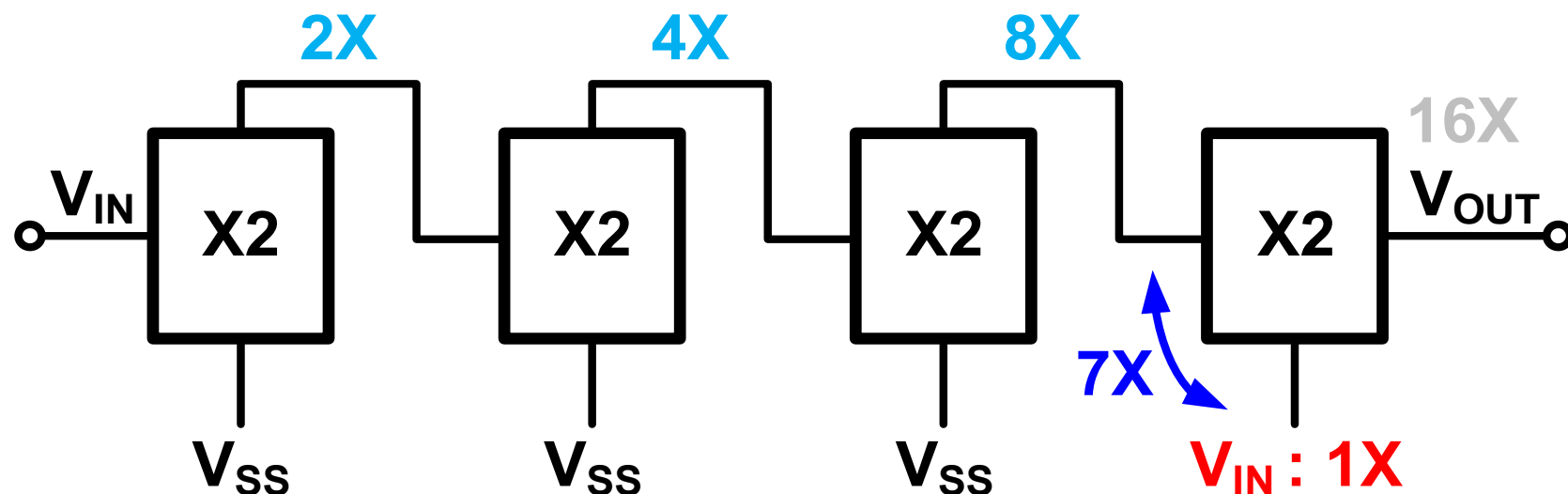
# Achieving Higher Conversion Ratios

- Bottom voltage modulation
  - Modifying bottom voltage changes  $V_{OUT}$



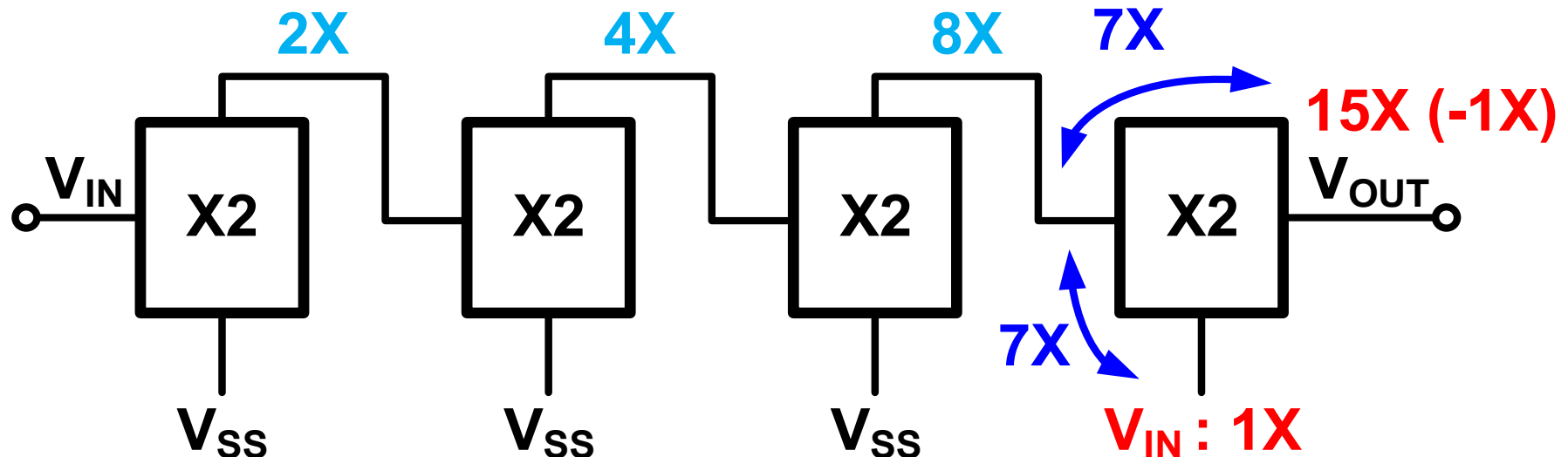
# Achieving Higher Conversion Ratios

- Bottom voltage modulation
  - Modifying bottom voltage changes  $V_{OUT}$
  - Example:  $V_{SS} \rightarrow V_{IN}$  at Final stage



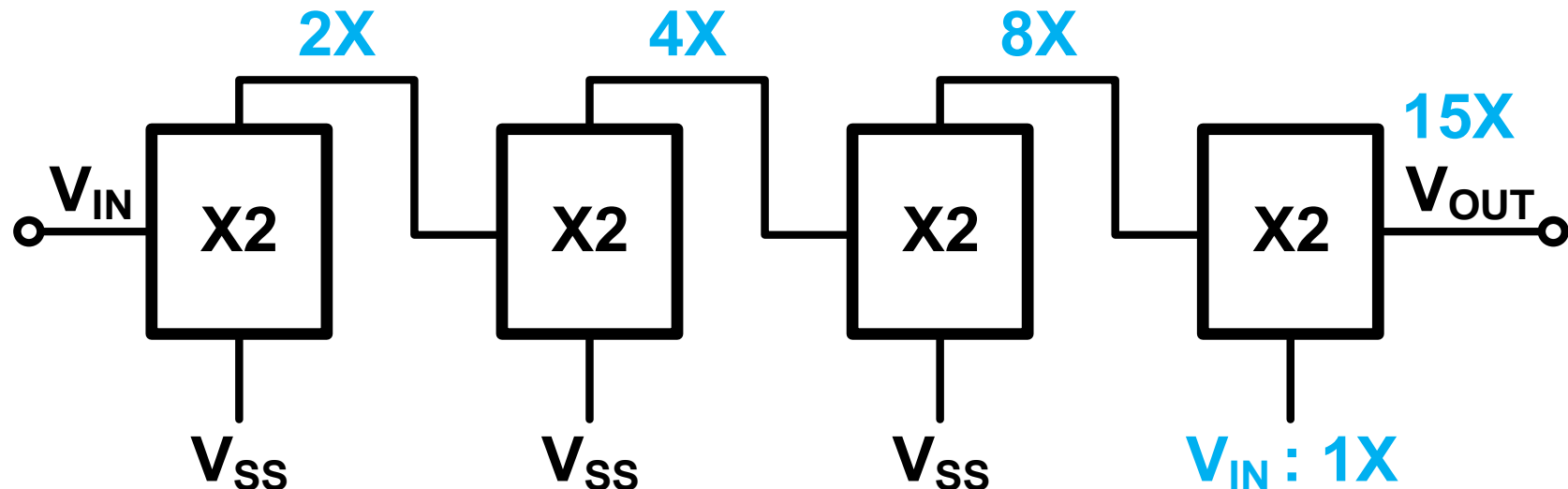
# Achieving Higher Conversion Ratios

- Bottom voltage modulation
  - Modifying bottom voltage changes  $V_{OUT}$
  - Example:  $V_{SS} \rightarrow V_{IN}$  at Final stage  $\rightarrow$  **15X (-1X)**
  - $V_{OUT} = V_{BOT} + 2(V_{IN} - V_{BOT}) = \mathbf{2V_{IN} - V_{BOT}}$



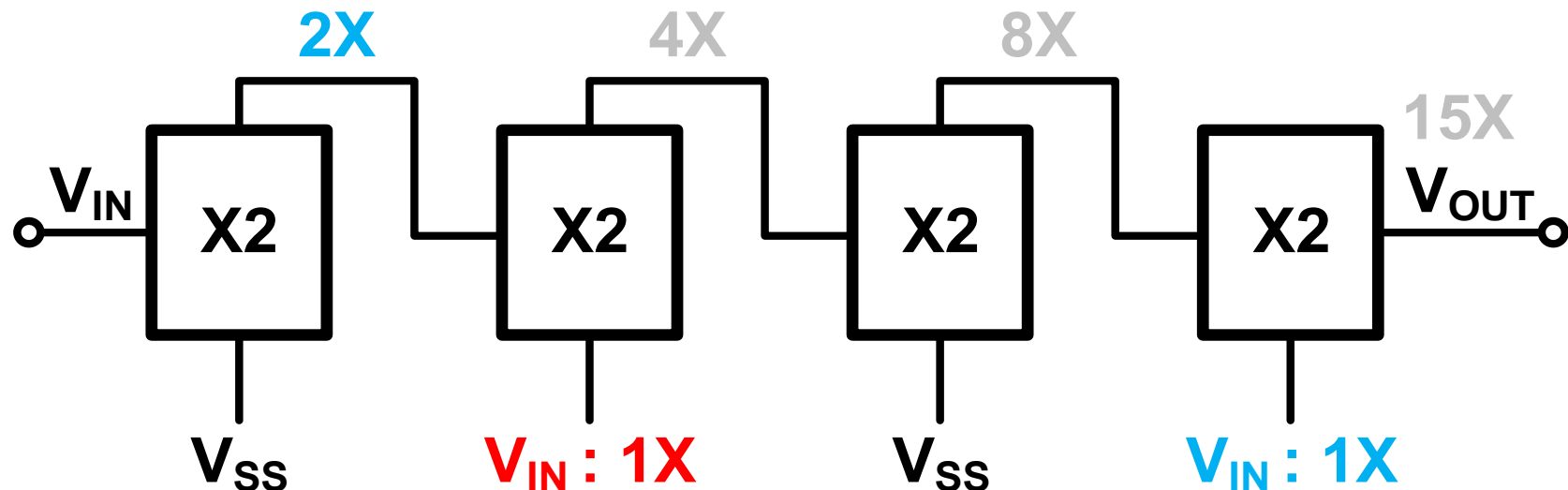
# Achieving Higher Conversion Ratios

- Bottom voltage modulation
  - Earlier stage has greater effect on ratio



# Achieving Higher Conversion Ratios

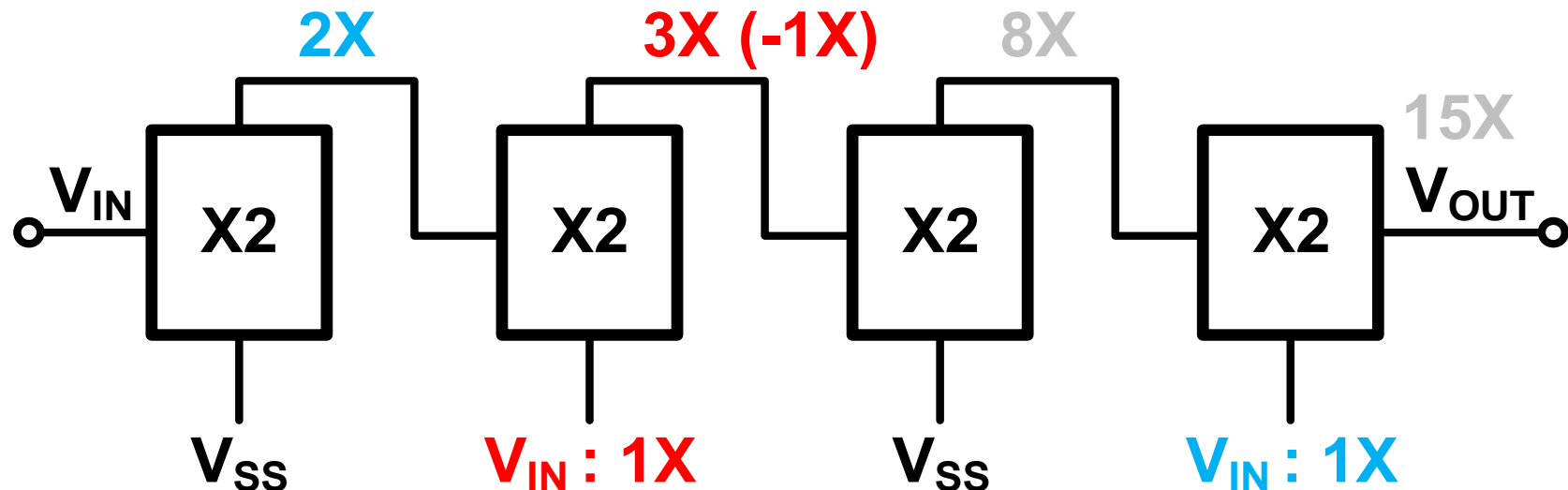
- Bottom voltage modulation
  - Earlier stage has greater effect on ratio
  - Example:  $V_{SS} \rightarrow V_{IN}$  at 2<sup>nd</sup> stage





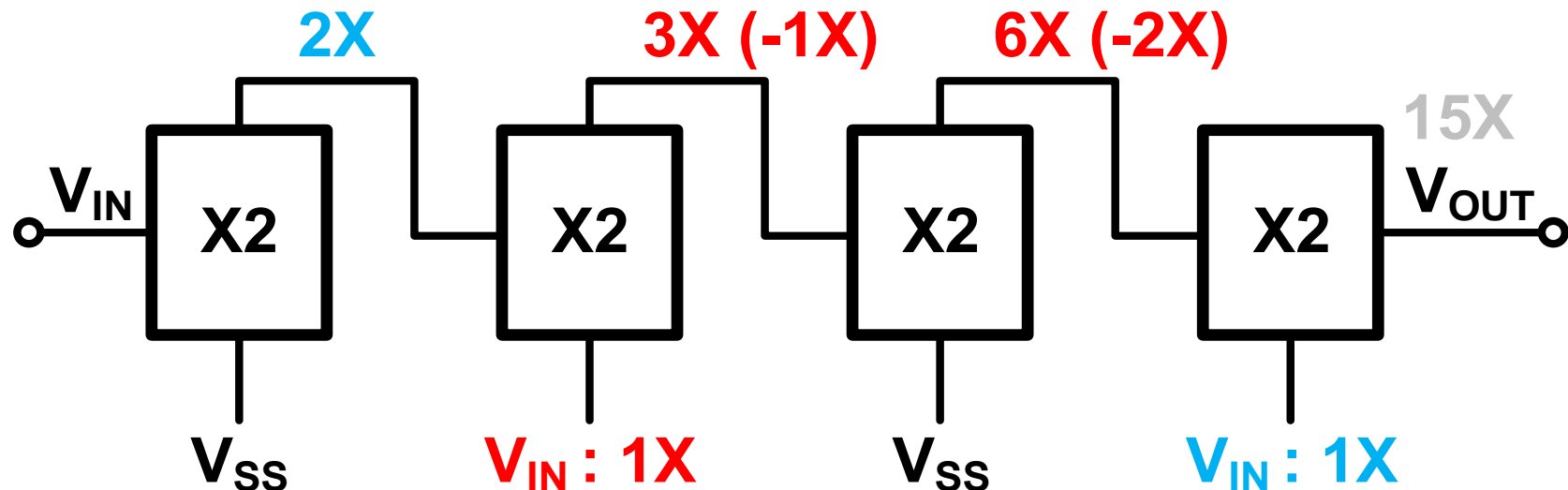
# Achieving Higher Conversion Ratios

- Bottom voltage modulation
  - Earlier stage has greater effect on ratio
  - Example:  $V_{SS} \rightarrow V_{IN}$  at 2<sup>nd</sup> stage



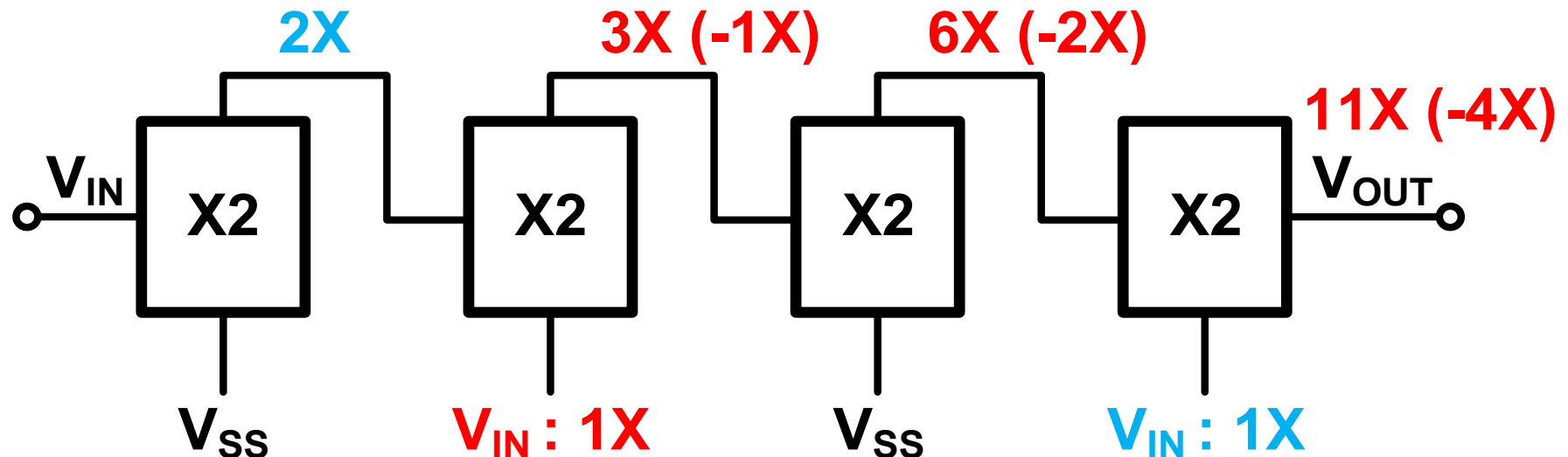
# Achieving Higher Conversion Ratios

- Bottom voltage modulation
  - Earlier stage has greater effect on ratio
  - Example:  $V_{SS} \rightarrow V_{IN}$  at 2<sup>nd</sup> stage



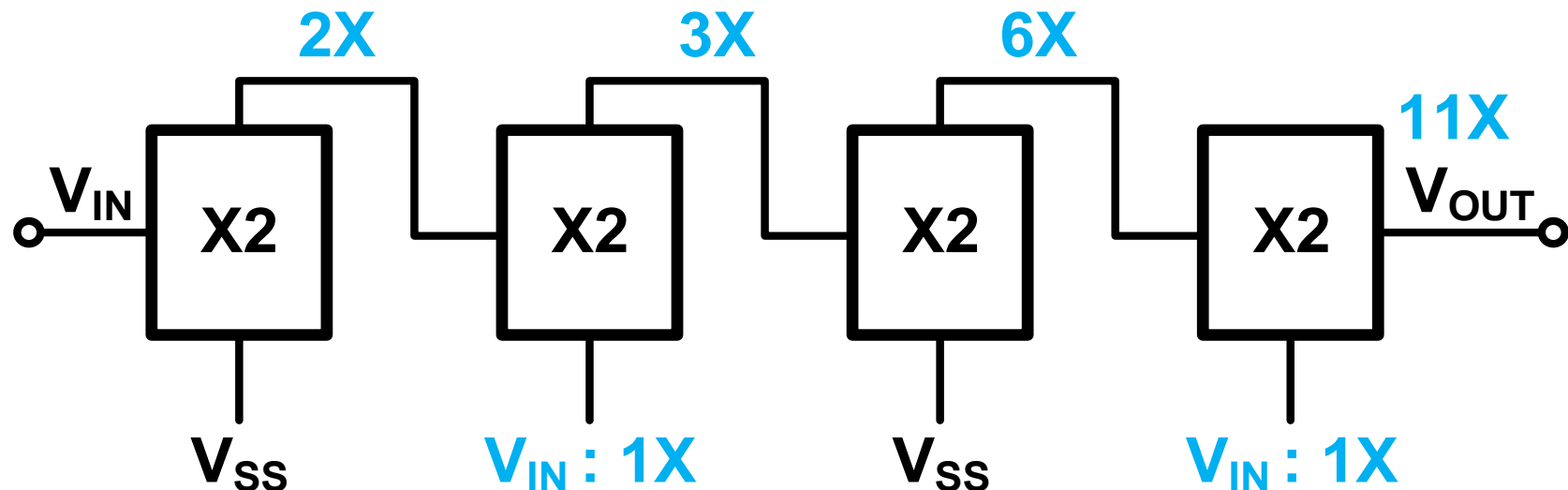
# Achieving Higher Conversion Ratios

- Bottom voltage modulation
  - Earlier stage has greater effect on ratio
  - Example:  $V_{SS} \rightarrow V_{IN}$  at 2<sup>nd</sup> stage  $\rightarrow$  **11X (-4X)**



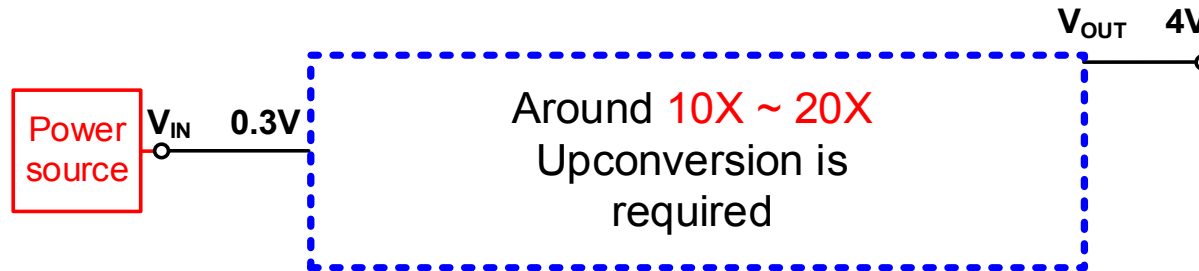
# Achieving Higher Conversion Ratios

- Bottom voltage modulation
  - Earlier stage has greater effect on ratio
  - Example:  $V_{SS} \rightarrow V_{IN}$  at 2<sup>nd</sup> stage  $\rightarrow$  **11X**
  - All changes are linearly combined
  - Arbitrary integer ratio can be achieved



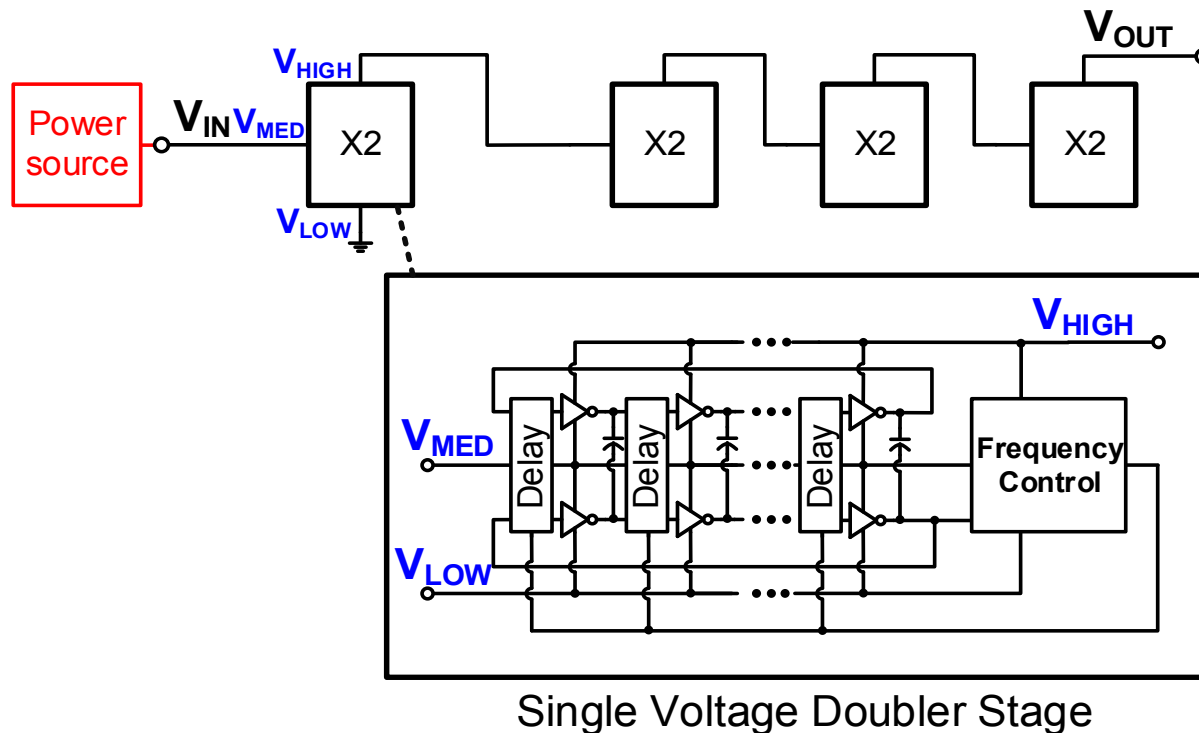
# Harvester System Architecture

- Up-conversion from low voltage harvesting source to battery
  - $V_{IN} \approx 0.3V$  (for solar cell),  $V_{OUT} \approx 4V$  (for battery)



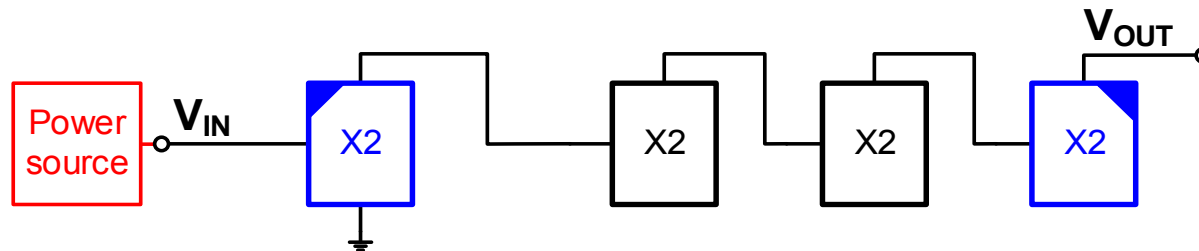
# Harvester System Architecture

- 4 cascaded voltage doublers – base **16X** ratio



# Harvester System Architecture

- Operating voltage is different at each stage
  - Bootstrapped lower  $V_{TH}$  drivers at 1<sup>st</sup> stage
  - Thick-oxide IO devices at the final stage

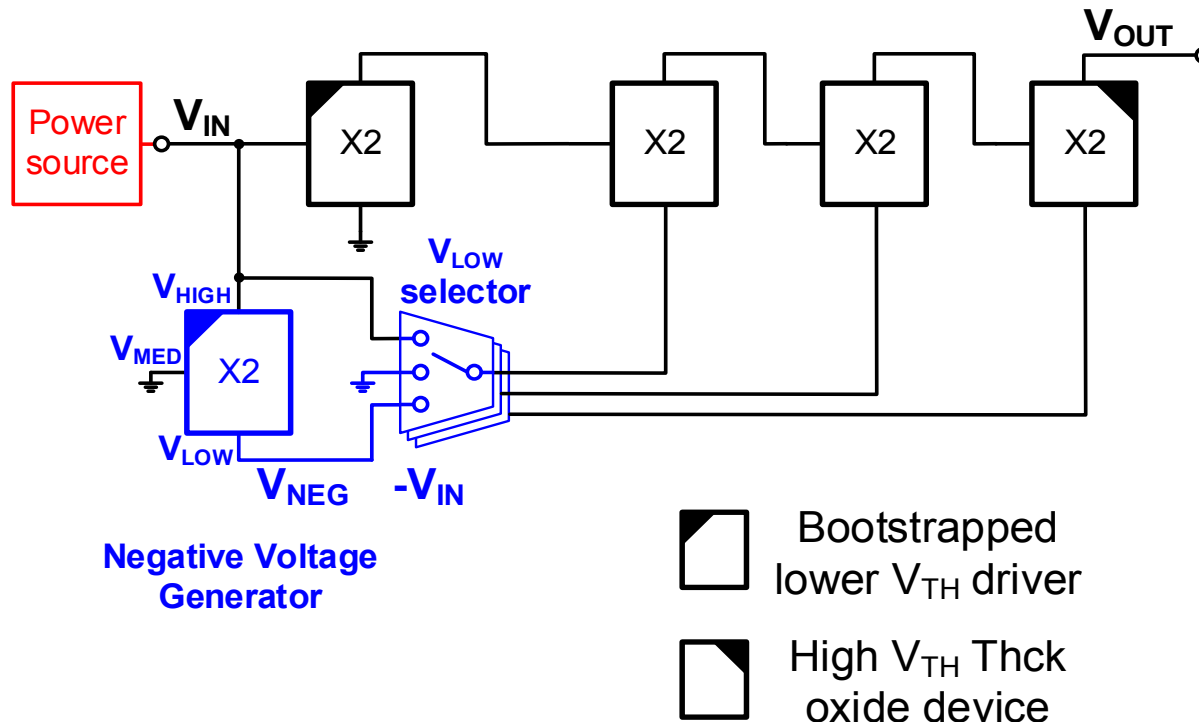


 Bootstrapped  
lower  $V_{TH}$  driver

 High  $V_{TH}$  Thick  
oxide device

# Harvester System Architecture

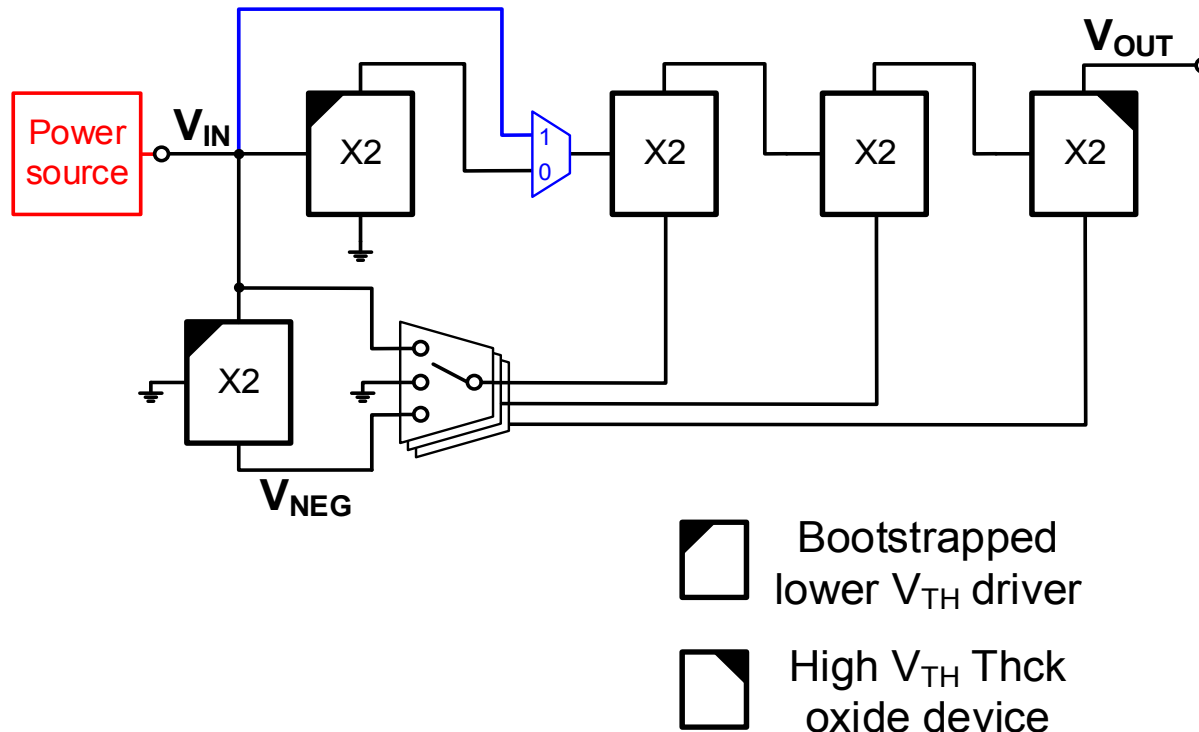
- Conversion ratio modulation for optimum  $V_{IN}$  level
- Bottom voltage is selected from  $V_{IN}$ ,  $G_{ND}$ ,  $V_{NEG}$ 
  - $V_{NEG}$  is generated using same doubler structure
- 16X – 23X ratios





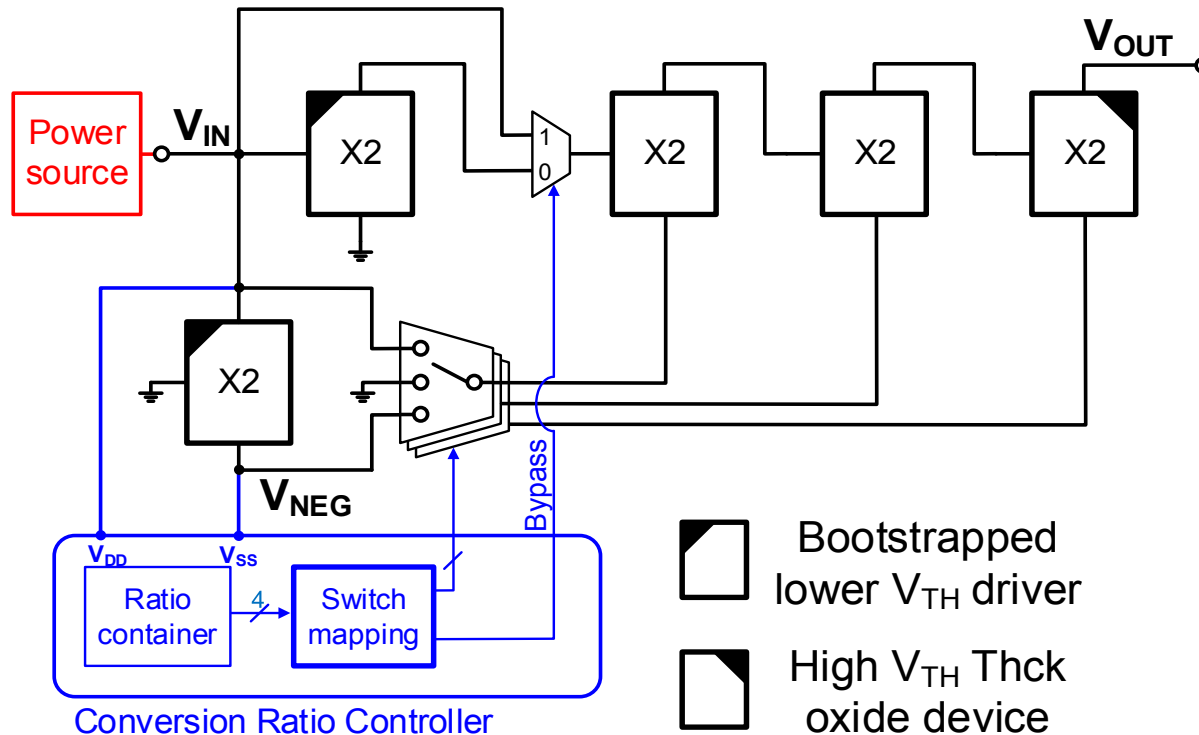
# Harvester System Architecture

- Conversion ratio modulation for optimum  $V_{IN}$  level
- Bypass 1<sup>st</sup> stage for lower ratios (9X – 15X)
- 9X – 23X ratios



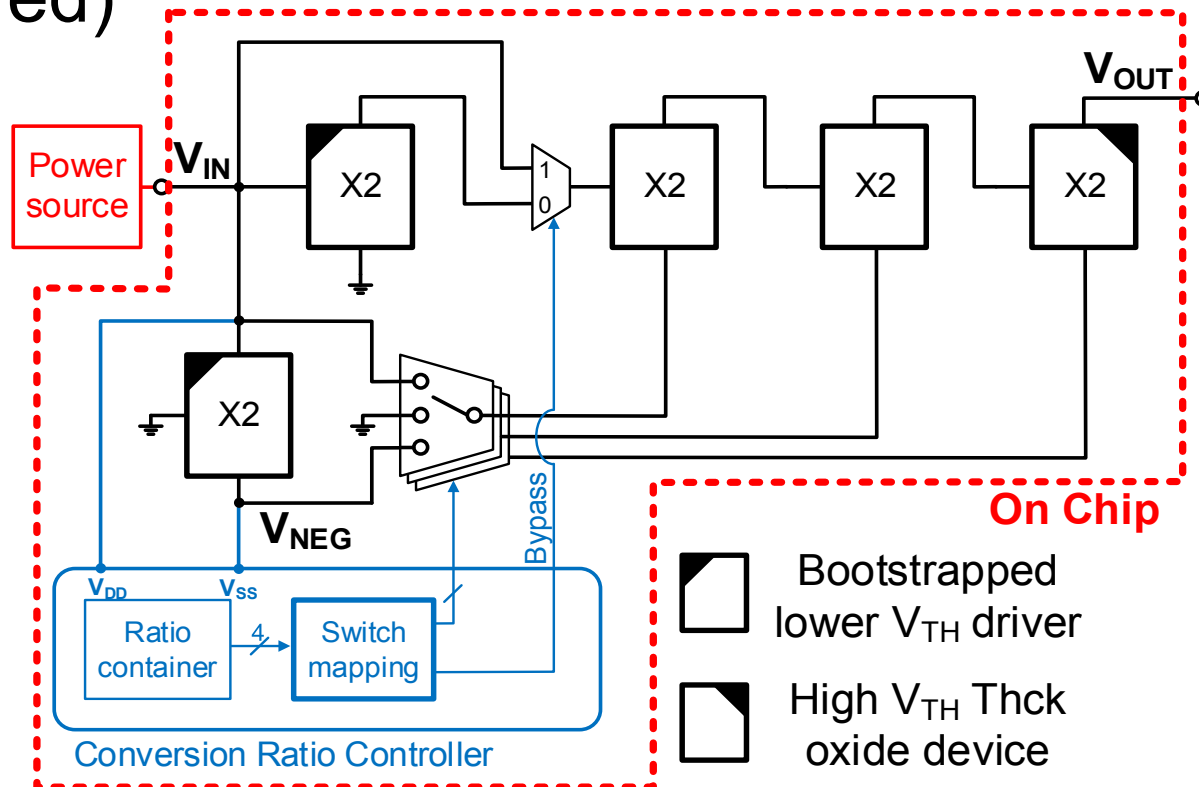
# Harvester System Architecture

- Ratio controller operates between  $V_{IN}$  and  $V_{NEG}$  for better self-startup capability



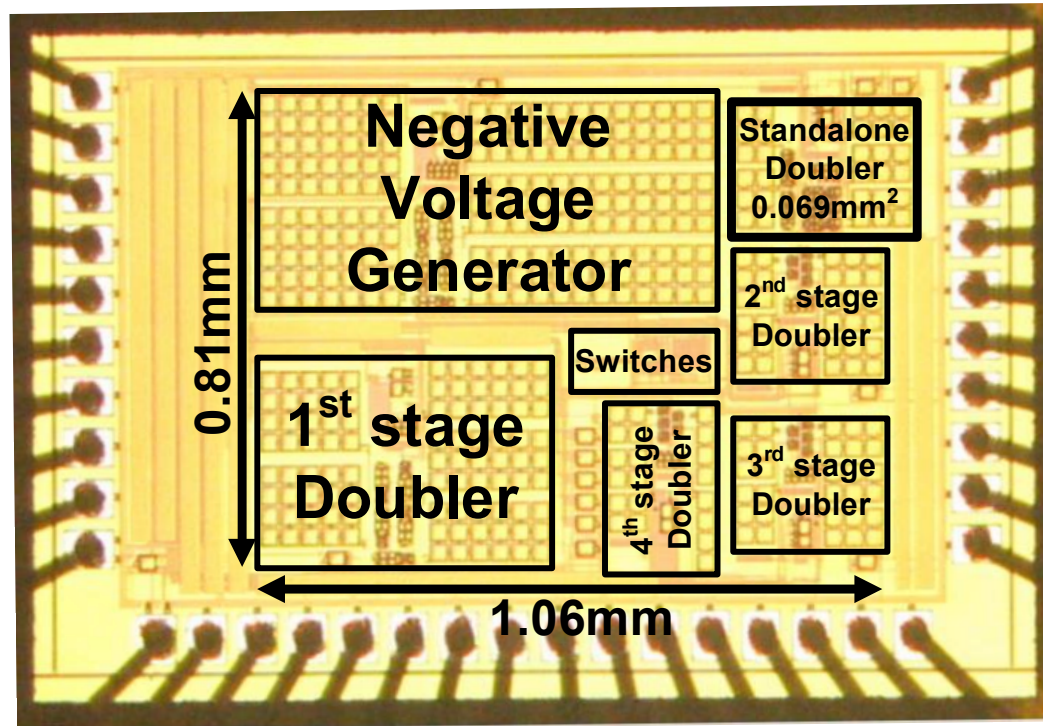
# Harvester System Architecture

- Whole system is fully integrated on chip
- No external devices are needed
- Capable of self-startup with low  $V_{IN}$  (140mV, measured)



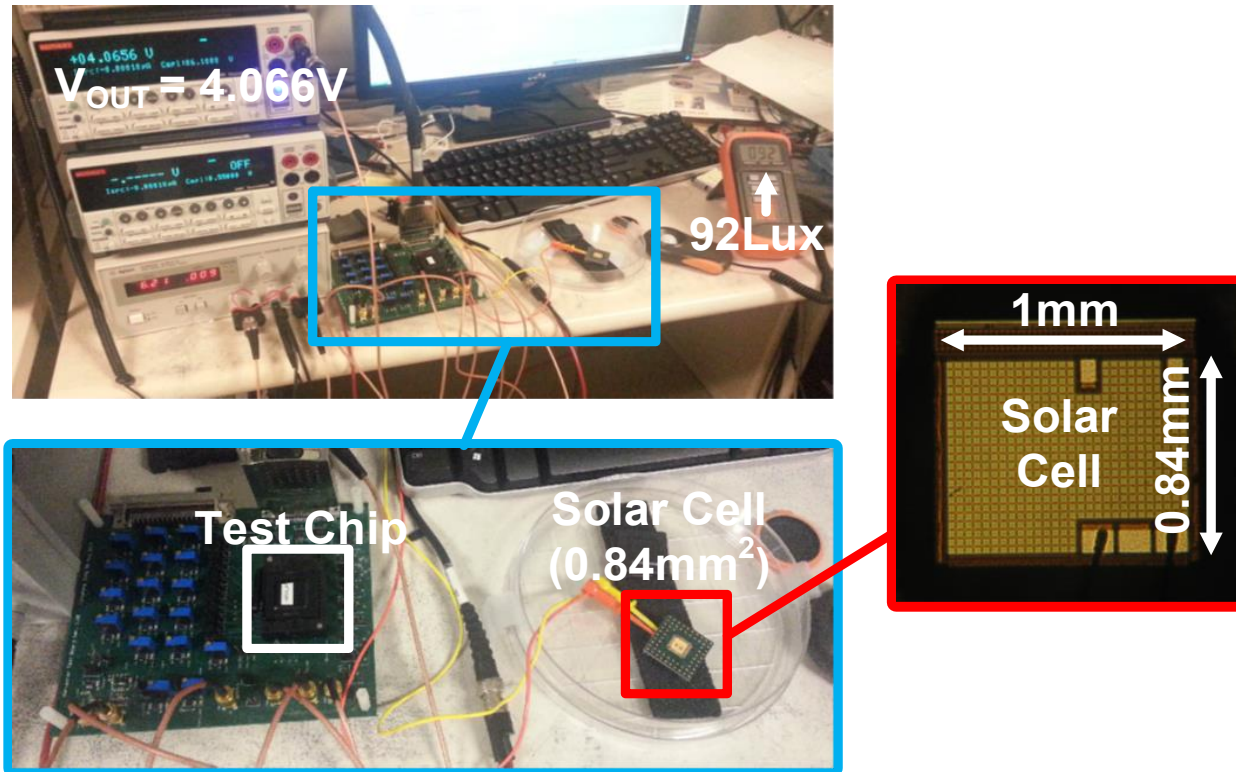
# Die Micrograph

- 0.18 $\mu\text{m}$  CMOS test chip
- Standalone voltage doubler: 0.069mm<sup>2</sup>, 54pF total flying cap
- Harvester: 0.86mm<sup>2</sup>, 600pF total flying cap



# Test Setup

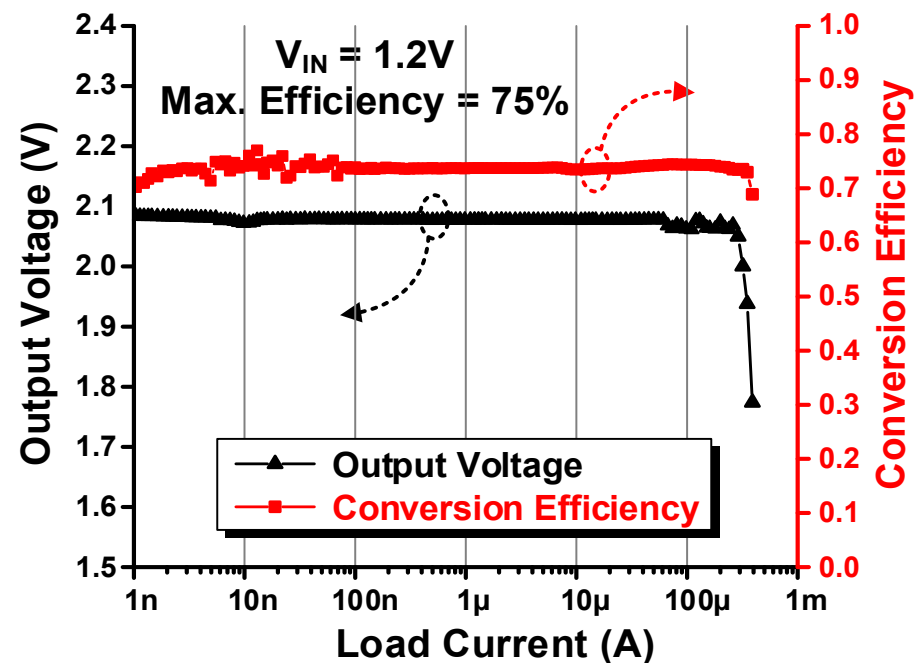
- Test with voltage / current source
- Test with silicon solar cell chip
  - $0.84\text{mm}^2$  130nm CMOS ( $\sim 10\text{nW}$  under room light)



# MEASURED RESULTS

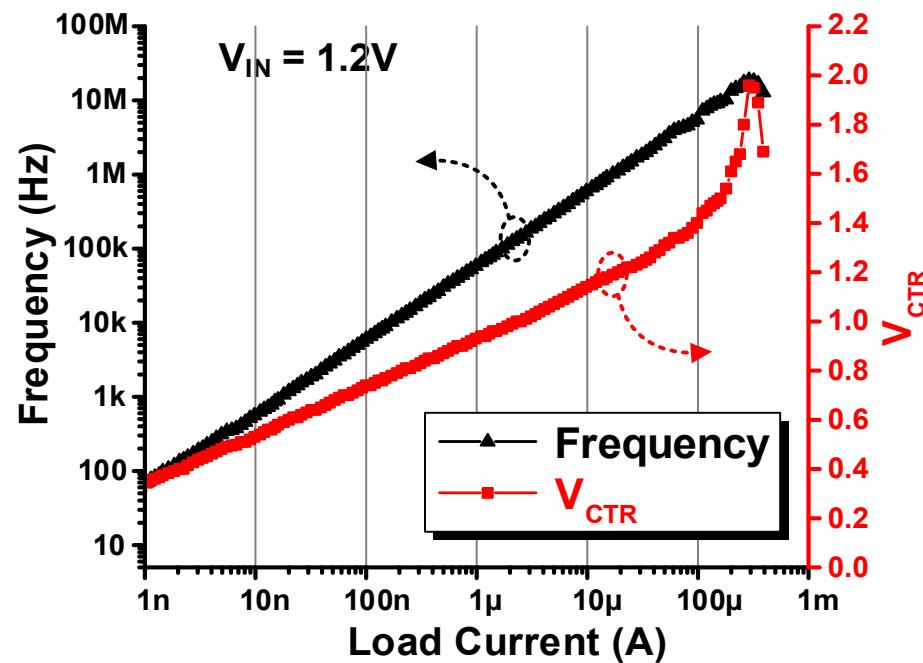
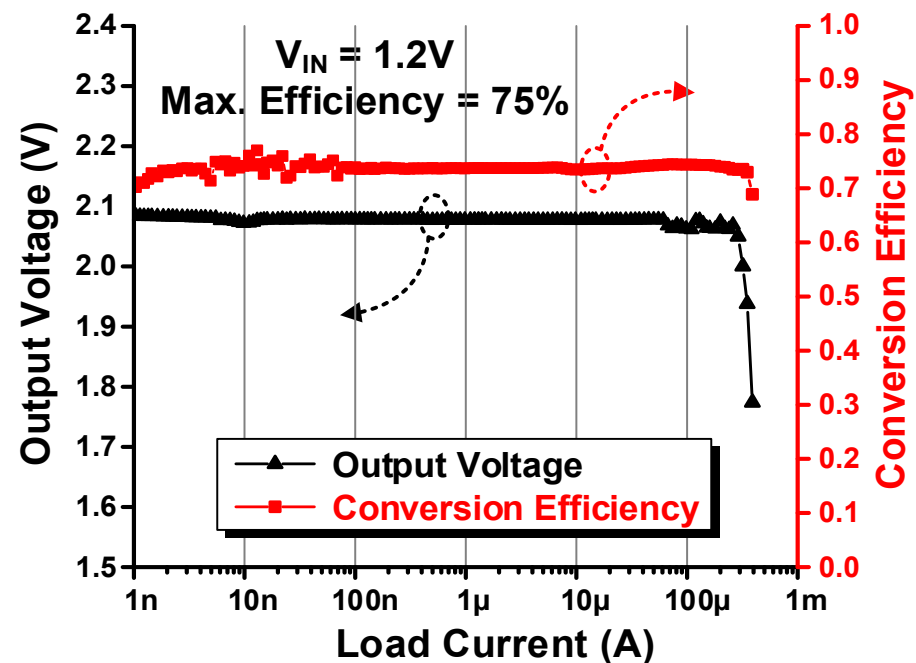
# Standalone Voltage Doubler

- $V_{IN} = 1.2V$ ,  $R_{DIV} = 1.73$  (for  $\Delta$  to be  $0.27 V_{IN}$ )
- Near maximum efficiency over  $>10^5$  range
- Idle power consumption: **170pW @ 1.2V  $V_{IN}$**



# Standalone Voltage Doubler

- $V_{IN} = 1.2V$ ,  $R_{DIV} = 1.73$  (for  $\Delta$  to be  $0.27 V_{IN}$ )
- Near maximum efficiency over  $>10^5$  range
- Idle power consumption: **170pW @ 1.2V  $V_{IN}$**





# Comparison of Voltage Doubler

	JSSC 2010 [5]	VLSI 2010 [6]	VLSI 2009 [7]	This work (Doubler)
<b>Technology</b>	32nm CMOS	45nm SOI CMOS w/ trench cap	0.13 $\mu$ m CMOS	<b>0.18<math>\mu</math>m CMOS</b>
<b>Architecture</b>	Multi-phase voltage doubler	1:2 step-up/down converter	Multi-phase voltage doubler	<b>Self-oscillating voltage doubler</b>
<b>Conversion ratio</b>	1 : 2	2 : 1, 1 : 2	1 : 2	<b>1 : 2</b>
<b>Tested input voltage</b>	1V-1.2V	1V	1V-1.2V	<b>1.2V</b>
<b>Frequency</b>	250MHz-2GHz <sup>1</sup>	100MHz	N/R	<b>70Hz-19MHz</b>
<b>Peak efficiency</b>	64%	90%	82%	<b>75%</b>
<b>Load range</b>	0.4mA-9mA w/ $\eta > 40\%$ <sup>1</sup>	0.5mA-5mA w/ $\eta > 80\%$ <sup>1</sup>	0.15mA-2.2mA w/ $\eta > 70\%$ <sup>1</sup>	<b>1nA-0.35mA w/ <math>\eta &gt; 70\%</math></b>
<b>Area</b>	0.0067mm <sup>2</sup>	0.0012mm <sup>2</sup>	2.25mm <sup>2</sup>	<b>0.069mm<sup>2</sup></b>

N/R: Not reported

<sup>1</sup> : Estimated number from the paper

# Comparison of Voltage Doubler

	JSSC 2010 [5]	VLSI 2010 [6]	VLSI 2009 [7]	This work (Doubler)
<b>Technology</b>	32nm CMOS	45nm SOI CMOS w/ trench cap	0.13 $\mu$ m CMOS	<b>0.18<math>\mu</math>m CMOS</b>
<b>Architecture</b>	Multi-phase voltage doubler	1:2 step-up/down converter	Multi-phase voltage doubler	<b>Self-oscillating voltage doubler</b>
<b>Conversion ratio</b>	1 : 2	2 : 1, 1 : 2	1 : 2	<b>1 : 2</b>
<b>Tested input voltage</b>	1V-1.2V	1V	1V-1.2V	<b>1.2V</b>
<b>Frequency</b>	250MHz-2GHz <sup>1</sup>	100MHz	N/R	<b>70Hz-19MHz</b>
<b>Peak efficiency</b>	64%	90%	82%	<b>75%</b>
<b>Load range</b>	0.4mA-9mA w/ $\eta > 40\%$ <sup>1</sup>	0.5mA-5mA w/ $\eta > 80\%$ <sup>1</sup>	0.15mA-2.2mA w/ $\eta > 70\%$ <sup>1</sup>	<b>1nA-0.35mA w/ <math>\eta &gt; 70\%</math></b>
<b>Area</b>	0.0067mm <sup>2</sup>	0.0012mm <sup>2</sup>	2.25mm <sup>2</sup>	<b>0.069mm<sup>2</sup></b>

N/R: Not reported

<sup>1</sup> : Estimated number from the paper

# Comparison of Voltage Doubler

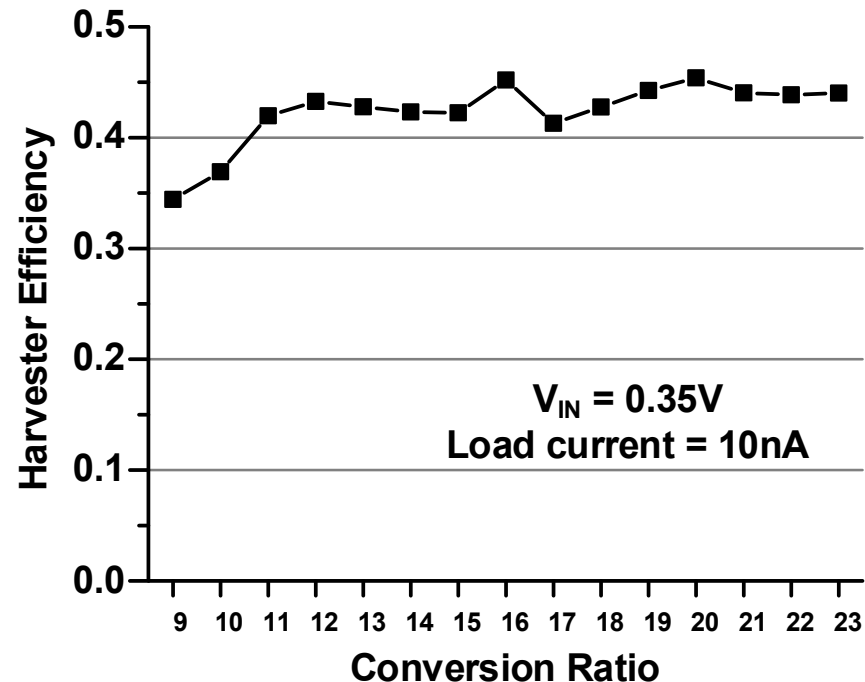
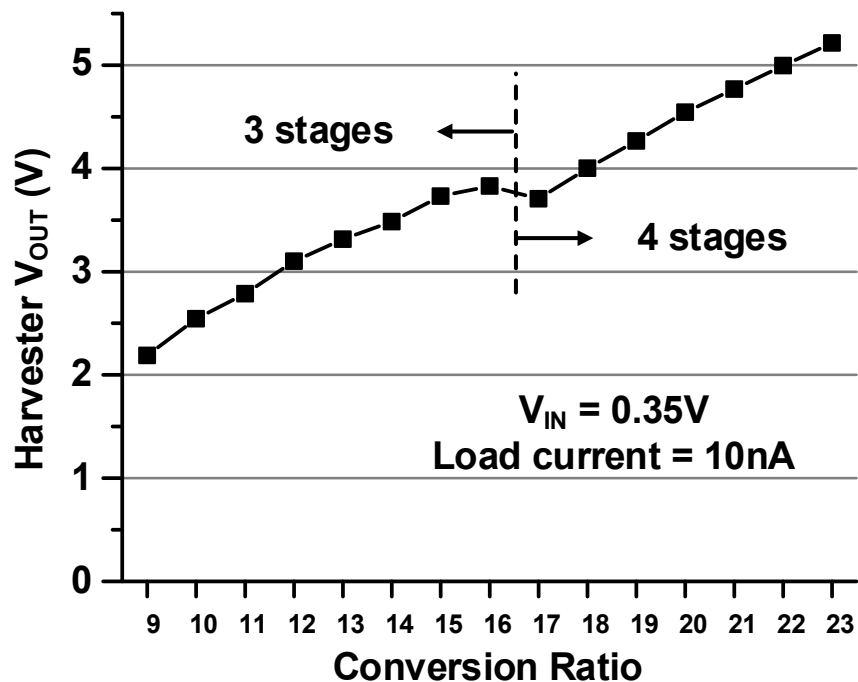
	JSSC 2010 [5]	VLSI 2010 [6]	VLSI 2009 [7]	This work (Doubler)
<b>Technology</b>	32nm CMOS	45nm SOI CMOS w/ trench cap	0.13 $\mu$ m CMOS	<b>0.18<math>\mu</math>m CMOS</b>
<b>Architecture</b>	Multi-phase voltage doubler	1:2 step-up/down converter	Multi-phase voltage doubler	<b>Self-oscillating voltage doubler</b>
<b>Conversion ratio</b>	1 : 2	2 : 1, 1 : 2	1 : 2	<b>1 : 2</b>
<b>Tested input voltage</b>	1V-1.2V	1V	1V-1.2V	<b>1.2V</b>
<b>Frequency</b>	250MHz-2GHz <sup>1</sup>	100MHz	N/R	<b>70Hz-19MHz</b>
<b>Peak efficiency</b>	64%	90%	82%	<b>75%</b>
<b>Load range</b>	0.4mA-9mA w/ $\eta > 40\%$ <sup>1</sup>	0.5mA-5mA w/ $\eta > 80\%$ <sup>1</sup>	0.15mA-2.2mA w/ $\eta > 70\%$ <sup>1</sup>	<b>1nA-0.35mA w/ <math>\eta &gt; 70\%</math></b>
<b>Area</b>	0.0067mm <sup>2</sup>	0.0012mm <sup>2</sup>	2.25mm <sup>2</sup>	<b>0.069mm<sup>2</sup></b>

N/R: Not reported

<sup>1</sup>: Estimated number from the paper

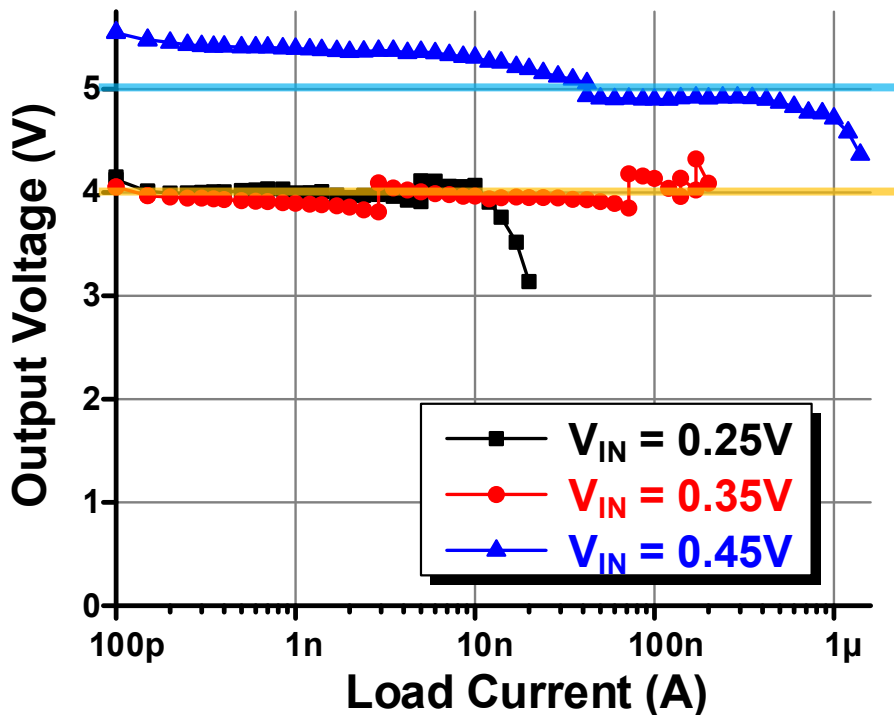
# Harvester

- Conversion ratio control
  - $V_{OUT}$  of **2.2V** to **5.2V** from 0.35V  $V_{IN}$



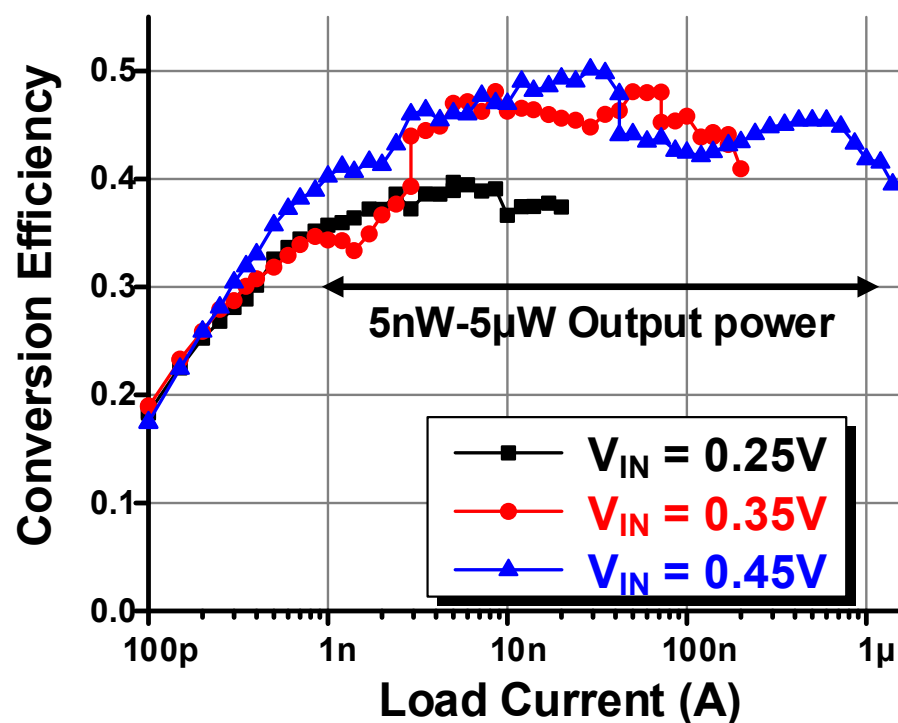
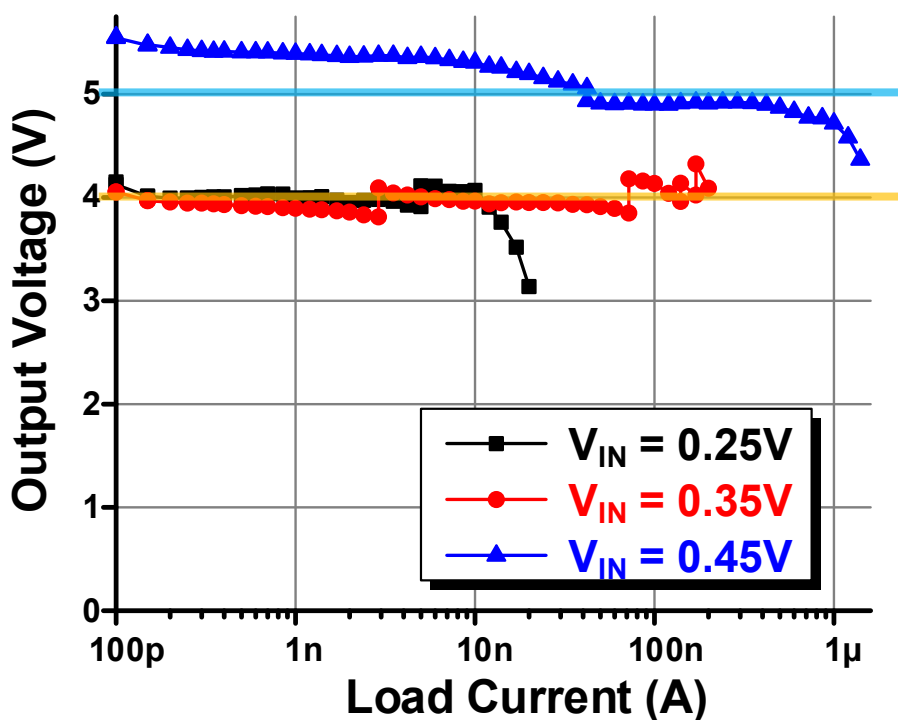
# Harvester

- Result for  $V_{IN} = 0.25V$ ,  $0.35V$ , and  $0.45V$ 
  - Conversion ratio controlled to keep  $V_{OUT}$  flat
  - Idle power consumption:  $<3nW$



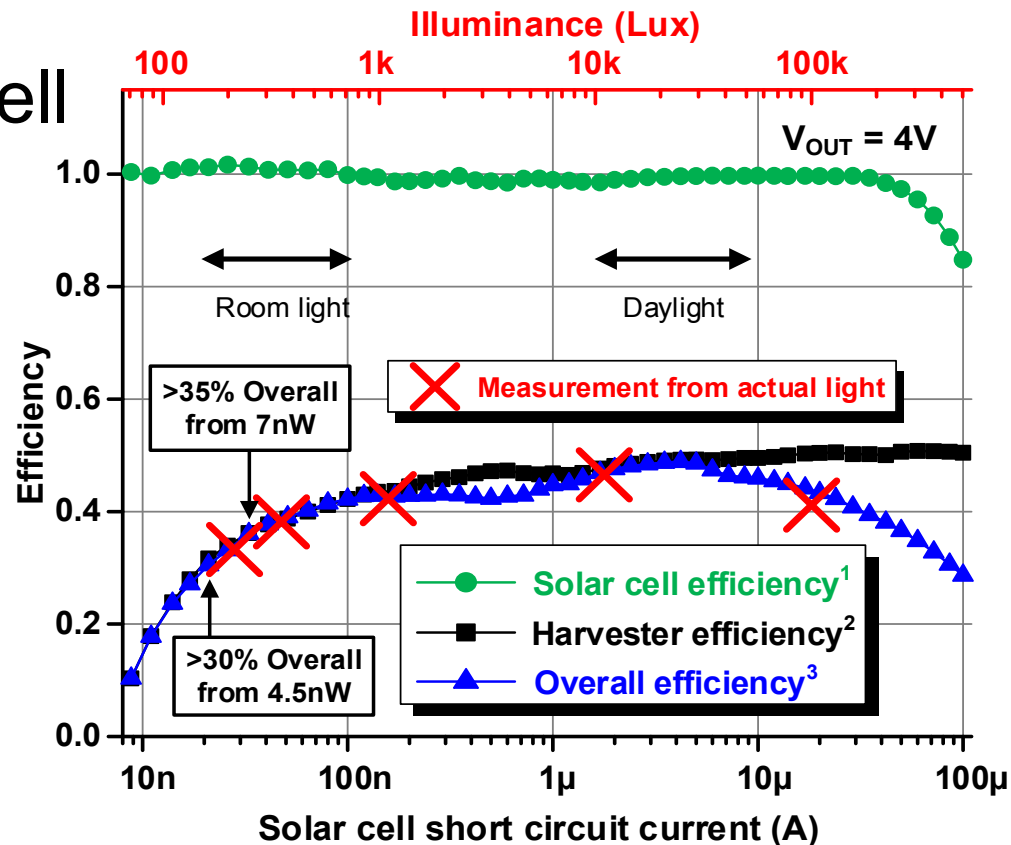
# Harvester

- Result for  $V_{IN} = 0.25V$ ,  $0.35V$ , and  $0.45V$ 
  - Conversion ratio controlled to keep  $V_{OUT}$  flat
  - Idle power consumption:  $<3nW$



# Harvester with Solar Cell

- 0.86mm<sup>2</sup> harvester with 0.84mm<sup>2</sup> CMOS solar cell
- Operates properly under room light to daylight condition
- Conversion ratio modulation can bring  $V_{IN}$  near optimum level
- Able to cold start from dim light of <200lux (~6nW from solar cell)



1. Solar cell efficiency  
= Harvester input / Max. Solar cell power
2. Harvester efficiency  
= Harvester output / Harvester input
3. Overall efficiency  
= Harvester output / Max. Solar cell power

# Comparison of Harvester

	ISSCC 2012 [2]	ASP-DAC 2012 [4]	ISSCC 2009 [8]	This work (Harvester)
<b>Technology</b>	0.13 $\mu$ m CMOS	65nm CMOS	0.35 $\mu$ m CMOS	0.18 $\mu$ m CMOS
<b>Architecture</b>	Transformer self-startup	Integrated charge pump	Integrated charge pump	<b>Cascade of voltage doublers</b>
<b>Fully integrated</b>	No (transformer)	Yes	Yes	Yes
<b>Self-startup</b>	Yes (min. 40mV)	Yes (min. 120mV)	N/R	Yes (min. 140mV)
<b>Input voltage</b>	40mV-300mV	0.12V-0.16V	0.6V-4V	0.14V-0.5V
<b>Output voltage</b>	2V	1V, 1.8V, 3V	N/R	2.2V-5.2V (0.35V $V_{IN}$ , 10nA $I_{LOAD}$ )
<b>Peak efficiency</b>	61% @ 0.3V $V_{IN}$	38.8% @ 0.12V $V_{IN}$	70% @ 2V $V_{IN}$	50% @ 0.45V $V_{IN}$
<b>Output power range</b>	N/R	1 $\mu$ W-10 $\mu$ W w/ $\eta > 15\%$ <sup>1</sup>	1 $\mu$ W-1mW (Efficiency N/R)	5nW-5 $\mu$ W w/ $\eta > 40\%$
<b>Idle power consumption</b>	N/R	N/R	2 $\mu$ W @ 100 $\mu$ W input 7 $\mu$ W @ 1mW input	<3nW
<b>Minimum input power</b>	N/R	N/R	N/R	6nW for self-startup 1.7nW while harvesting
<b>Area</b>	0.093mm <sup>2</sup>	0.78mm <sup>2</sup>	59mm <sup>2</sup>	0.86mm <sup>2</sup>

N/R: Not reported

<sup>1</sup>: Estimated number from the paper



# Comparison of Harvester

	ISSCC 2012 [2]	ASP-DAC 2012 [4]	ISSCC 2009 [8]	This work (Harvester)
<b>Technology</b>	0.13 $\mu$ m CMOS	65nm CMOS	0.35 $\mu$ m CMOS	<b>0.18<math>\mu</math>m CMOS</b>
<b>Architecture</b>	Transformer self-startup	Integrated charge pump	Integrated charge pump	<b>Cascade of voltage doublers</b>
<b>Fully integrated</b>	No (transformer)	Yes	Yes	<b>Yes</b>
<b>Self-startup</b>	Yes (min. 40mV)	Yes (min. 120mV)	N/R	<b>Yes (min. 140mV)</b>
<b>Input voltage</b>	40mV-300mV	0.12V-0.16V	0.6V-4V	<b>0.14V-0.5V</b>
<b>Output voltage</b>	2V	1V, 1.8V, 3V	N/R	<b>2.2V-5.2V (0.35V <math>V_{IN}</math>, 10nA <math>I_{LOAD}</math>)</b>
<b>Peak efficiency</b>	61% @ 0.3V $V_{IN}$	38.8% @ 0.12V $V_{IN}$	70% @ 2V $V_{IN}$	<b>50% @ 0.45V <math>V_{IN}</math></b>
<b>Output power range</b>	N/R	1 $\mu$ W-10 $\mu$ W w/ $\eta > 15\%$ <sup>1</sup>	1 $\mu$ W-1mW (Efficiency N/R)	<b>5nW-5<math>\mu</math>W w/ <math>\eta &gt; 40\%</math></b>
<b>Idle power consumption</b>	N/R	N/R	2 $\mu$ W @ 100 $\mu$ W input 7 $\mu$ W @ 1mW input	<b>&lt;3nW</b>
<b>Minimum input power</b>	N/R	N/R	N/R	<b>6nW for self-startup 1.7nW while harvesting</b>
<b>Area</b>	0.093mm <sup>2</sup>	0.78mm <sup>2</sup>	59mm <sup>2</sup>	<b>0.86mm<sup>2</sup></b>

N/R: Not reported

<sup>1</sup>: Estimated number from the paper

# Comparison of Harvester

	ISSCC 2012 [2]	ASP-DAC 2012 [4]	ISSCC 2009 [8]	This work (Harvester)
<b>Technology</b>	0.13 $\mu$ m CMOS	65nm CMOS	0.35 $\mu$ m CMOS	<b>0.18<math>\mu</math>m CMOS</b>
<b>Architecture</b>	Transformer self-startup	Integrated charge pump	Integrated charge pump	<b>Cascade of voltage doublers</b>
<b>Fully integrated</b>	No (transformer)	Yes	Yes	Yes
<b>Self-startup</b>	Yes (min. 40mV)	Yes (min. 120mV)	N/R	<b>Yes (min. 140mV)</b>
<b>Input voltage</b>	40mV-300mV	0.12V-0.16V	0.6V-4V	<b>0.14V-0.5V</b>
<b>Output voltage</b>	2V	1V, 1.8V, 3V	N/R	<b>2.2V-5.2V (0.35V <math>V_{IN}</math>, 10nA <math>I_{LOAD}</math>)</b>
<b>Peak efficiency</b>	61% @ 0.3V $V_{IN}$	38.8% @ 0.12V $V_{IN}$	70% @ 2V $V_{IN}$	<b>50% @ 0.45V <math>V_{IN}</math></b>
<b>Output power range</b>	N/R	1 $\mu$ W-10 $\mu$ W w/ $\eta > 15\%$ <sup>1</sup>	1 $\mu$ W-1mW (Efficiency N/R)	<b>5nW-5<math>\mu</math>W w/ <math>\eta &gt; 40\%</math></b>
<b>Idle power consumption</b>	N/R	N/R	2 $\mu$ W @ 100 $\mu$ W input 7 $\mu$ W @ 1mW input	<b>&lt;3nW</b>
<b>Minimum input power</b>	N/R	N/R	N/R	<b>6nW for self-startup 1.7nW while harvesting</b>
<b>Area</b>	0.093mm <sup>2</sup>	0.78mm <sup>2</sup>	59mm <sup>2</sup>	<b>0.86mm<sup>2</sup></b>

N/R: Not reported

<sup>1</sup>: Estimated number from the paper

# Comparison of Harvester

	ISSCC 2012 [2]	ASP-DAC 2012 [4]	ISSCC 2009 [8]	This work (Harvester)
<b>Technology</b>	0.13 $\mu$ m CMOS	65nm CMOS	0.35 $\mu$ m CMOS	<b>0.18<math>\mu</math>m CMOS</b>
<b>Architecture</b>	Transformer self-startup	Integrated charge pump	Integrated charge pump	<b>Cascade of voltage doublers</b>
<b>Fully integrated</b>	No (transformer)	Yes	Yes	<b>Yes</b>
<b>Self-startup</b>	Yes (min. 40mV)	Yes (min. 120mV)	N/R	<b>Yes (min. 140mV)</b>
<b>Input voltage</b>	40mV-300mV	0.12V-0.16V	0.6V-4V	<b>0.14V-0.5V</b>
<b>Output voltage</b>	2V	1V, 1.8V, 3V	N/R	<b>2.2V-5.2V (0.35V <math>V_{IN}</math>, 10nA <math>I_{LOAD}</math>)</b>
<b>Peak efficiency</b>	61% @ 0.3V $V_{IN}$	38.8% @ 0.12V $V_{IN}$	70% @ 2V $V_{IN}$	<b>50% @ 0.45V <math>V_{IN}</math></b>
<b>Output power range</b>	N/R	1 $\mu$ W-10 $\mu$ W w/ $\eta > 15\%$ <sup>1</sup>	1 $\mu$ W-1mW (Efficiency N/R)	<b>5nW-5<math>\mu</math>W w/ <math>\eta &gt; 40\%</math></b>
<b>Idle power consumption</b>	N/R	N/R	2 $\mu$ W @ 100 $\mu$ W input 7 $\mu$ W @ 1mW input	<b>&lt;3nW</b>
<b>Minimum input power</b>	N/R	N/R	N/R	<b>6nW for self-startup 1.7nW while harvesting</b>
<b>Area</b>	0.093mm <sup>2</sup>	0.78mm <sup>2</sup>	59mm <sup>2</sup>	<b>0.86mm<sup>2</sup></b>

N/R: Not reported

<sup>1</sup>: Estimated number from the paper

# Comparison of Harvester

	ISSCC 2012 [2]	ASP-DAC 2012 [4]	ISSCC 2009 [8]	This work (Harvester)
<b>Technology</b>	0.13 $\mu$ m CMOS	65nm CMOS	0.35 $\mu$ m CMOS	<b>0.18<math>\mu</math>m CMOS</b>
<b>Architecture</b>	Transformer self-startup	Integrated charge pump	Integrated charge pump	<b>Cascade of voltage doublers</b>
<b>Fully integrated</b>	No (transformer)	Yes	Yes	<b>Yes</b>
<b>Self-startup</b>	Yes (min. 40mV)	Yes (min. 120mV)	N/R	<b>Yes (min. 140mV)</b>
<b>Input voltage</b>	40mV-300mV	0.12V-0.16V	0.6V-4V	<b>0.14V-0.5V</b>
<b>Output voltage</b>	2V	1V, 1.8V, 3V	N/R	<b>2.2V-5.2V (0.35V <math>V_{IN}</math>, 10nA <math>I_{LOAD}</math>)</b>
<b>Peak efficiency</b>	61% @ 0.3V $V_{IN}$	38.8% @ 0.12V $V_{IN}$	70% @ 2V $V_{IN}$	<b>50% @ 0.45V <math>V_{IN}</math></b>
<b>Output power range</b>	N/R	1 $\mu$ W-10 $\mu$ W w/ $\eta > 15\%$ <sup>1</sup>	1 $\mu$ W-1mW (Efficiency N/R)	<b>5nW-5<math>\mu</math>W w/ <math>\eta &gt; 40\%</math></b>
<b>Idle power consumption</b>	N/R	N/R	2 $\mu$ W @ 100 $\mu$ W input 7 $\mu$ W @ 1mW input	<b>&lt;3nW</b>
<b>Minimum input power</b>	N/R	N/R	N/R	<b>6nW for self-startup 1.7nW while harvesting</b>
<b>Area</b>	0.093mm <sup>2</sup>	0.78mm <sup>2</sup>	59mm <sup>2</sup>	<b>0.86mm<sup>2</sup></b>

N/R: Not reported

<sup>1</sup>: Estimated number from the paper

# Comparison of Harvester

	ISSCC 2012 [2]	ASP-DAC 2012 [4]	ISSCC 2009 [8]	This work (Harvester)
<b>Technology</b>	0.13 $\mu$ m CMOS	65nm CMOS	0.35 $\mu$ m CMOS	<b>0.18<math>\mu</math>m CMOS</b>
<b>Architecture</b>	Transformer self-startup	Integrated charge pump	Integrated charge pump	<b>Cascade of voltage doublers</b>
<b>Fully integrated</b>	No (transformer)	Yes	Yes	<b>Yes</b>
<b>Self-startup</b>	Yes (min. 40mV)	Yes (min. 120mV)	N/R	<b>Yes (min. 140mV)</b>
<b>Input voltage</b>	40mV-300mV	0.12V-0.16V	0.6V-4V	<b>0.14V-0.5V</b>
<b>Output voltage</b>	2V	1V, 1.8V, 3V	N/R	<b>2.2V-5.2V (0.35V <math>V_{IN}</math>, 10nA <math>I_{LOAD}</math>)</b>
<b>Peak efficiency</b>	61% @ 0.3V $V_{IN}$	38.8% @ 0.12V $V_{IN}$	70% @ 2V $V_{IN}$	<b>50% @ 0.45V <math>V_{IN}</math></b>
<b>Output power range</b>	N/R	1 $\mu$ W-10 $\mu$ W w/ $\eta > 15\%$ <sup>1</sup>	1 $\mu$ W-1mW (Efficiency N/R)	<b>5nW-5<math>\mu</math>W w/ <math>\eta &gt; 40\%</math></b>
<b>Idle power consumption</b>	N/R	N/R	2 $\mu$ W @ 100 $\mu$ W input 7 $\mu$ W @ 1mW input	<b>&lt;3nW</b>
<b>Minimum input power</b>	N/R	N/R	N/R	<b>6nW for self-startup 1.7nW while harvesting</b>
<b>Area</b>	0.093mm <sup>2</sup>	0.78mm <sup>2</sup>	59mm <sup>2</sup>	<b>0.86mm<sup>2</sup></b>

N/R: Not reported

<sup>1</sup>: Estimated number from the paper

# Conclusions

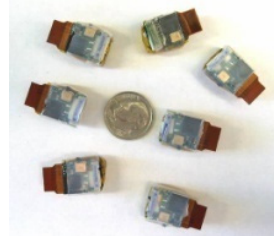
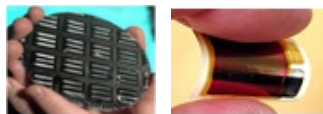
- Self-oscillating voltage doubler is proposed
  - Reduced overhead for clock generation and level shifting
  - Small output ripple by multi-phased operation
  - Frequency is automatically modulated to maximize efficiency
  - Test chip shows  $>10^5$  load range and 170pW idle power consumption
- Low power energy harvester is implemented
  - Cascading self-oscillating voltage doublers
  - Conversion ratio is modulated by changing bottom voltages
  - Capable of self-startup from 6nW input power

**Dual-Source Single-Inductor  
0.18 $\mu$ m CMOS Charger-Supply  
with Nested Hysteretic  
and Adaptive On-Time PWM Control**

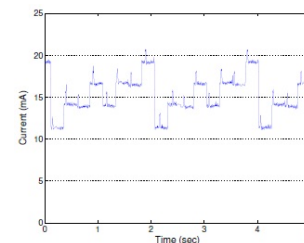
Suhwan Kim and Gabriel A. Rincón-Mora  
Georgia Tech Analog, Power, and Energy IC Research  
Georgia Institute of Technology, Atlanta, GA

# Outline

- Motivation / Challenges
- Hybrid Energy Sources / Power Conditioners



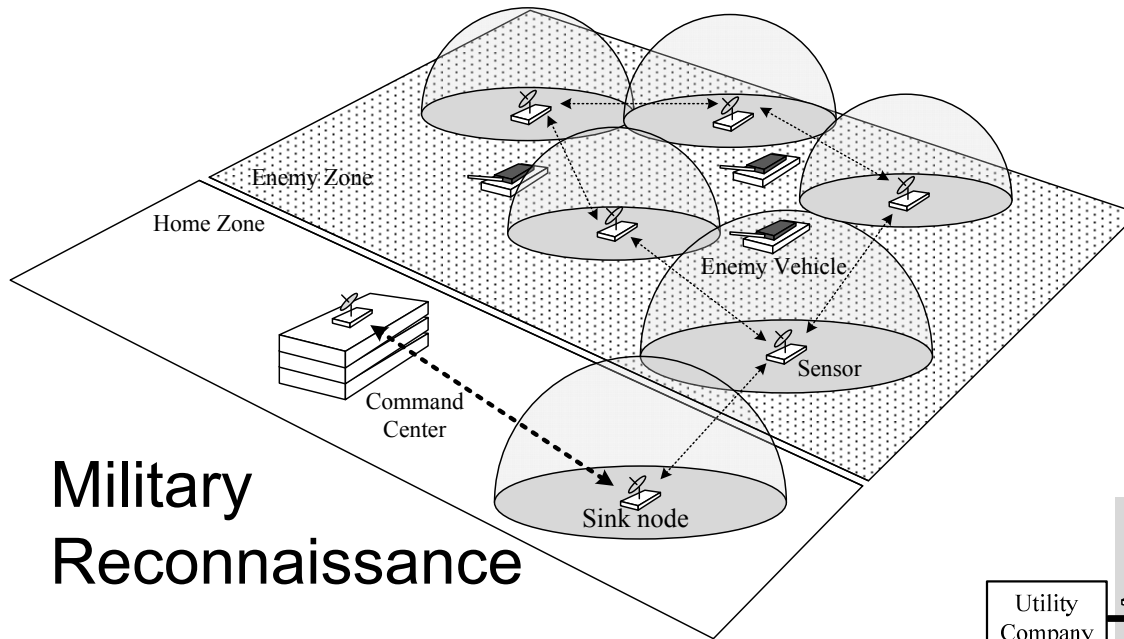
- Proposed Charger-Supply IC
  - Load-dependent Control
    - ✓ Light Mode: Hysteretic, Duty-cycled Operation
    - ✓ Heavy Mode: PWM Operation
- IC Prototype Results
  - ✓ Voltage Regulation
  - ✓ Efficiency, Reduction in of Required Sources
- Conclusions





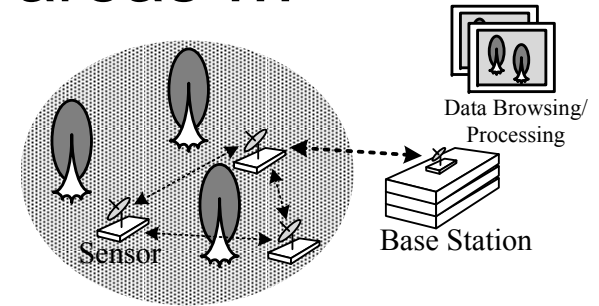
# Motivation

## Wireless sensors' wide application areas ...

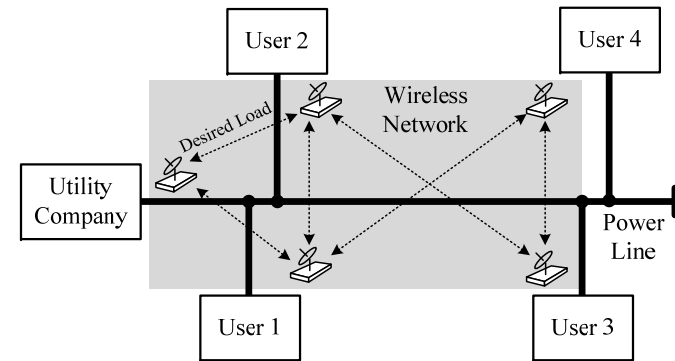


### Military Reconnaissance

✓ \$14.6B by 2019 *Reportlinker*



### Environment Monitoring

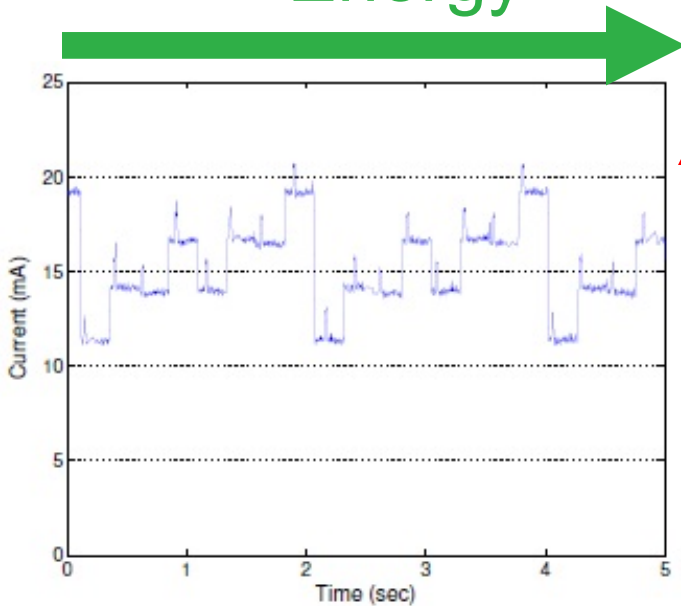


### Smart Grids

*“Wireless sensors can make  
Human Access to Important Information  
Much Easier, Safer, and Cheaper.”*

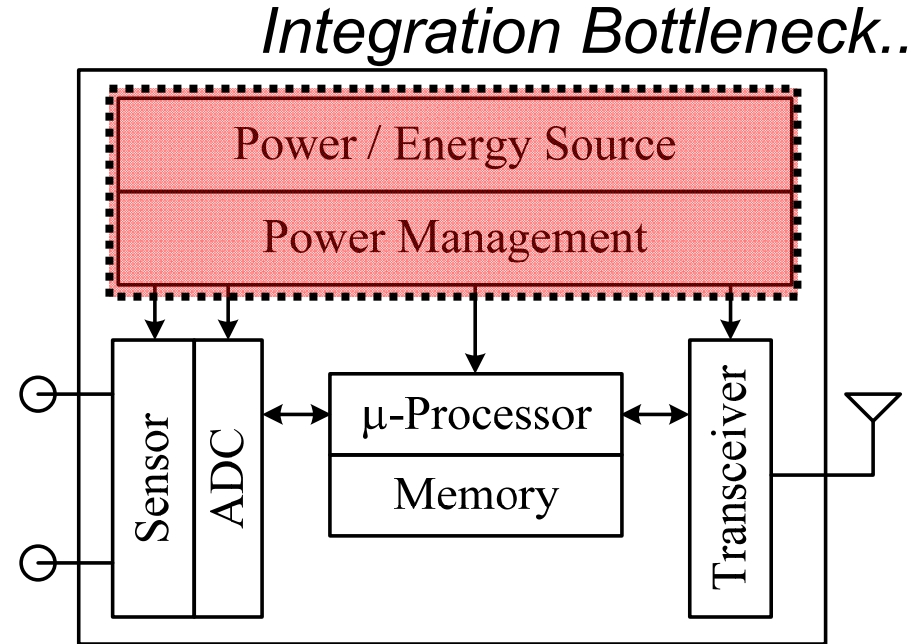
# Challenges

(1) Operational Life  
= Energy

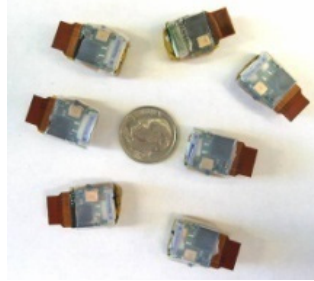


*Sensor's Load Profile*

(2) Functionality  
= Power



(3) In Limited Space :



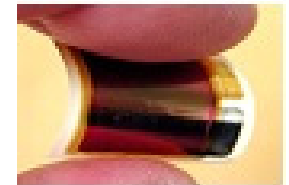
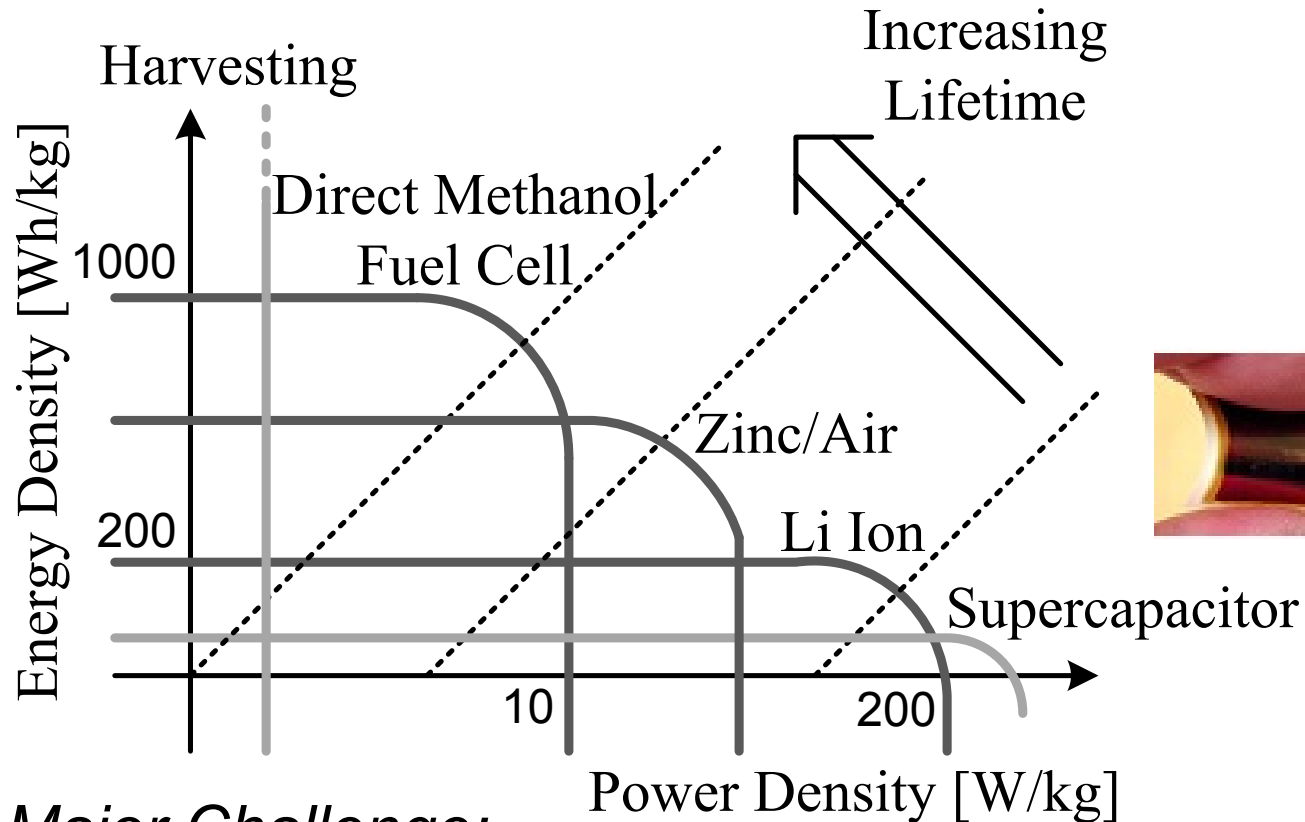
*Major Challenge:*

*Operational Life + Various Functionalities in Limited Space*

# Selection of Energy Sources

Ragone plot:

Energy and Power capabilities of energy sources



*Major Challenge:*

*Hard to find an Ideal Single Source  
with  $\uparrow$  Energy and  $\uparrow$  Power Densities*

# Hybrid Energy Sources

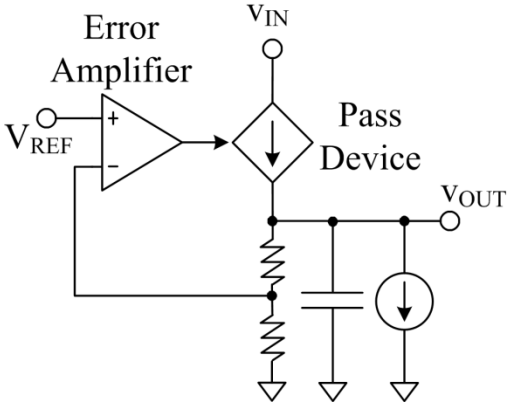
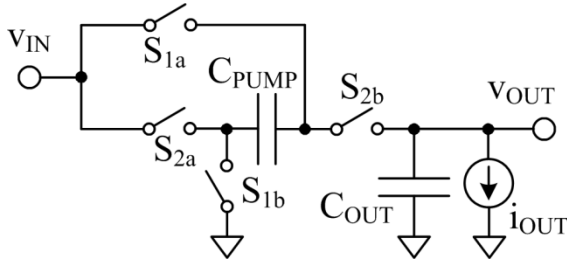
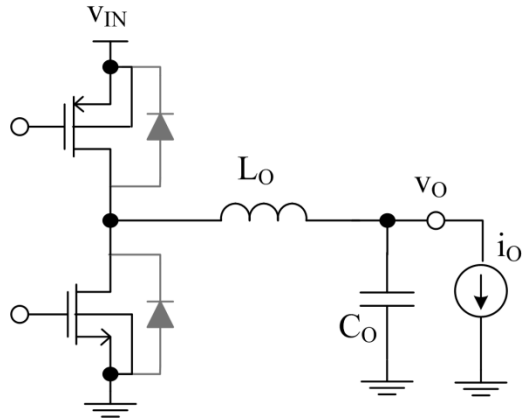
*To Achieve Optimum Volume for given Load's Targets:*

Solutions	Capability for unit volume	Required volume
<ul style="list-style-type: none"> <li>Energy-dense Source only</li> </ul>	<p><b>Sensor load's Target</b> ↓</p>	<p>Oversize x 4 for Power</p>
<ul style="list-style-type: none"> <li>Power-dense Source only</li> </ul>		<p>Oversize x 4 for Energy</p>
<ul style="list-style-type: none"> <li>✓ Energy-dense Source + Power-dense Source</li> </ul>		<p>✓ No Oversizing Required</p>

*Hybrid Energy Sources ...*

*Can meet Power and Lifetime demands with smaller volume.*

# Power Conditioners for Hybrid Sources

Linear Regulator	Switched Capacitor	✓ Switched Inductor
		
<ul style="list-style-type: none"> <li>▪ <math>V_{OUT} &lt; V_{IN}</math></li> <li>▪ <math>\uparrow</math> Conduction losses <math>\rightarrow \downarrow \eta</math></li> </ul>	<ul style="list-style-type: none"> <li>▪ <math>\uparrow \eta</math> for specific <math>V_{OUT}</math> from topology</li> <li>▪ Requires many switches in MIMO</li> </ul>	<ul style="list-style-type: none"> <li>▪ Flexible voltage in MIMO Converters</li> <li>▪ Single <math>\uparrow Q</math> inductor <math>\rightarrow</math> Compact and <math>\uparrow \eta</math></li> </ul>

*Inductor-based Switching Converters :*

*$\uparrow \eta$  Voltage Conversion for wide voltage ranges*

*$\rightarrow$  Suitable for MIMO Converters*

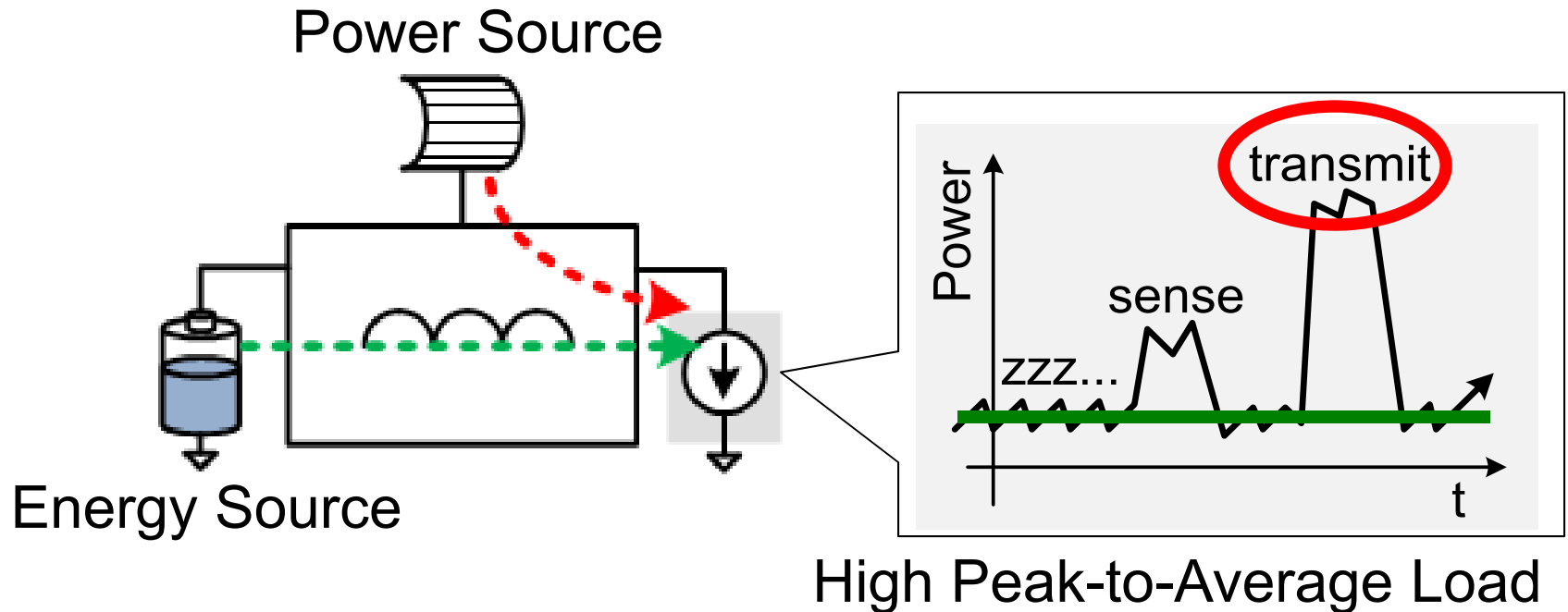
23.4: Dual-Source Single-Inductor 0.18 $\mu$ m CMOS Charger-Supply  
with Nested Hysteretic and Adaptive On-Time PWM Control

# Power Conditioners for Hybrid Sources

Control Intelligence Needed:

*Let Energy-dense Source to Supply Light Load*

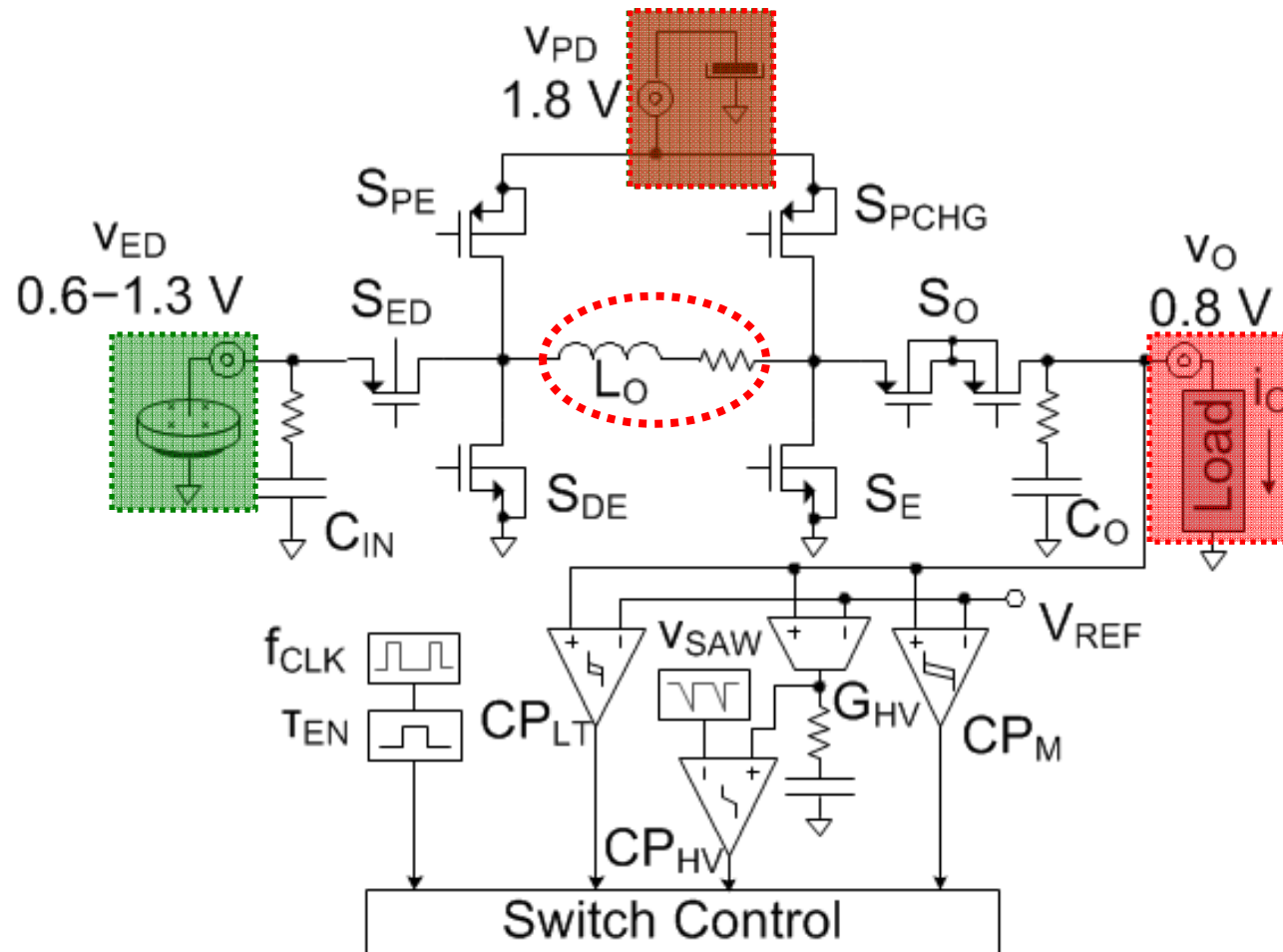
*Let Power-dense Source to Supply High, Peak Load*



Load-dependent Source-Selecting Control :

Can AVOID Oversizing *Energy Source* for Power Demand,  
*Power Source* for Lifetime Demand.

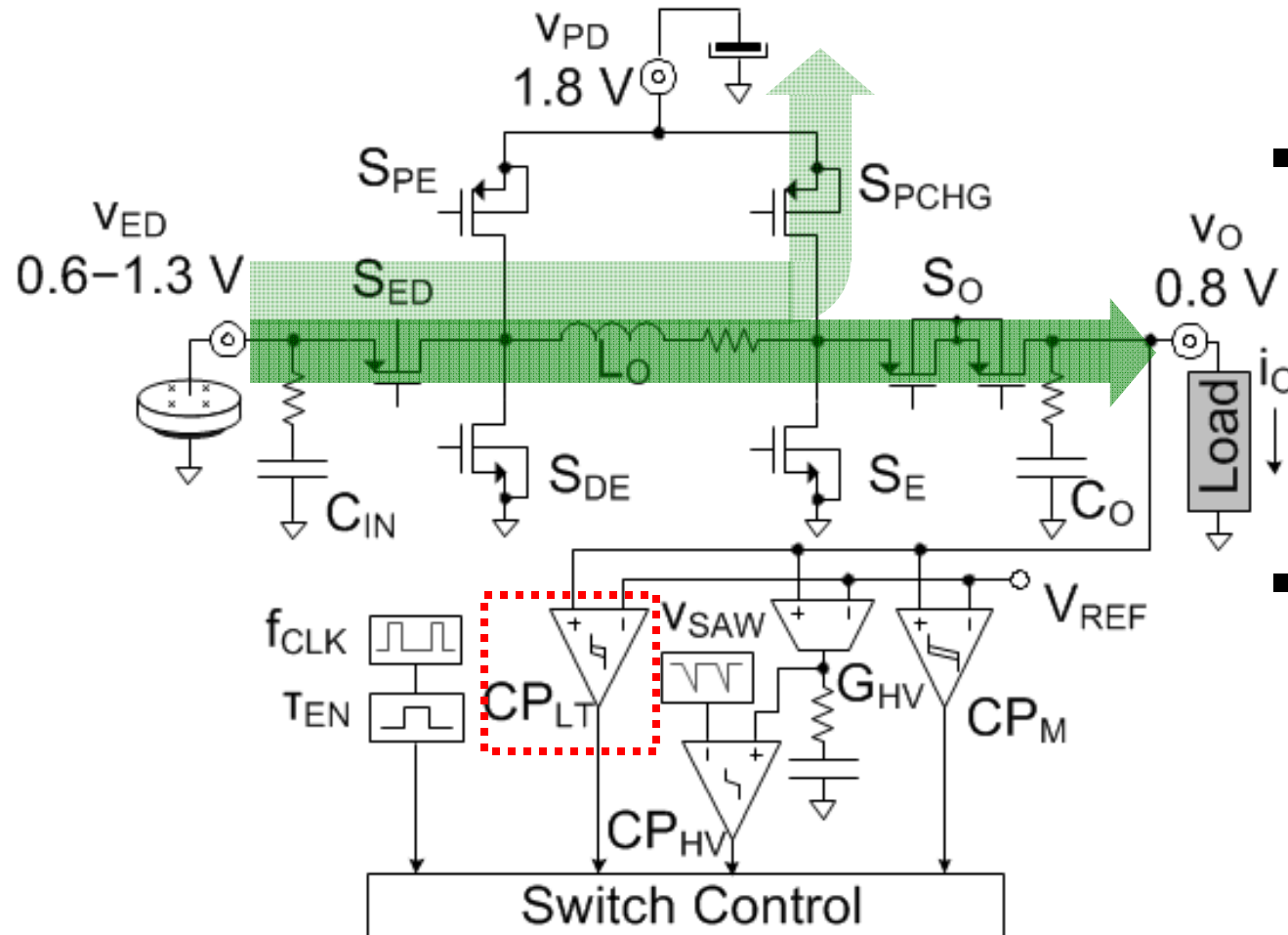
# Proposed PWM-Hysteretic Charger-supply



- Dual Input
  - ✓  $v_{ED}$  : Energy-dense Source
  - ✓  $v_{PD}$  : Power-dense Source
- Dual Output
  - ✓  $v_O$  : Load
  - ✓  $v_{PD}$  : When recharged
- Single Inductor

# Proposed PWM-Hysteretic Charger-supply

Energy Flow: (1) When  $p_O < P_{ED} \rightarrow$  Light Mode

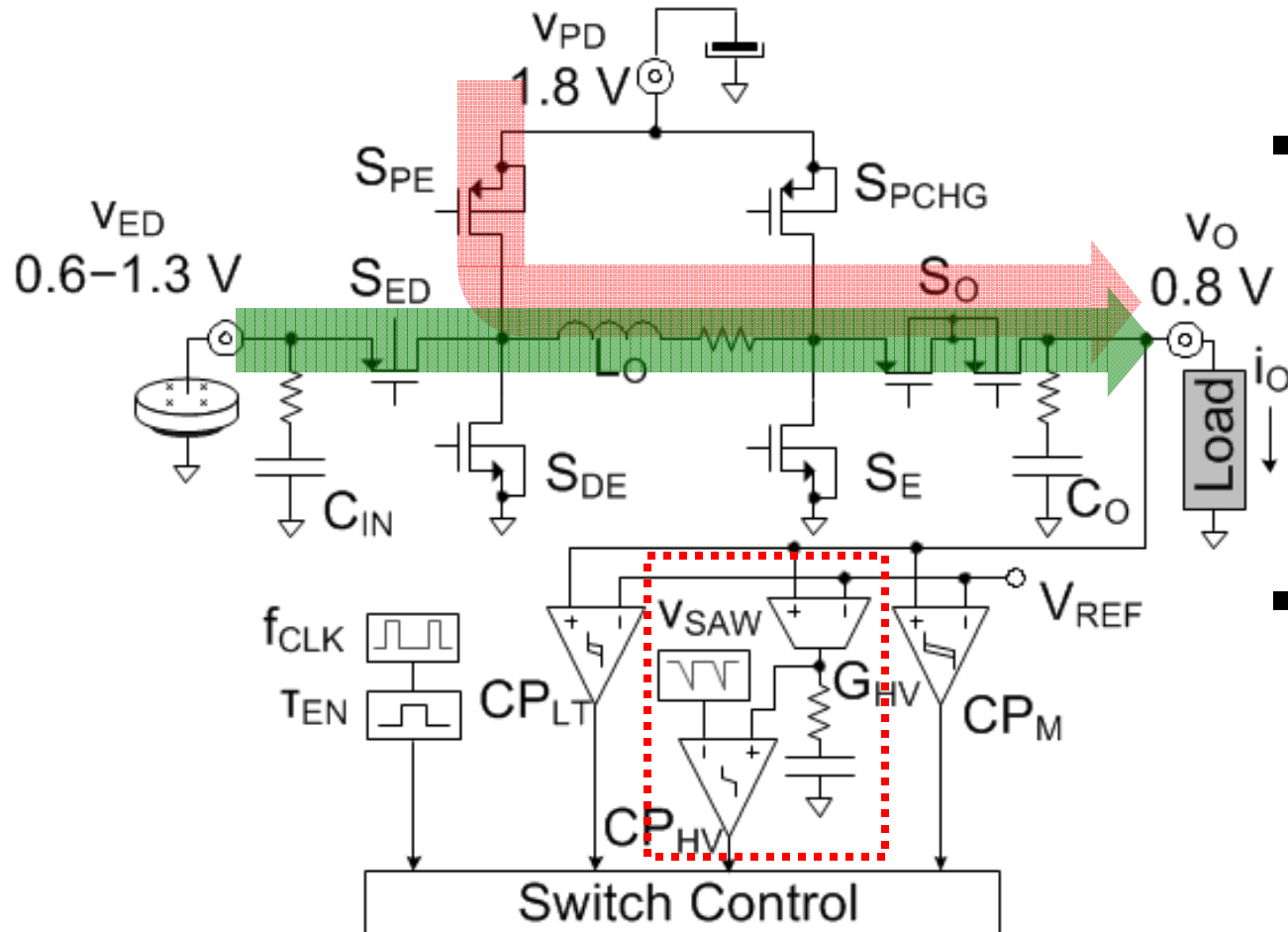


- Draw Const.  $P_{ED}$  from  $v_{ED}$ 
  - ✓ Supply Load
  - ✓ Recharge  $v_{PD}$  (if remnant  $P_{ED}$ )
- Hysteretic  $CP_{LT}$  :
  - ✓ Regulate  $v_O$  in Light Mode



# Proposed PWM-Hysteretic Charger-supply

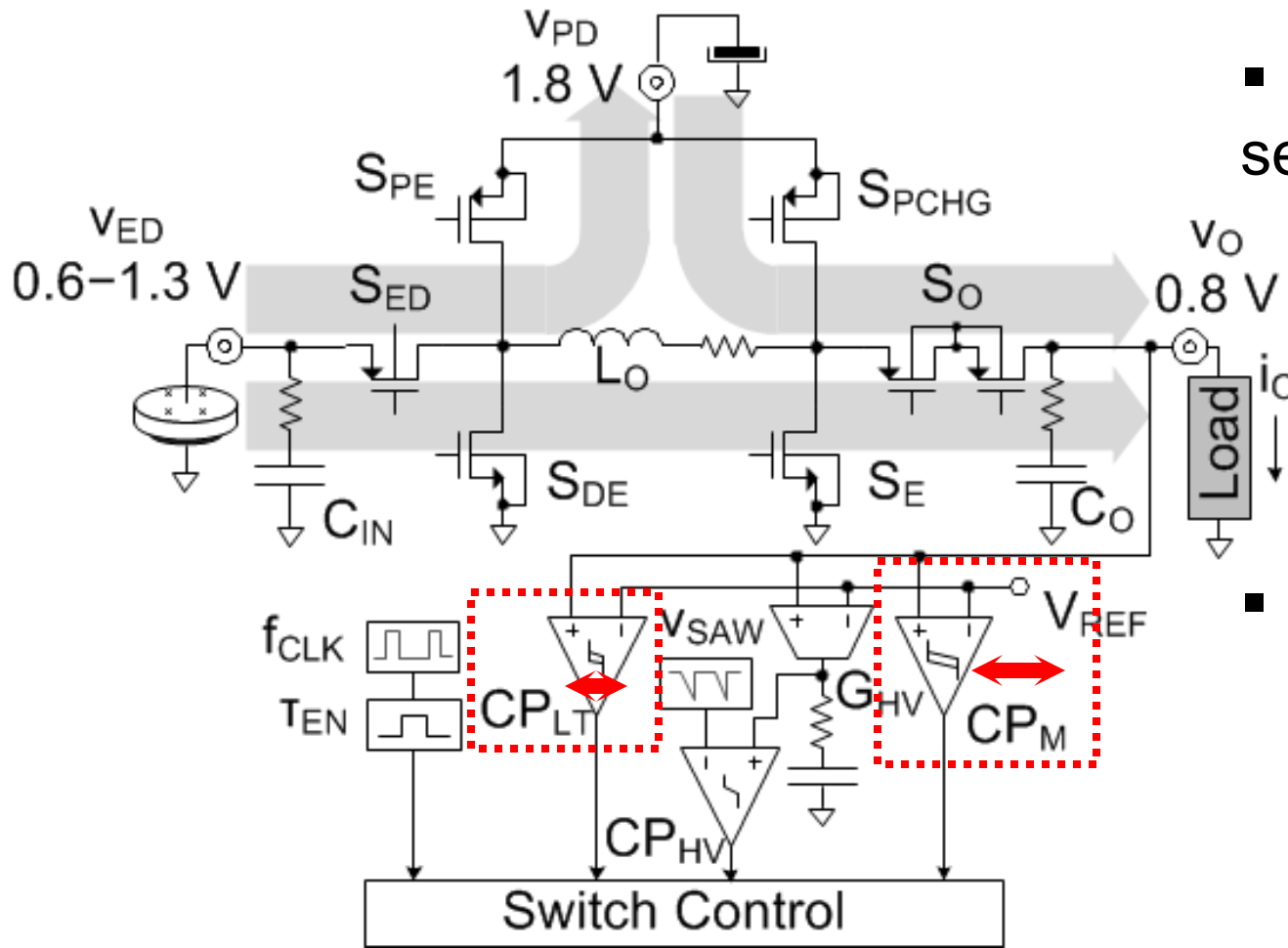
Energy Flow: (2) When  $p_O > P_{ED} \rightarrow$  Heavy Mode



- To supply  $p_o$ :
  - ✓ Const.  $P_{ED}$  from  $v_{ED}$
  - ✓ Var. Power from  $v_{PD}$  (PWM)
- PWM regulates  $v_o$  in Heavy Mode

# Proposed PWM-Hysteretic Charger-supply

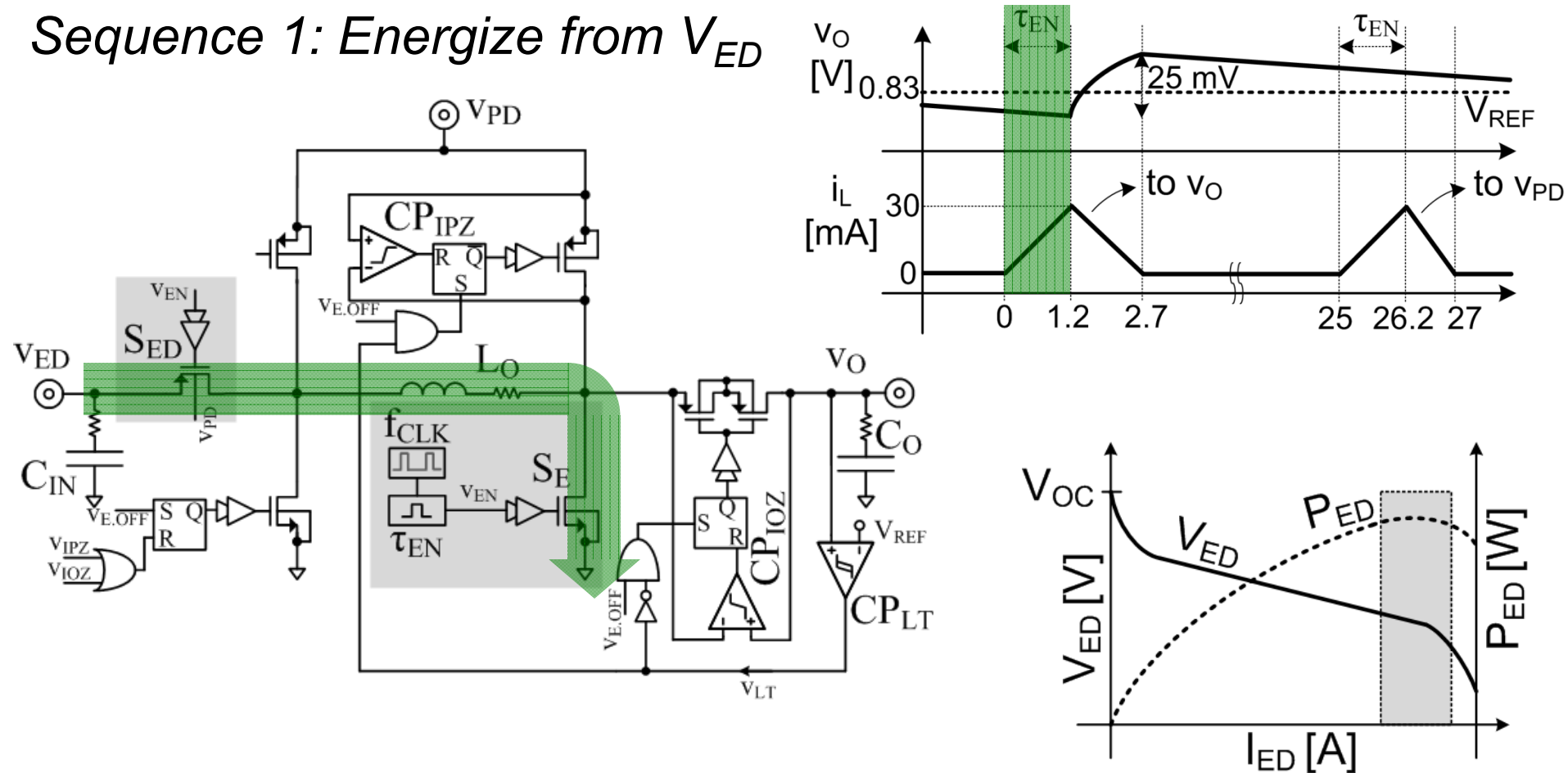
Mode Control:



- Hysteretic  $CP_M$  senses  $v_O$  ( $\Delta V_{HYST} > CP_{LT}$ )
  - ✓ Light  $\rightarrow$  Heavy :  $v_O \downarrow < V_{TH.L}$
  - ✓ Heavy  $\rightarrow$  Light :  $v_O \uparrow > V_{TH.H}$
- $\downarrow$  Complexity than Sensing  $i_O$

# Light Mode: (1) Energize from $v_{ED}$

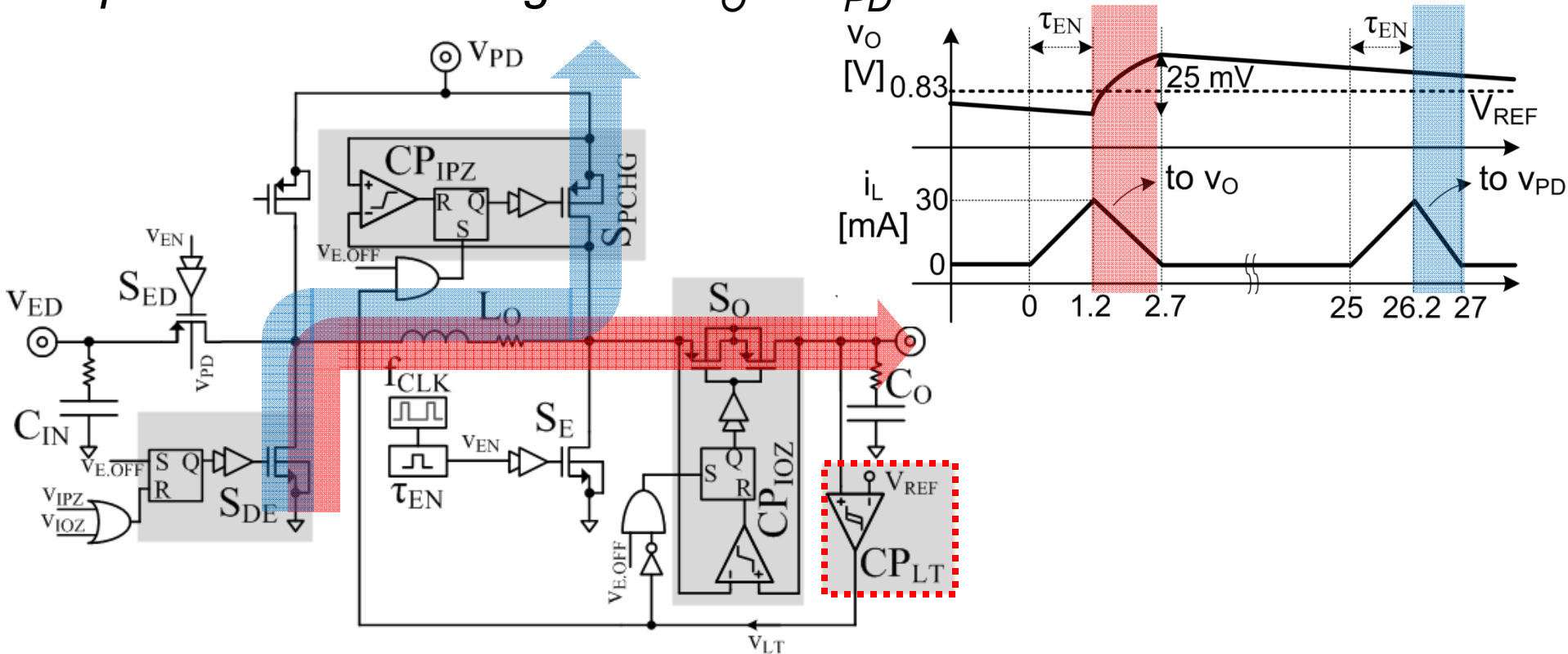
Sequence 1: Energize from  $V_{ED}$



- Starts from the rising edge of  $f_{CLK}$  (40kHz)
- Energize for the fixed  $\tau_{EN}$  to draw  $P_{ED}$
- ✓  $P_{ED}$  from the optimum/max power of the energy source

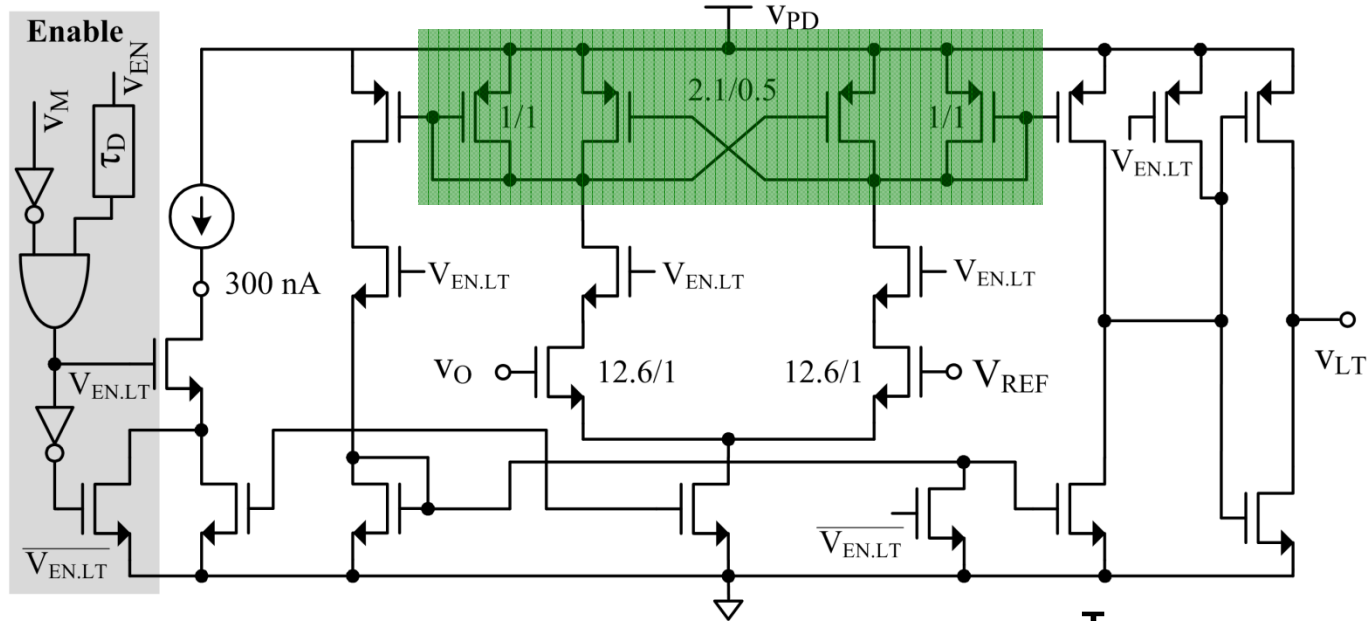
# Light Mode : (2) Supply $v_O$ / Recharge $v_{PD}$

Sequence 2: De-Energize to  $v_O$  or  $v_{PD}$

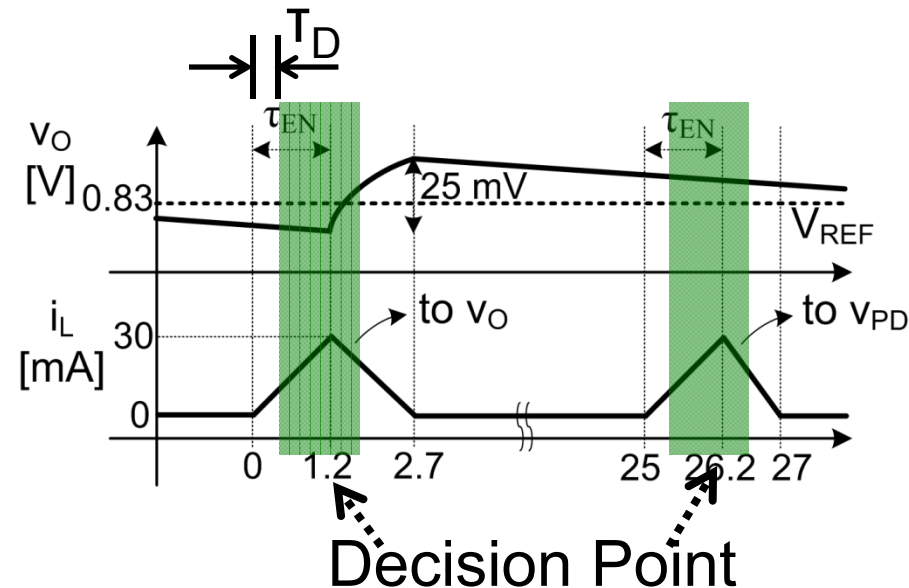


- At the end of  $\tau_{EN}$ : Check  $v_O$ 's level (Hysteretic  $CP_{LT}$ )
  - ✓ If  $v_{LT} \downarrow$ : Turn on  $S_O$  to supply  $v_O$
  - ✓ If  $v_{LT} \uparrow$ : Turn on  $S_{PCHG}$  to recharge  $v_{PD}$
- De-energize until  $i_L = \text{zero}$  (detected by  $CP_{IOZ}$  or  $CP_{IPZ}$ )

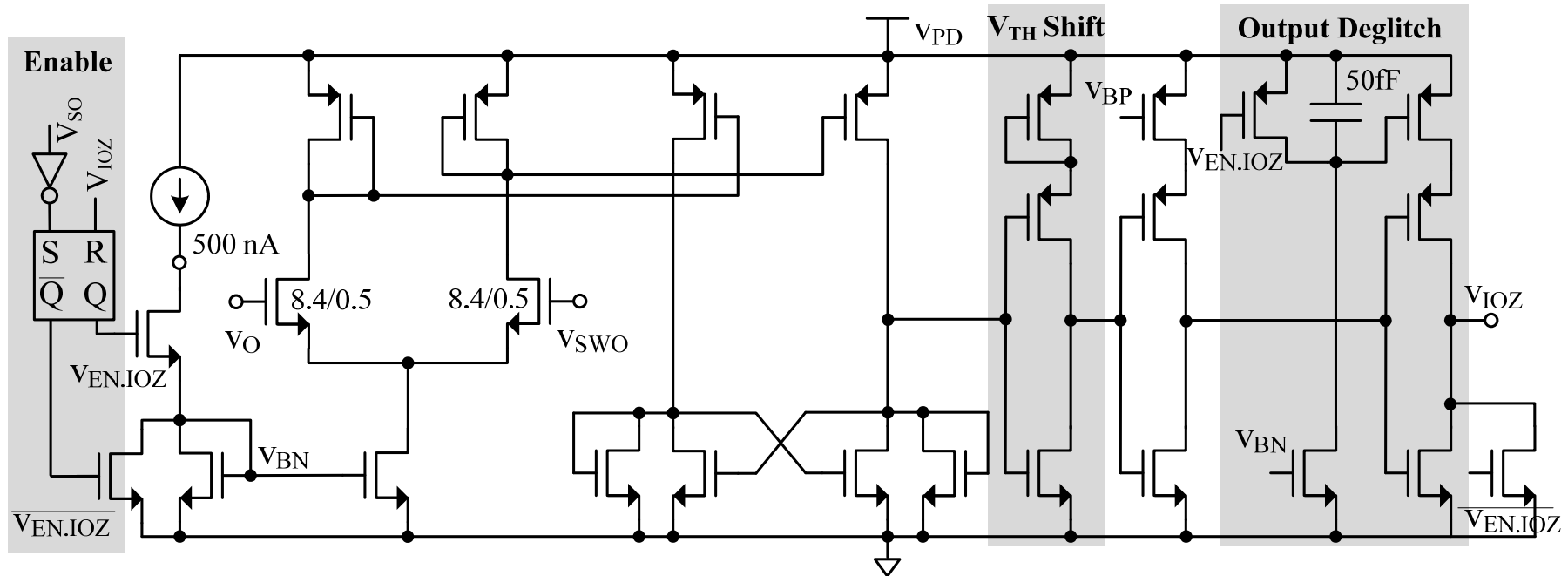
# Output Comparator $CP_{LT}$



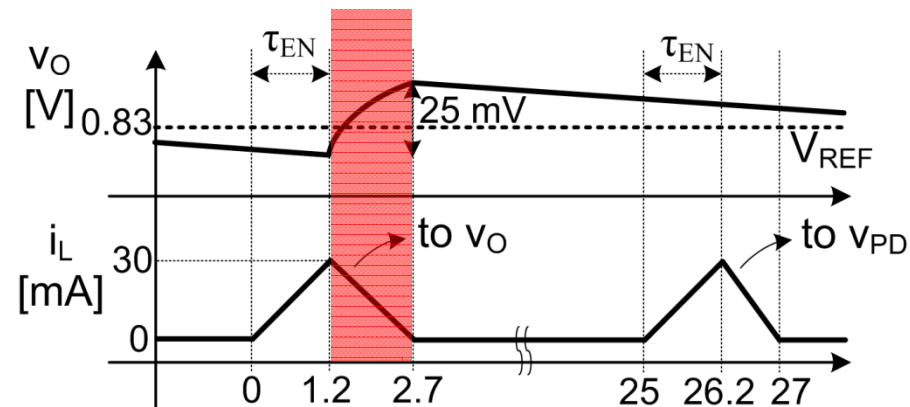
- $\Delta V_{HYST}$  by Latched TRs
- Duty-cycled to Save Power
  - ✓ ON at the end of  $\tau_{EN}$
  - ✓  $v_{EN}$  shifted by  $\tau_D$  to cover the moment



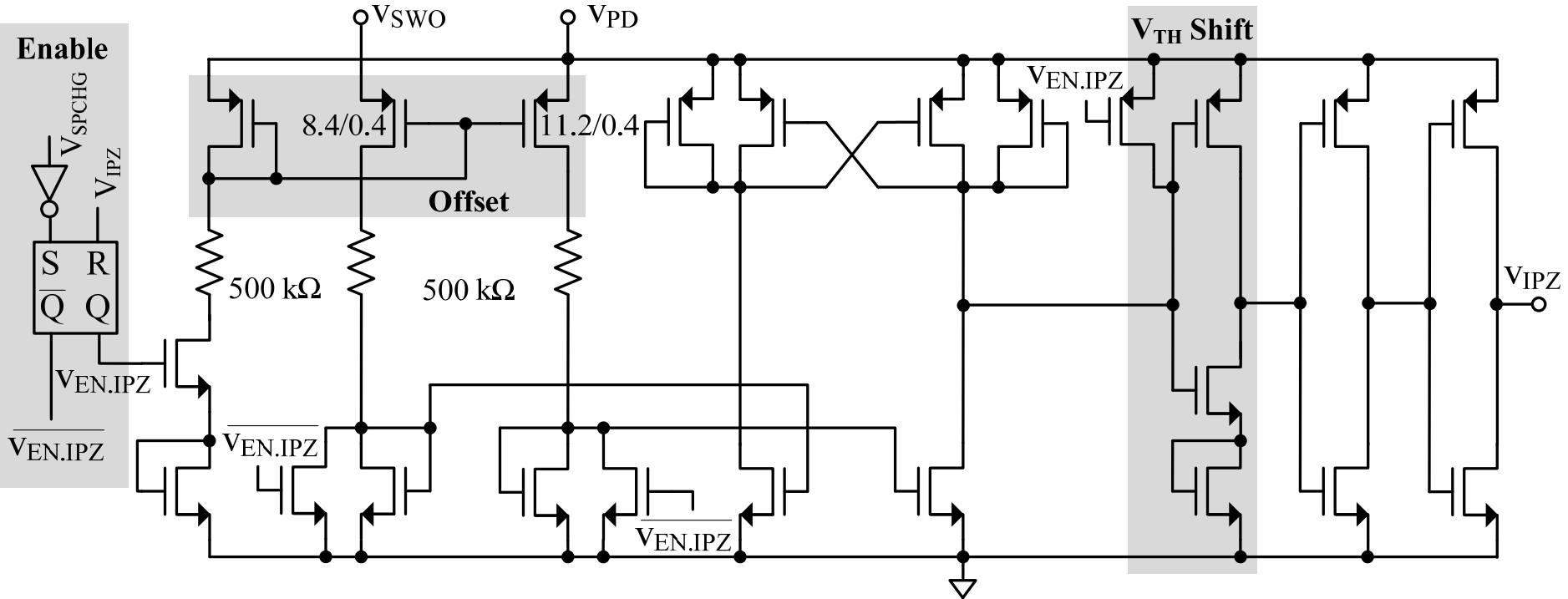
# Zero- $i_L$ -detect Comparator $CP_{IOZ}$



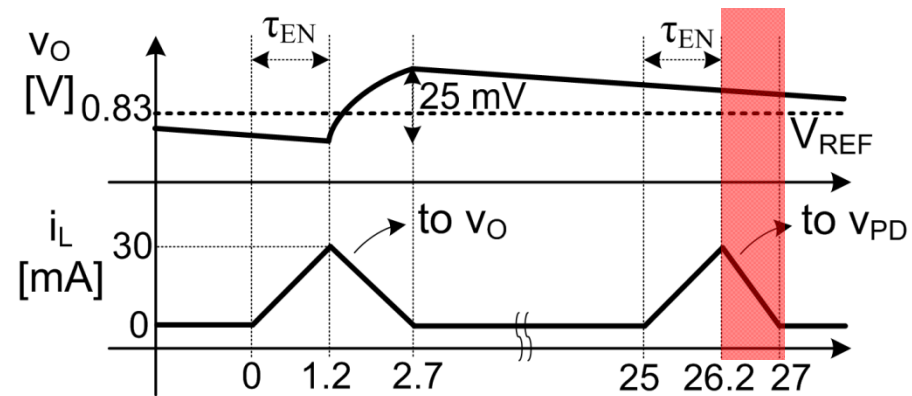
- Duty-cycled to Save Power
  - ✓ ON during  $S_O$  is on
  - ✓  $CP_{IOZ}$  turns off when it detects zero  $i_L$
- Output deglitched when Enable.



# Zero- $i_L$ -detect Comparator $CP_{IPZ}$

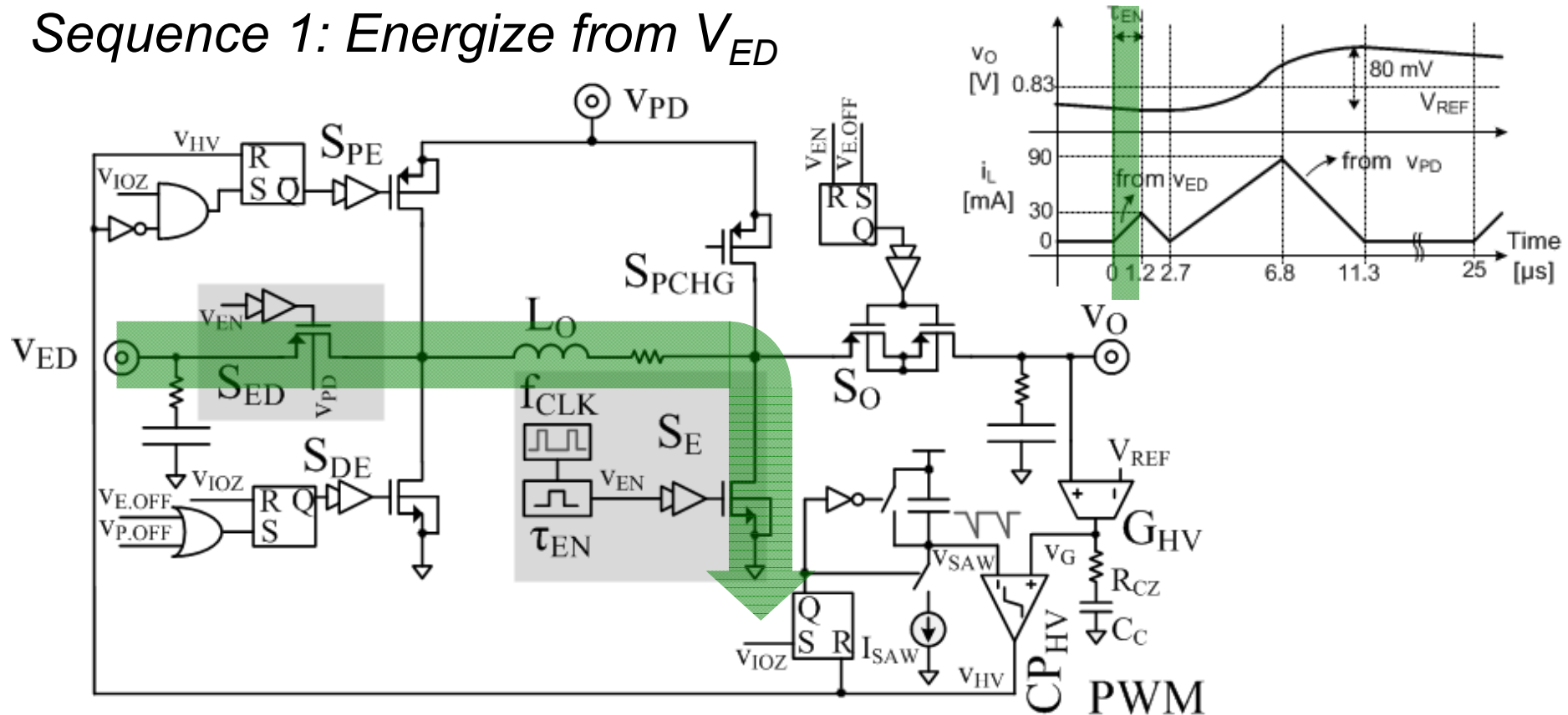


- Common-gate Input Pairs
- Intentional Offset to detect faster
- Duty-cycled to Save Power
  - ✓ ON during  $S_{PCHG}$  is on
  - ✓  $CP_{IPZ}$  turns off when it detects zero  $i_L$ .



# Heavy Mode: (1) Energize from $v_{ED}$

## Sequence 1: Energize from $V_{ED}$

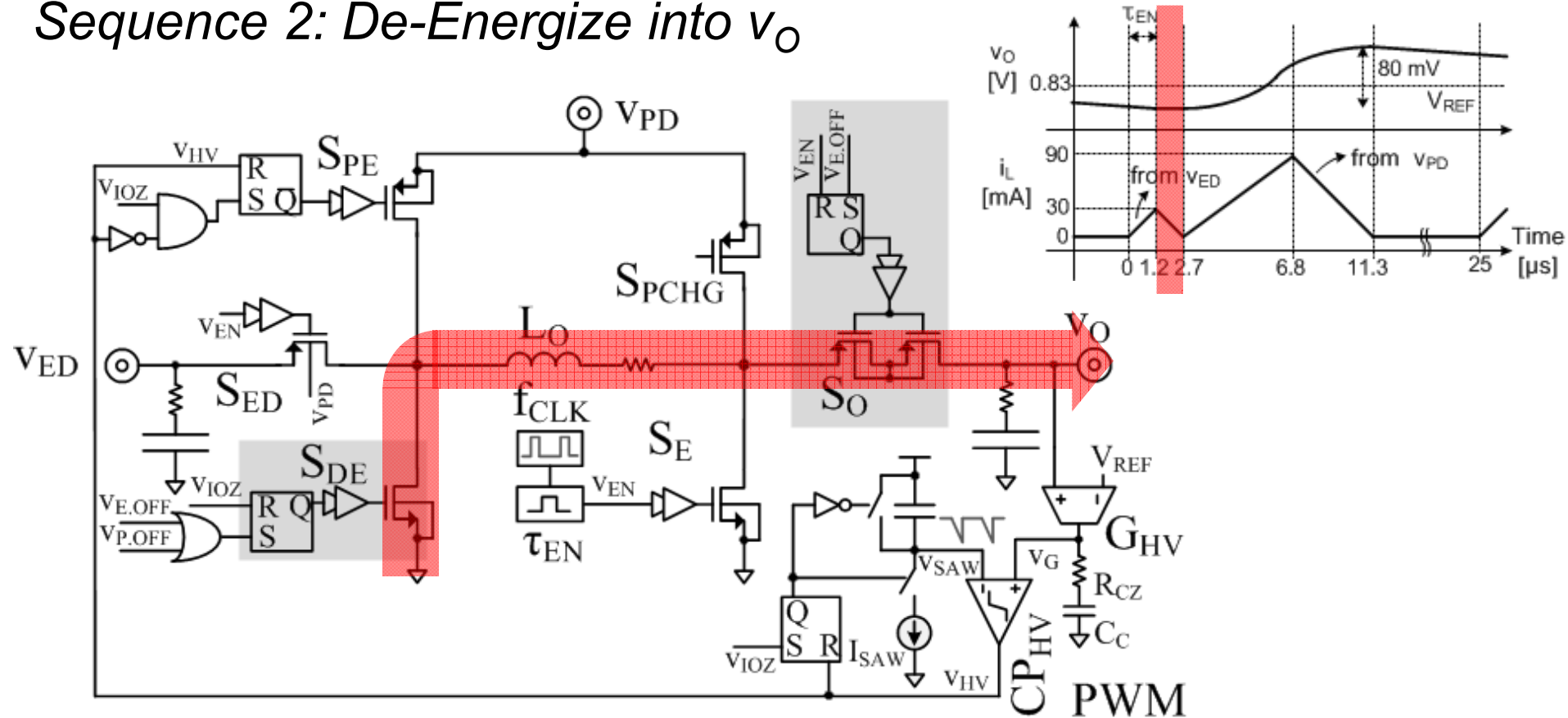


- Heavy Mode :  $P_O > \text{Energy sources' power } P_{ED}$
- Same sequence as Light Mode :
  - ✓ Starts from  $\uparrow$  edge of  $f_{CLK}$  (40kHz)
  - ✓ Energize for the fixed  $\tau_{EN}$  to draw  $P_{ED}$



# Heavy Mode: (2) Supply $v_O$

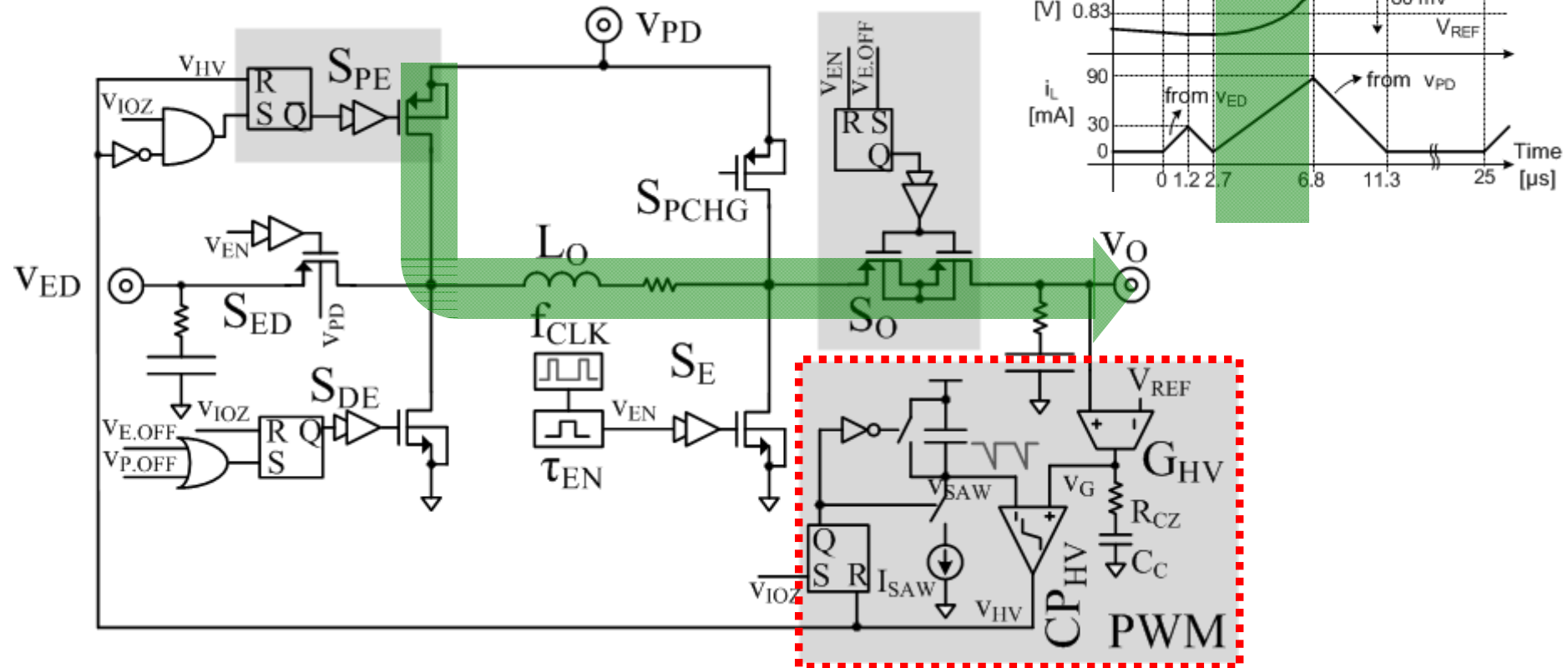
## Sequence 2: De-Energize into $v_O$



- De-energize to  $v_O$  only:
  - ✓ Because Load is heavy, no recharge power for  $v_{PD}$
- After  $V_{ED}$ 's cycle,  $v_O$  is still  $\downarrow$ 
  - The power source  $V_{PD}$  is needed!

# Heavy Mode: (3) Energize from $v_{PD}$

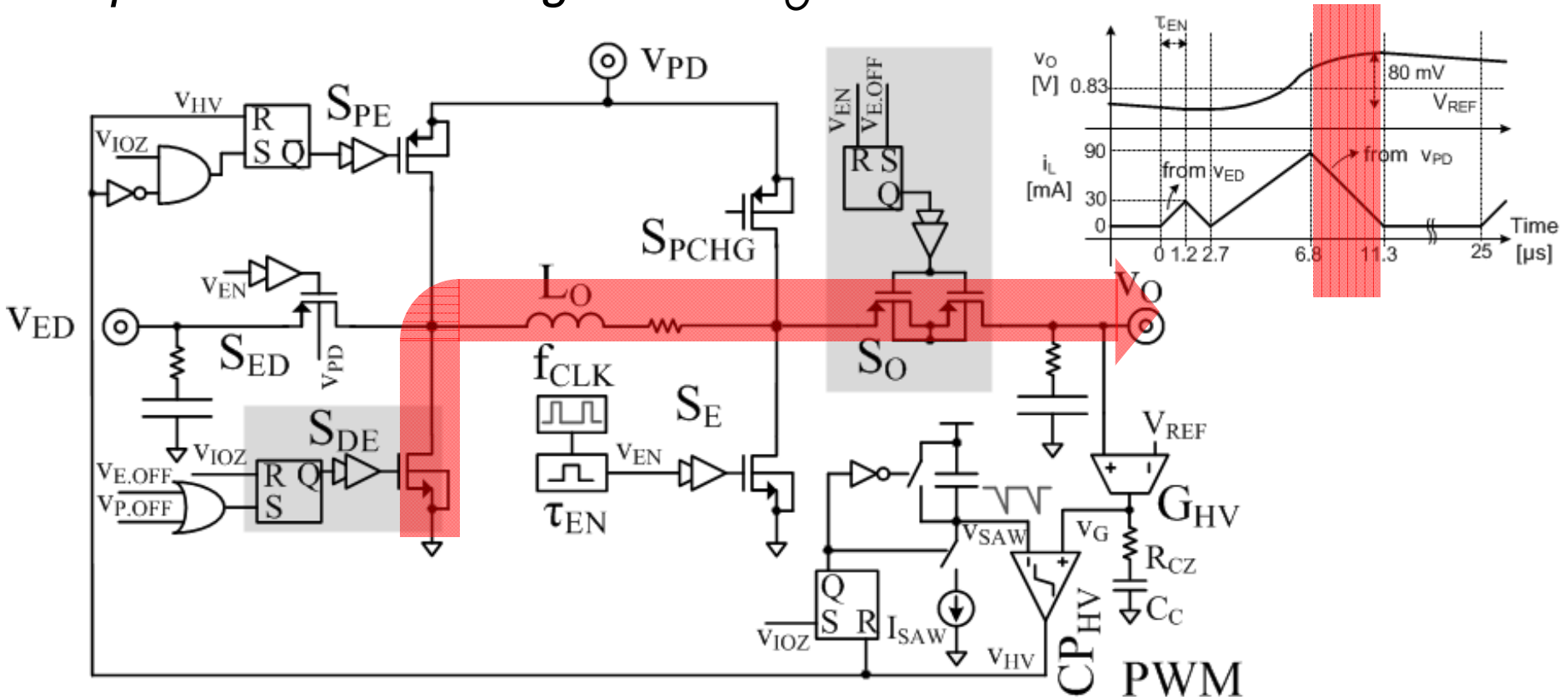
## Sequence 3: Energize from $V_{PD}$



- To supply  $\uparrow$  power to  $v_O$  with  $v_{PD}$ 's power
  - ✓ Controlled by PWM  $\rightarrow \updownarrow$  Power
  - ✓ Start energizing from  $v_{PD}$  after  $V_{ED}$ 's energy cycle
  - ✓ End when  $CP_{HV}$ 's output  $V_{HV} \uparrow$

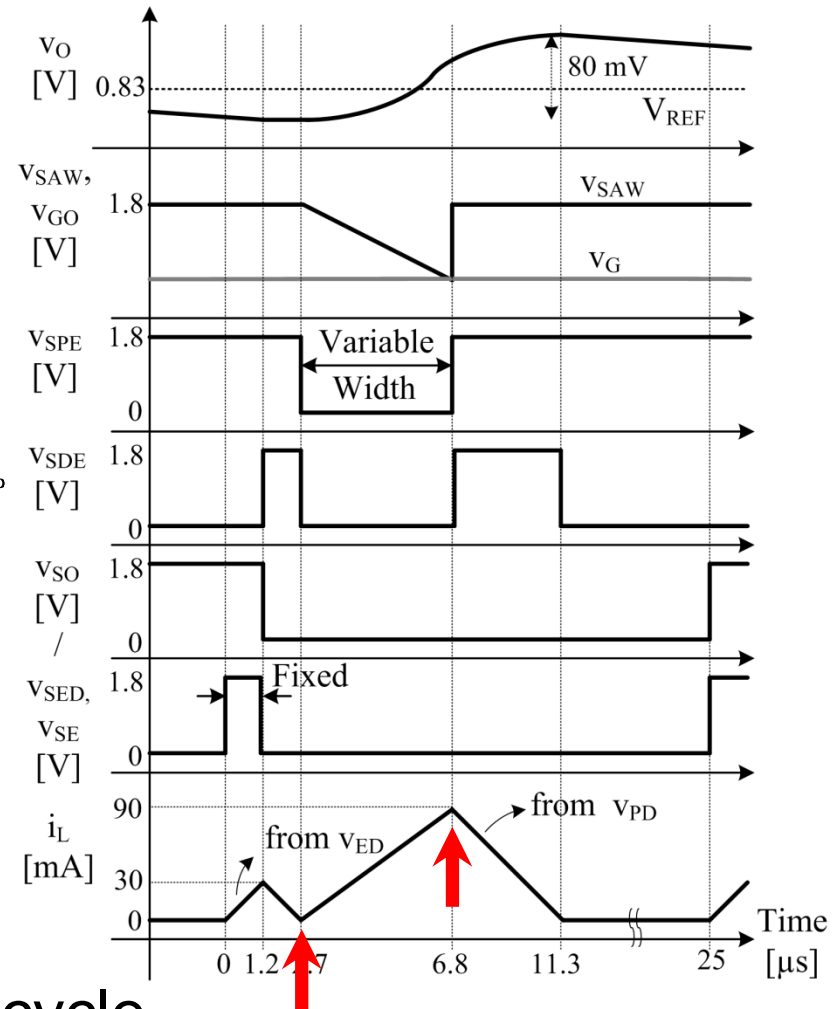
# Heavy Mode (4) Supply $v_O$


## Sequence 4: De-Energize into $v_O$



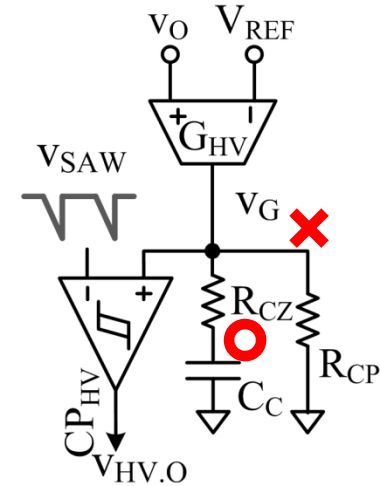
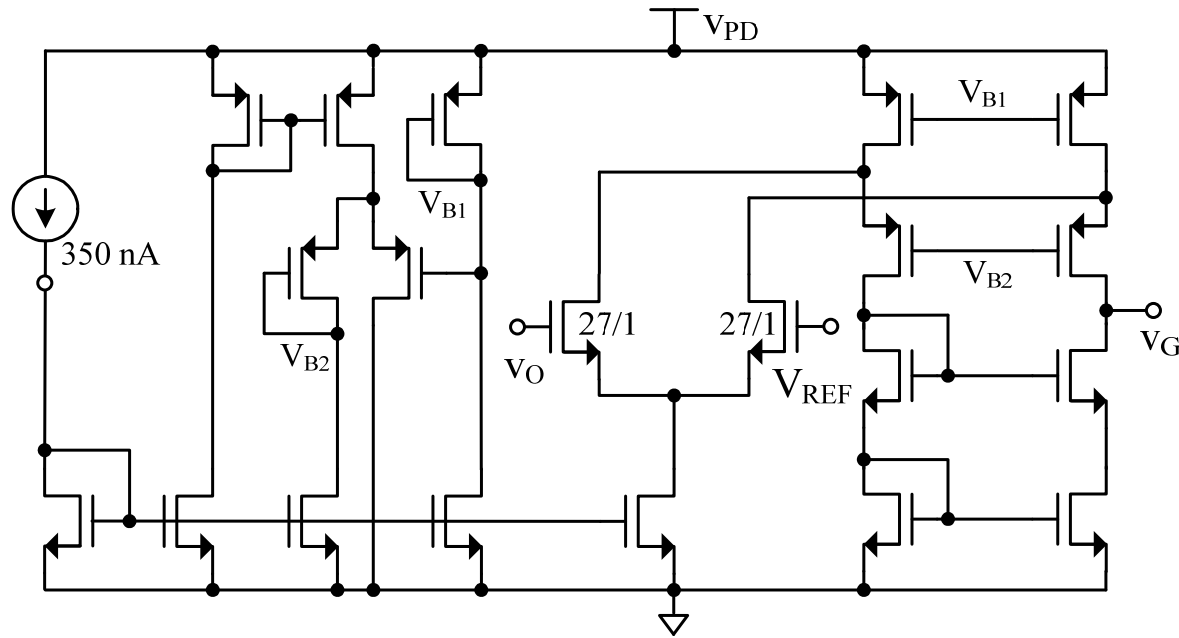
- Turn on  $S_{DE}$  to discharge  $L_O$  into  $v_O$
- All switches kept OFF until the next  $f_{CLK} \uparrow$

### PWM Operation for $V_{PD}$ 's $\uparrow$ Power



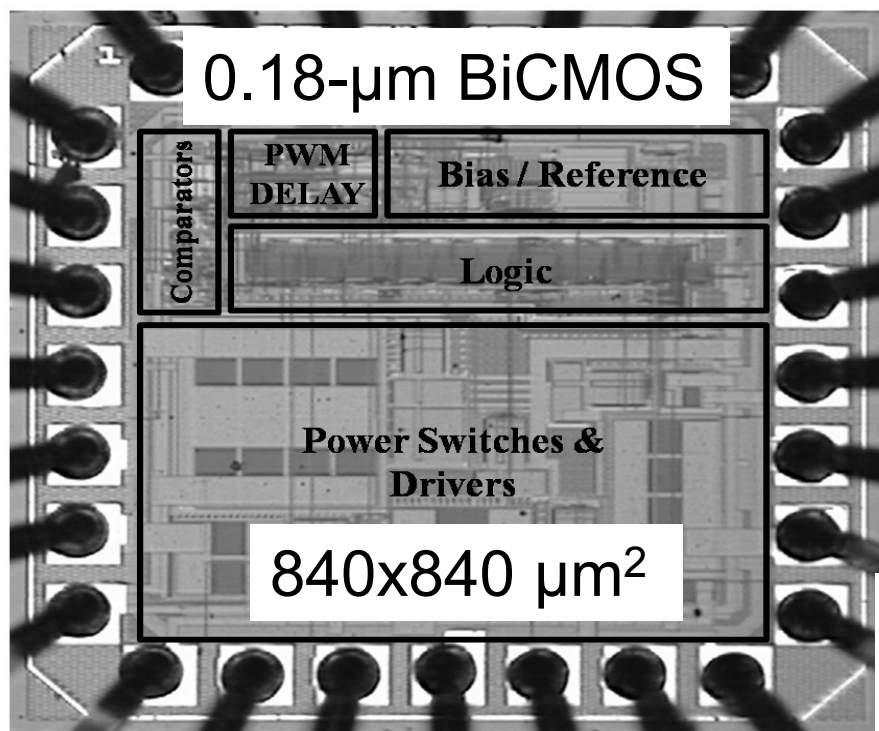
- Comparator  $CP_{HV} \rightarrow v_G$  VS  $v_{SAW}$ 
    - ✓  $v_{SAW}$  starts after  $v_{ED}$ 's energy cycle
    - ✓ Compensated  $v_G$  from Error amplifier  $G_{HV}$
  - When  $v_{HV} \uparrow \rightarrow$  Turns off  $S_{PE}$ , resets  $v_{SAW}$
- 

# Transconductance PWM Amplifier $G_{HV}$



- Folded-cascode structure,  $G_m = 2.5 \mu S$
  - Overall loop gain  $A_{OL} \big|_0 \approx 43 \text{ dB}$
  - Compensation:
    - ✓ System's Dominant Pole at  $v_G$
    - ✓ Insert a zero to cancel the second pole at  $v_O$
- $PM \approx 90 \text{ degrees}$ , stable.

# Die Photo and PCB Prototype



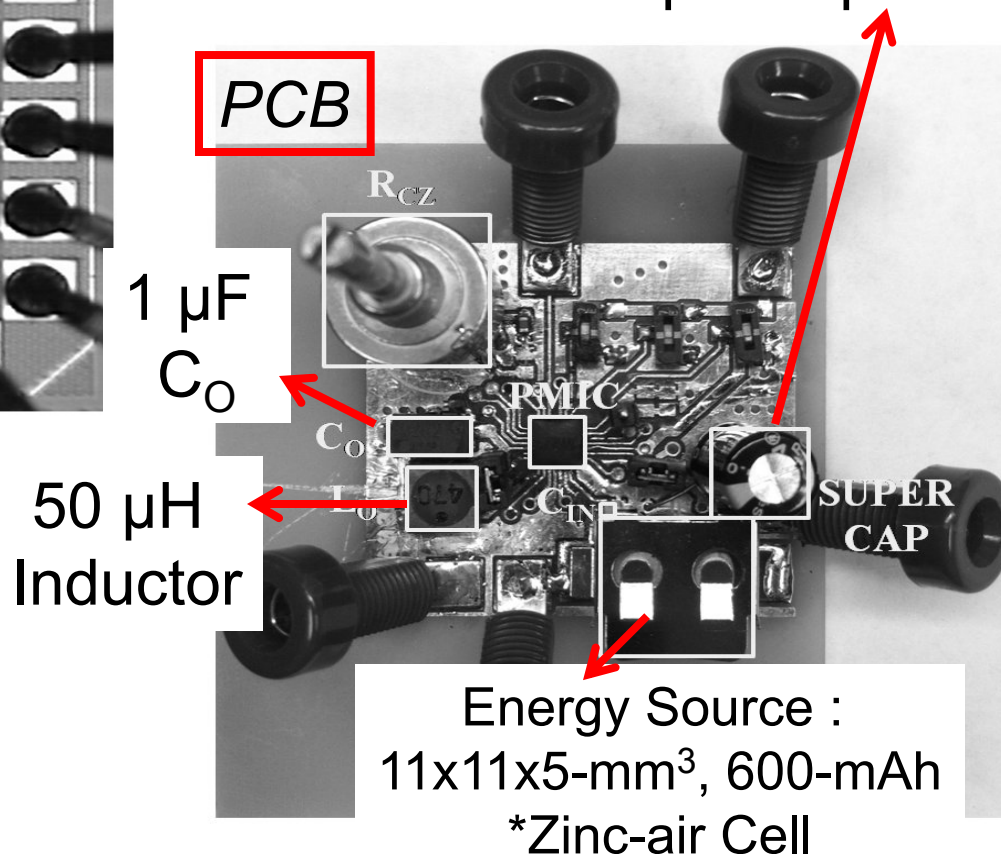
*Die Photo*

\*Zinc-air Cell: Hearing-Aids

- ✓ Fuel Cell-like Battery
- ✓ Use Air as fuel
- ✓ As a test vehicle

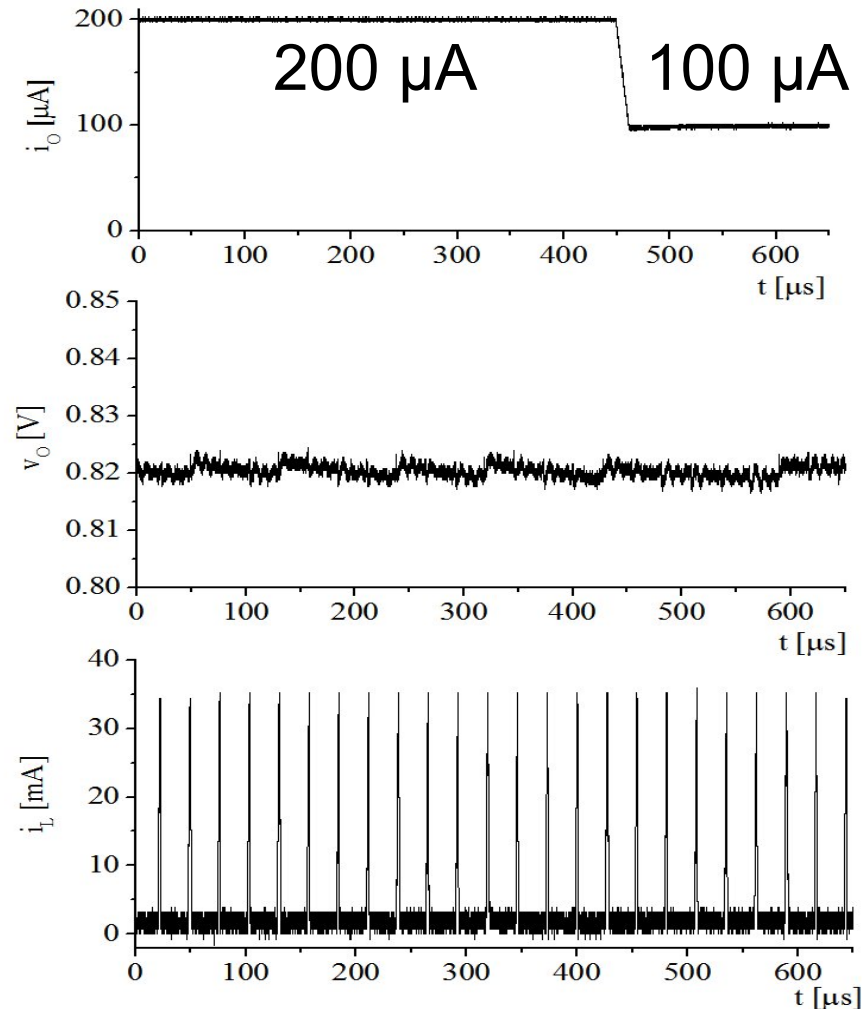
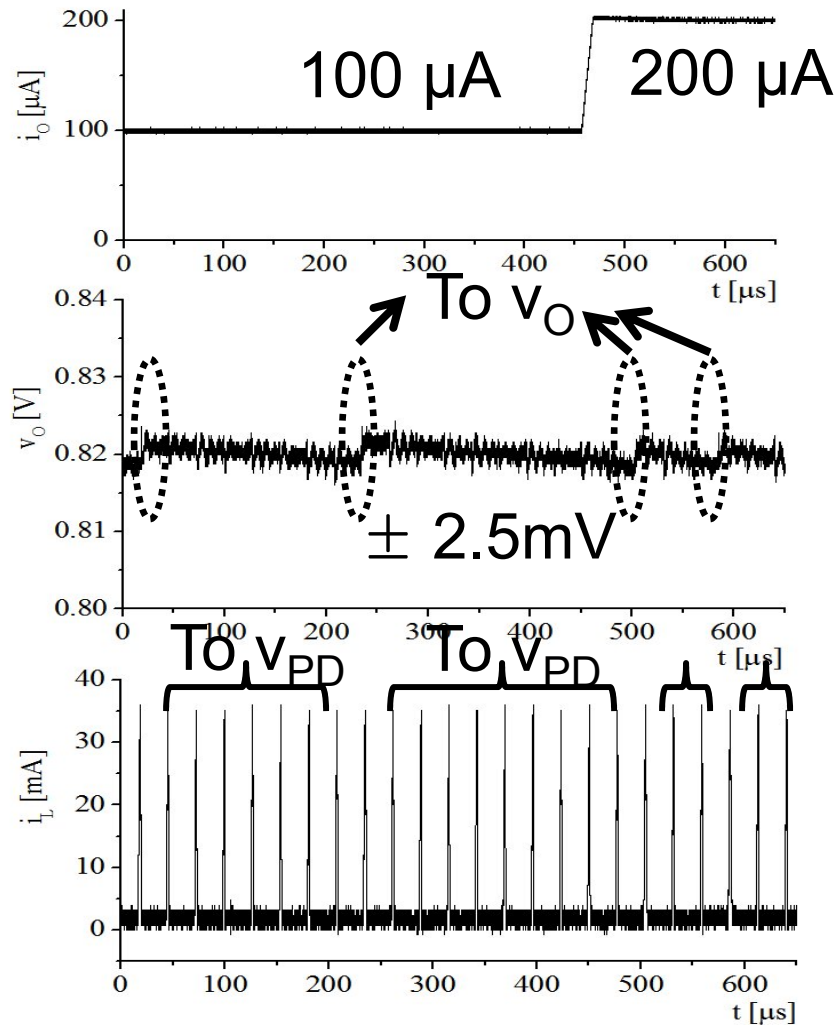


Power Source :  
8x8x12-mm<sup>3</sup> 1-F  
super capacitor





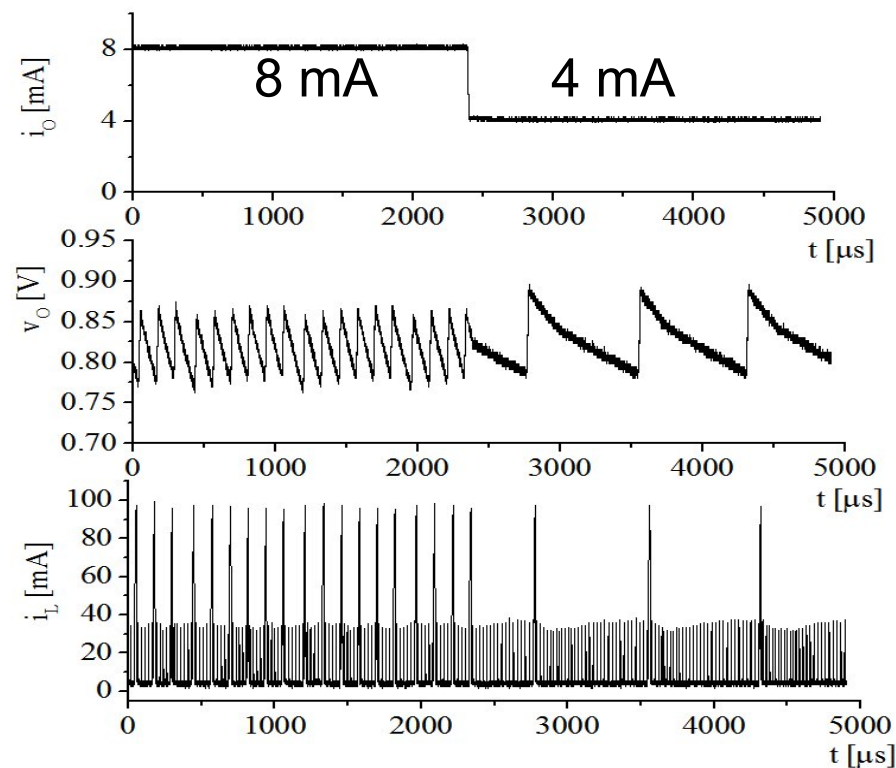
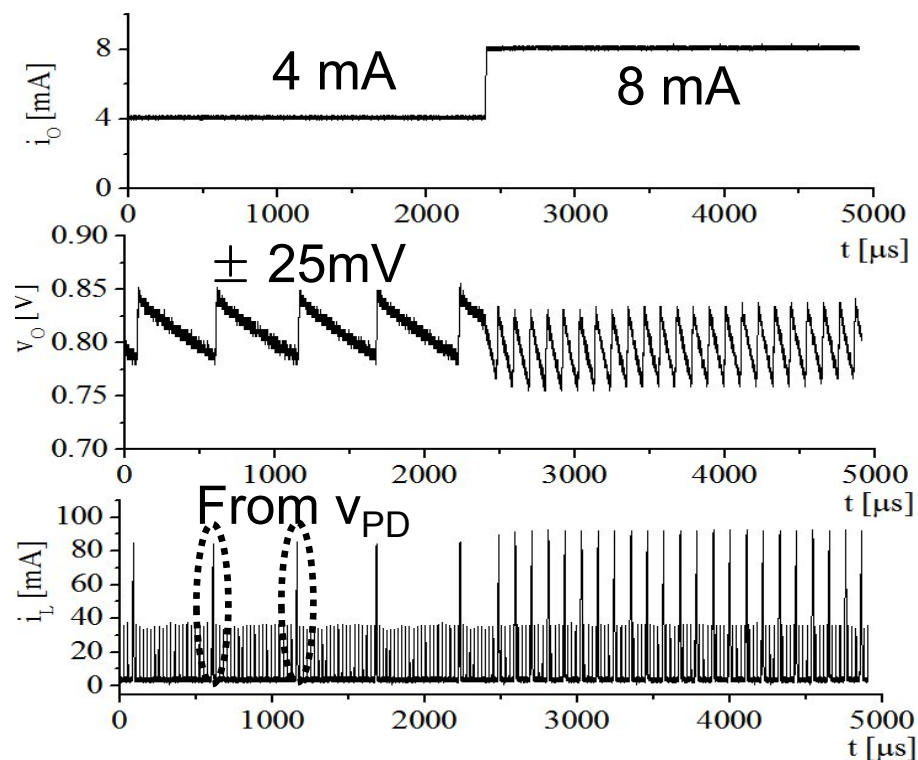
# Regulation Performance in Light Mode



## ■ Regulation within Light Mode

✓  $< 0.2\%$  DC variations @  $i_o = 100\ \mu\text{A} \leftrightarrow 200\ \mu\text{A}$

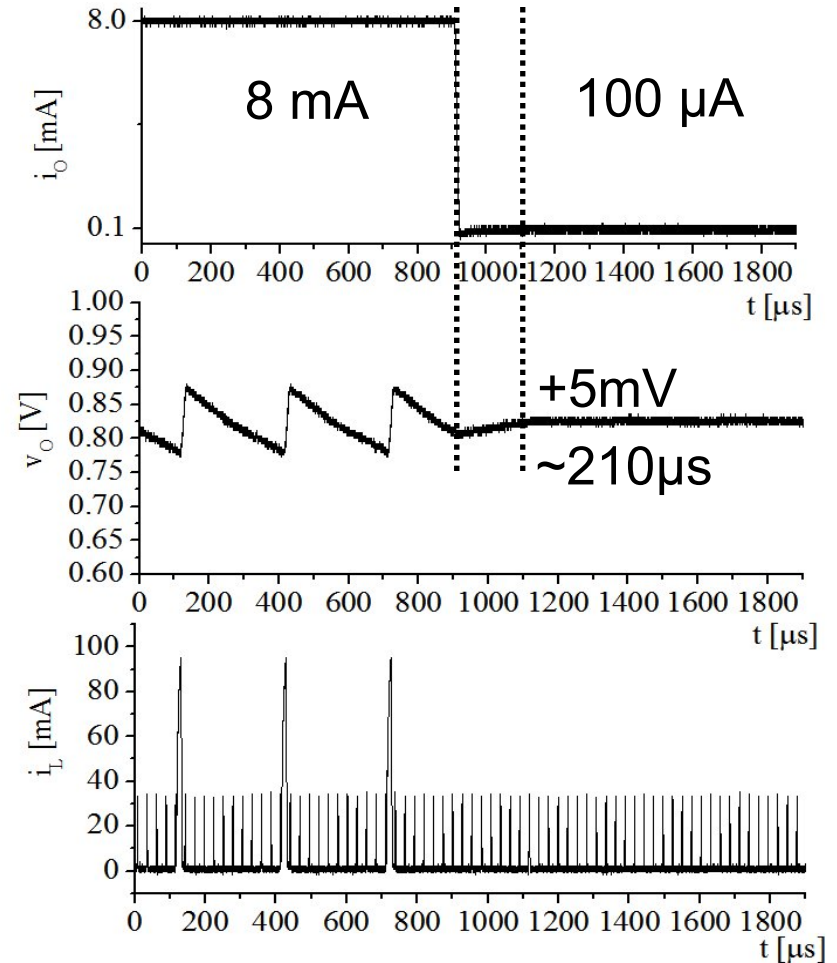
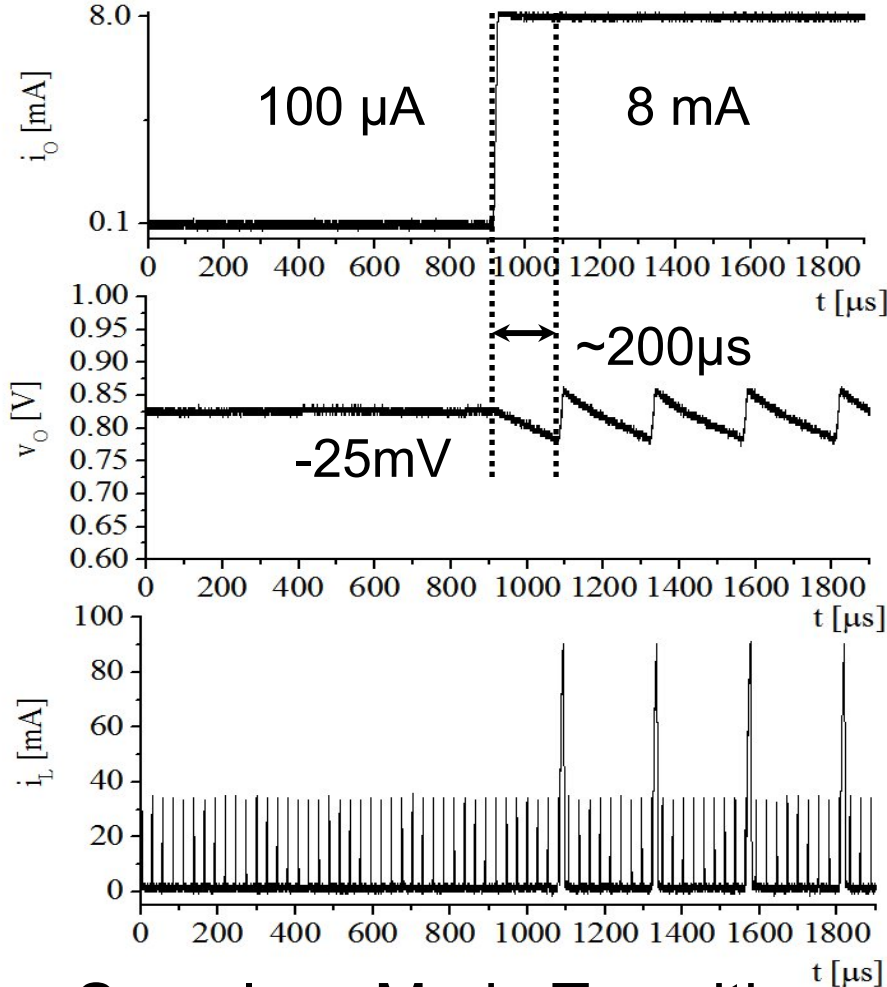
# Regulation Performance in Heavy Mode



- Regulation within Heavy Mode
  - ✓  $< 2.5\%$  DC variations @  $i_o = 4\text{ mA} \leftrightarrow 8\text{ mA}$
  - ✓  $\Delta v_o = \pm 25\text{ mV} \rightarrow$  Due to  $\uparrow$  energy packet from  $v_{PD}$

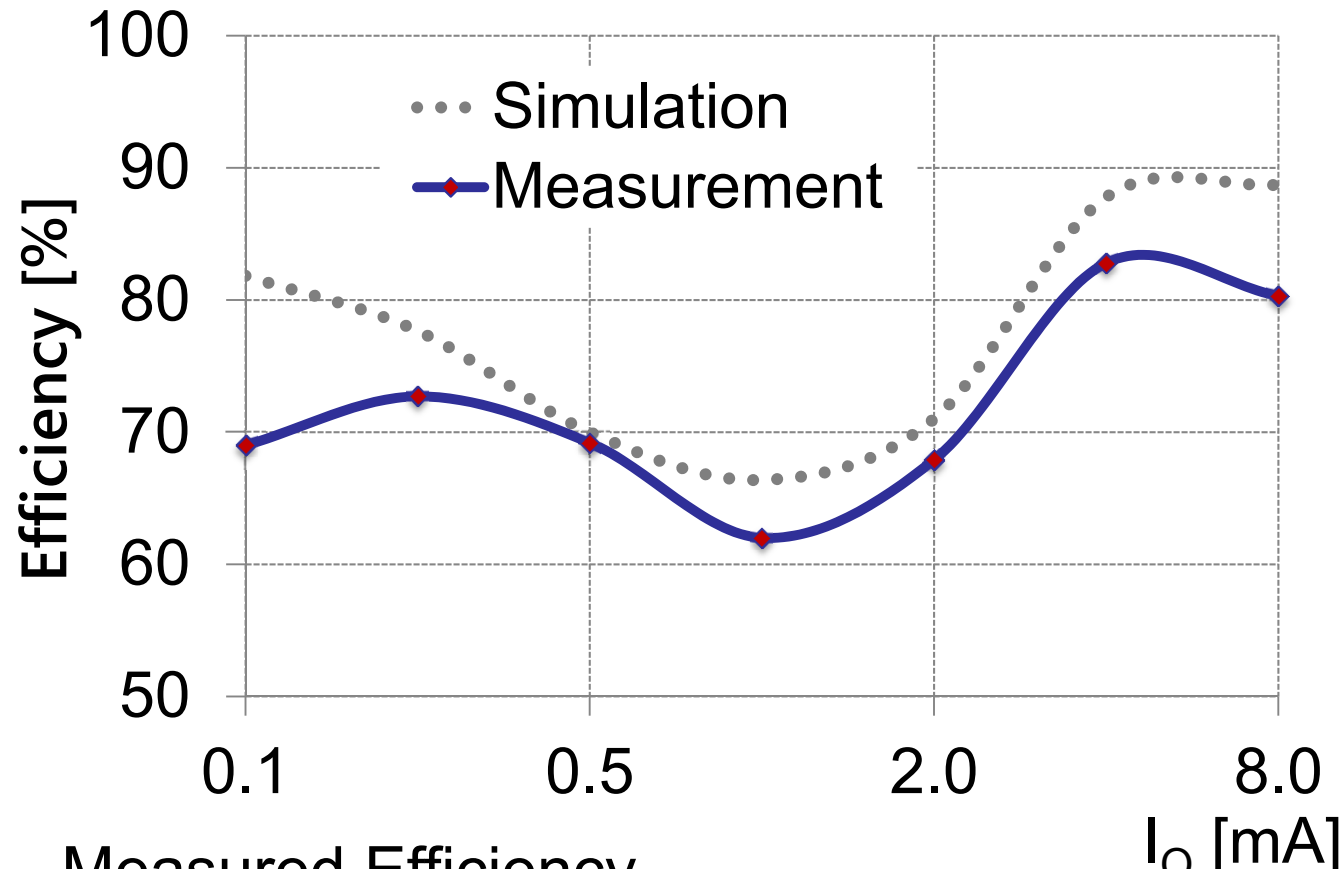


# Mode Transitions



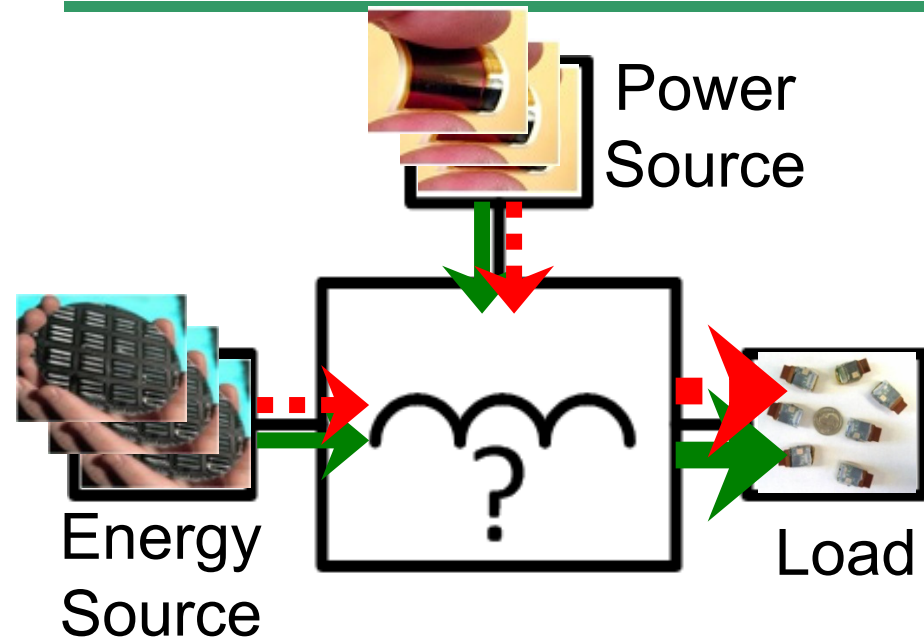
- Seamless Mode Transitions @  $i_o = 0.1 \leftrightarrow 8 \text{ mA}$
- Indirect  $i_o$  sensing from  $v_o$  (Hysteretic  $\text{CP}_M$ )  
 $t_{HL}, t_{LH} = f(C_O, i_o) \rightarrow \text{Slow, but } \downarrow \text{ complexity}$

# Efficiency Performance

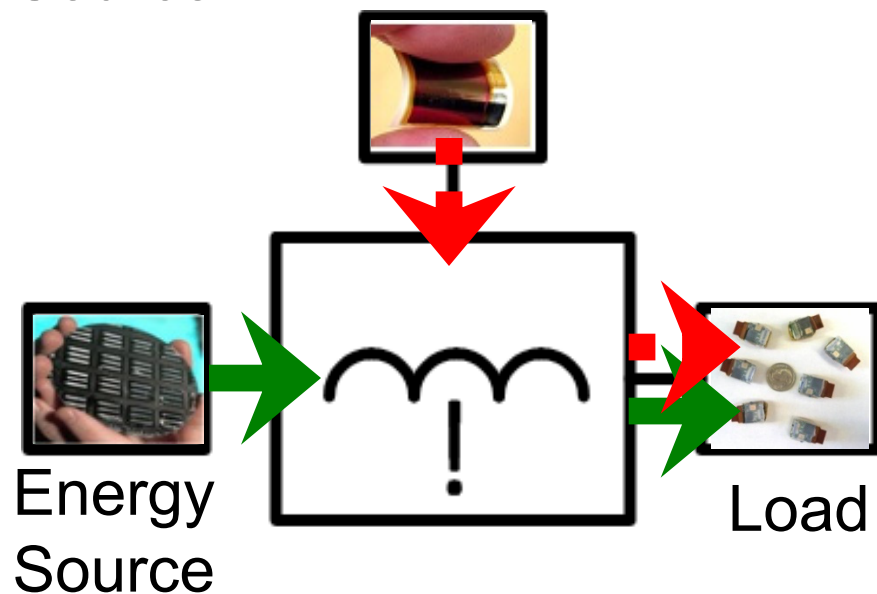


- Measured Efficiency ...
  - ✓ Peaked at 83% @  $i_O = 4$  mA
  - ✓  $\downarrow \eta$  @  $i_O = 1$  mA, due to  $\uparrow$  Gate-drive losses
  - ✓ Simulation VS Measurement :  
 $\downarrow I_{BIAS} \rightarrow \uparrow \tau_{EN} \rightarrow \uparrow i_{L(PK)} \rightarrow \uparrow$  Conduction losses

# Load-dependent Source-selection Control



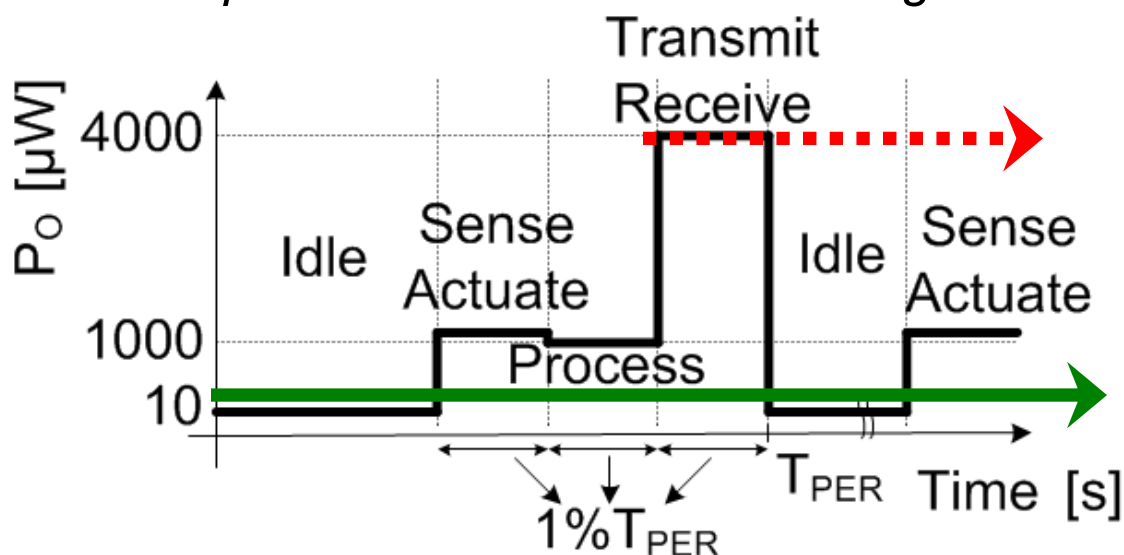
Without Load-Dependent  
Source-Selection control,  
→  $V_{ED}$  Oversized for  $P_{O.PEAK}$ ,  
Or  
→  $V_{PD}$  Oversized for  $t_{1-MONTH}$



With Load-Dependent  
Source-Selection control,  
→  $V_{ED}$  for  $t_{1-MONTH}$   
→  $V_{PD}$  for  $P_{O.PEAK}$   
→ *Optimum Use of Sources!*

# Example Load Profile

To estimate the required Sources' Volume / Weight



Functions	Power	Duty
Sense / Actuate	1200 $\mu\text{W}$	1 %
Process	1000 $\mu\text{W}$	1%
Transmit / Receive	4000 $\mu\text{W}$	1%
Idle	10 $\mu\text{W}$	97 %
Average	72 $\mu\text{W}$	100%

*\*Halgamuge, Progress in Electromagnetics Research B 2009*

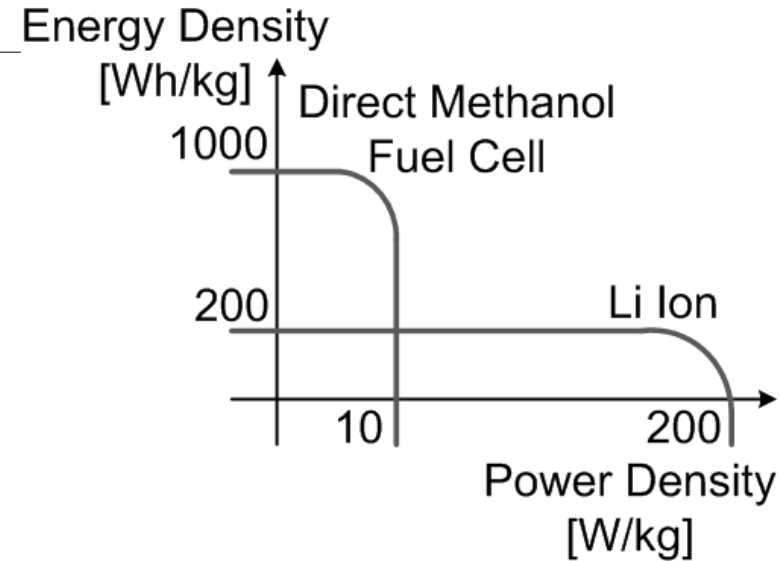
# Calculation of Required Sources

## DMFC for $p_{O.AVE}$ , 1-MONTH

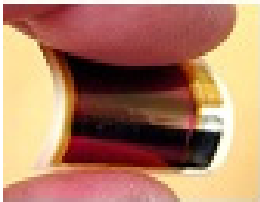


$$W_{FC} = \frac{(\text{Total Energy})}{(\text{Energy Density})_{FC}}$$

$$= \frac{P_{O(AVG)} t_{1\text{-MONTH}}}{\eta_{C(AVG)} ED_{FC}}$$



## Li Ion for $p_{O.PEAK}$



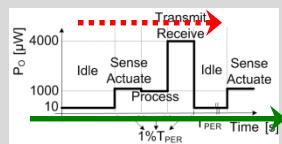
$$W_{LI} = \frac{(\text{Peak Power})}{(\text{Power Density})_{LI}}$$

$$= \frac{P_{O(PEAK)}}{\eta_{C(PEAK)} PD_{LI}}$$

$$W_{TOT} = W_{FC} + W_{LI} \ll W_{FC.ONLY} \text{ or } W_{LI.ONLY}$$

# Performance Comparison Table

	Huang, JSSC 09	Qiu, ISSCC 11	Chew, ISSCC 13	Kim, AICSP 12	This work
$\eta_{0.1\text{mW}}$ / $\eta_{\text{PEAK}}$	80% / 93%	83% / 87%	83% / 83%	4% / 32%	70% / 83%
*LD/SS Control	x	x	x	o	o
Sources required to supply the load	430-mg DMFC Or 326-mg Li Ion	460-mg DMFC Or 314-mg Li Ion	482-mg DMFC Or 314-mg Li Ion	1.3-g DMFC + 63-mg Li Ion = 1363 mg	74.5-mg DMFC + 24-mg Li Ion = 98.6 mg <b>&lt; 32% of SoAs</b>

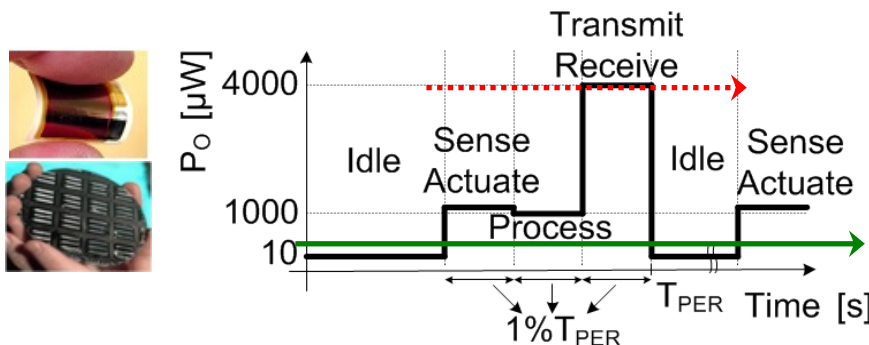


\* Load-dependent Source-Selecting Control

# Conclusions

- This IC Selectively draws power from hybrid sources
  - ✓  $p_{O.AVE}$  from Energy-dense source
  - ✓  $p_{O.PEAK}$  from Power-dense source

→ To optimize sources' volume for  $\uparrow p_{O.PEAK} / p_{O.AVE}$
- Peak  $\eta$  of 83% in 0.1-8mA's  $i_o$
- Reduction in sources' weight:  
< 32% for a  $\uparrow p_{O.PEAK} / p_{O.AVE}$  sensor load



# **An Energy Pile-up Resonance Circuit Extracting Maximum 422% Energy from Piezoelectric Material in a Dual-Source Energy-Harvesting Interface**

**Young-Sub Yuk, Seungchul Jung, Hui-Dong Gwon, Sukhwan Choi, Si  
Duk Sung, Tae-Hwang Kong, Sung-Wan Hong, Jun-Han Choi, Min-Yong  
Jeong, Jong-Pil Im, Seung-Tak Ryu, Gyu-Hyeong Cho**

**KAIST, Republic of Korea**

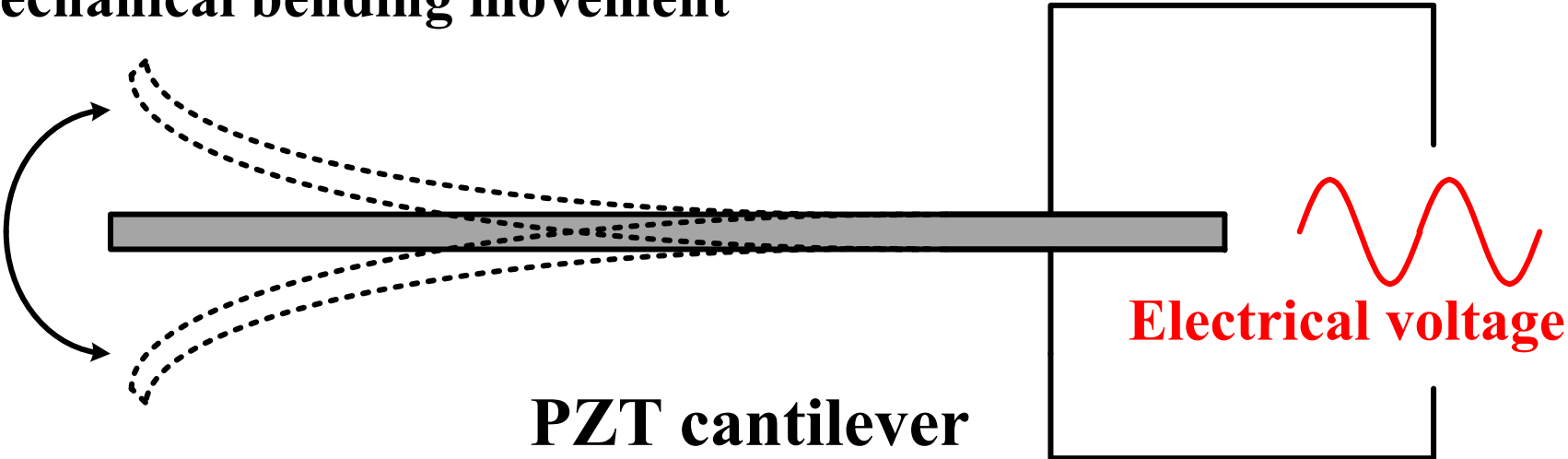


- **Introduction about the Piezoelectric Transducer (PZT)**
- **The Previous works for Energy Extraction from PZT**
- **A Proposed Energy Pile-up Resonance Circuit**
- **Chip Implementation**
- **Measurement Results**
- **Conclusion**

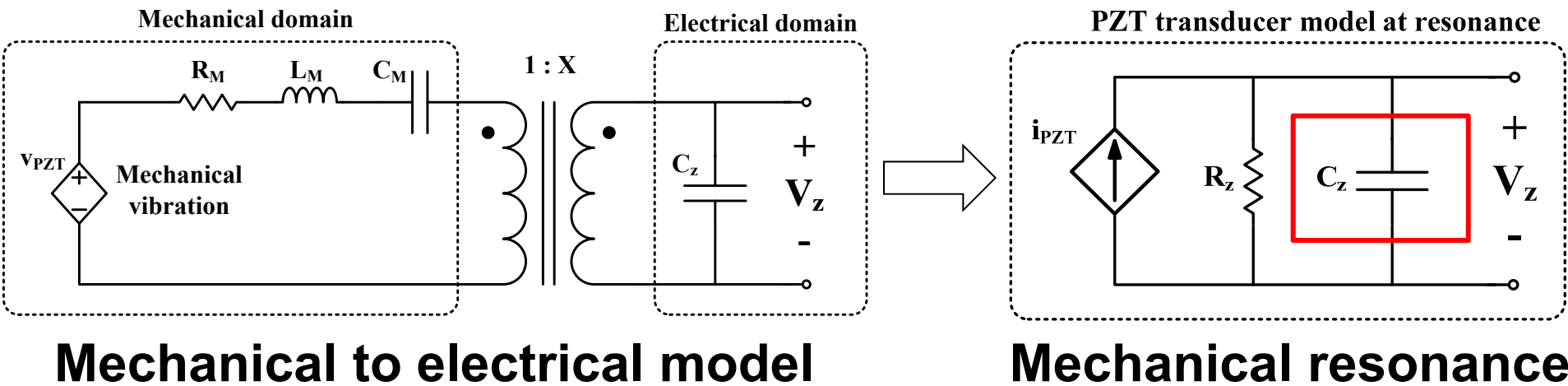
- **Introduction about the Piezoelectric Transducer (PZT)**
- The Previous works for Energy Extraction from PZT
- A Proposed Energy Pile-up Resonance Technique
- Chip Implementation
- Measurement Results
- Conclusion

# Electrical Modeling of the PZT

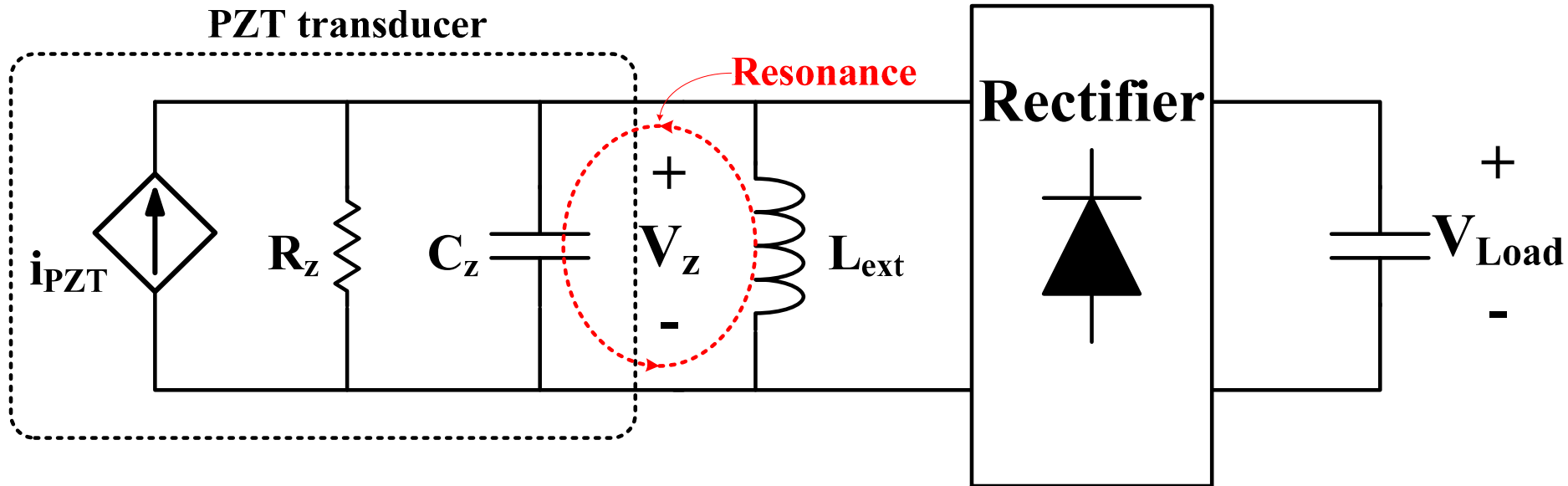
## Mechanical bending movement



PZT cantilever



# Ideal Resonance Technique for PZT



$$L_{ext} = \frac{1}{(2\pi f_r)^2 \cdot C_z}$$

- The  $C_z$  is 220 nF and mechanical resonance  $f_r$  is 100 Hz
- The required external inductor is 11.5 H
- **Too much large inductor is required!**

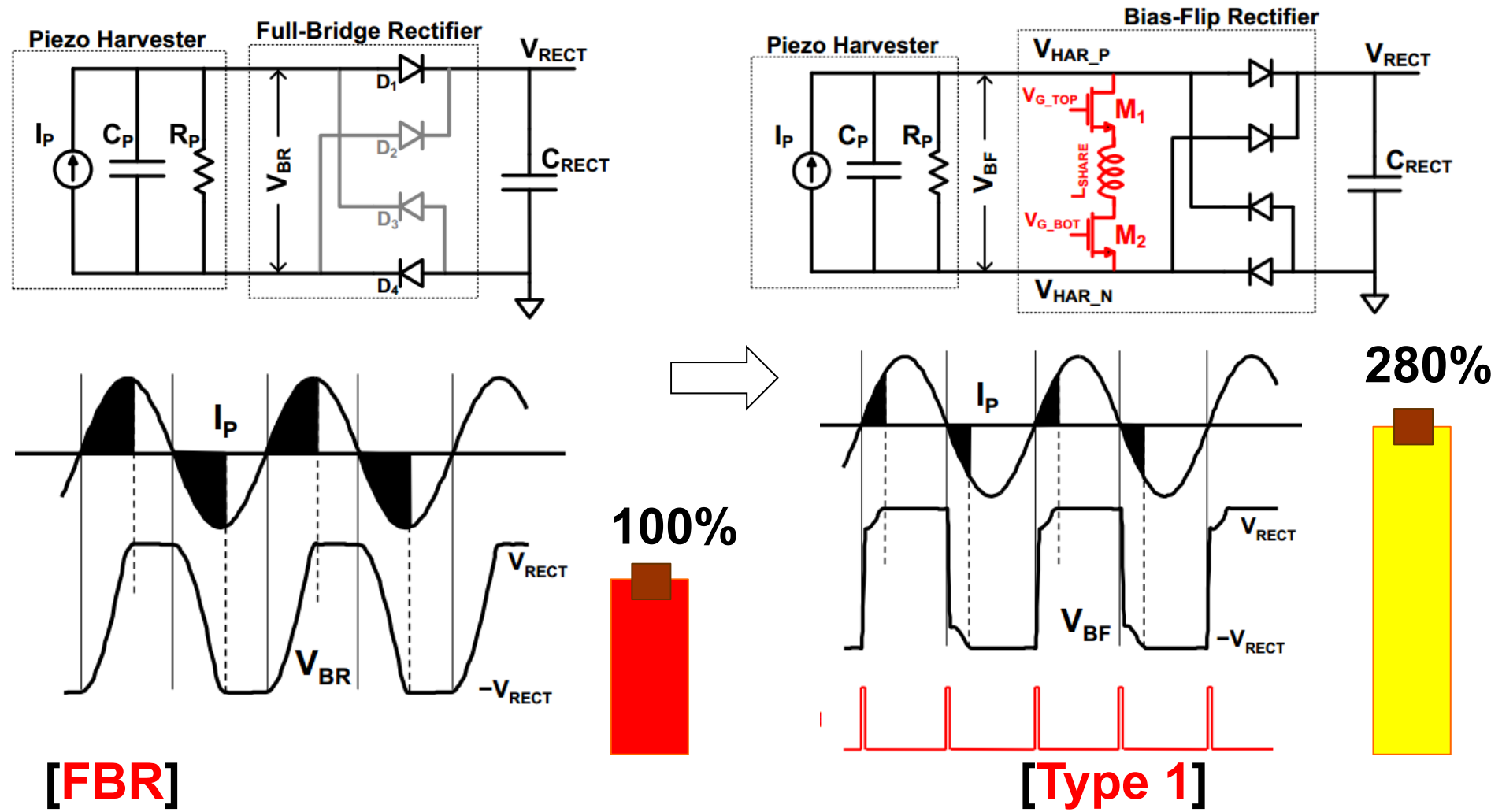
# Contents

---

- Introduction about the Piezoelectric Transducer (PZT)
- **The Previous works for Energy Extraction from PZT**
- A Proposed Energy Pile-up Resonance Technique
- Chip Implementation
- Measurement Results
- Conclusion

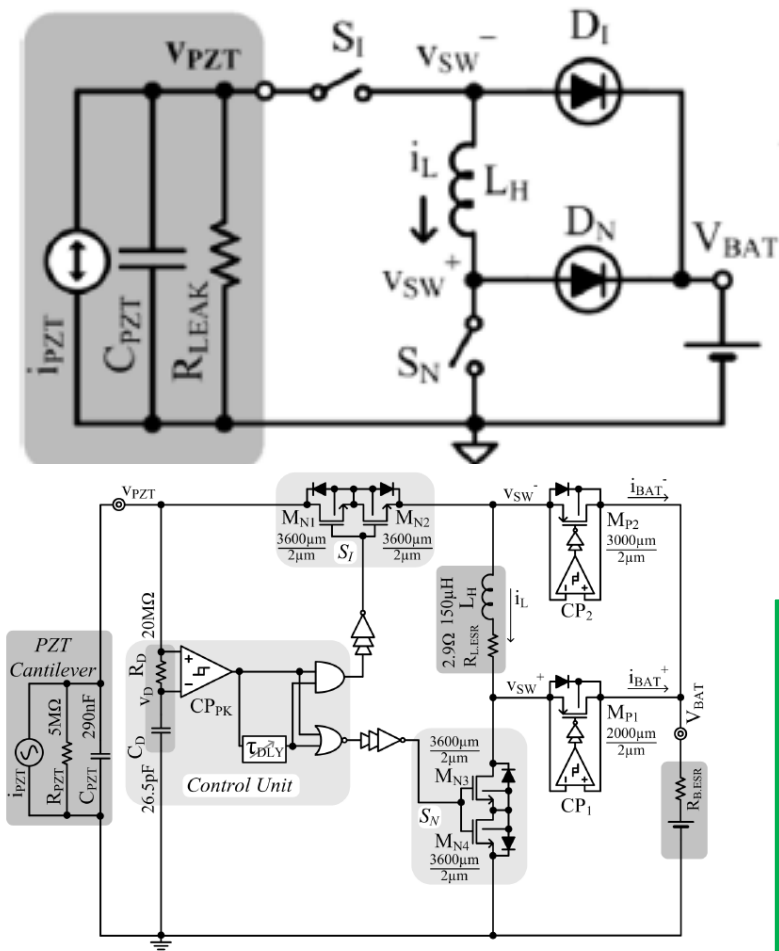
# Previous work [1]

## An Efficient Piezoelectric Energy Harvesting Interface Circuit Using A Bias Flip Rectifier and Shared Inductor, ISSCC 2009



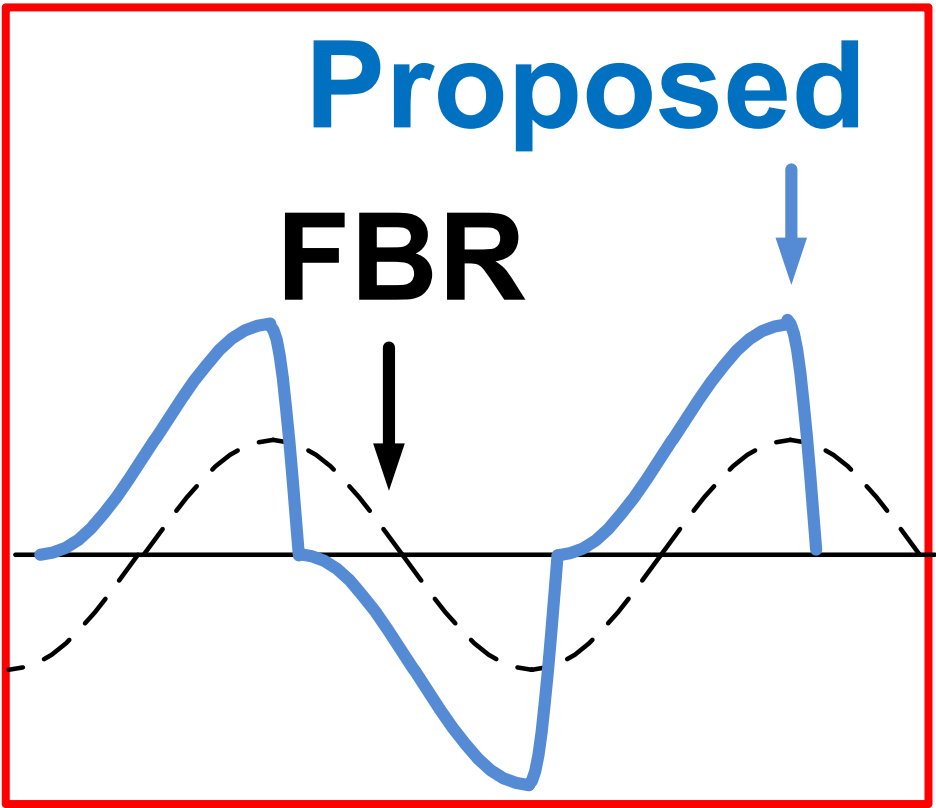
# Previous work [2]

## A Single-Inductor AC-DC Piezoelectric Energy-Harvester/ Battery-Charger IC Converting 0.35 to 1.2V, ISSCC 2010



[Type 2]

180%



FBR: Full Bridge Rectifier

# Previous work [3]

## A Single-Inductor 0.35um CMOS Energy-Investing Piezoelectric Harvester, ISSCC 2013

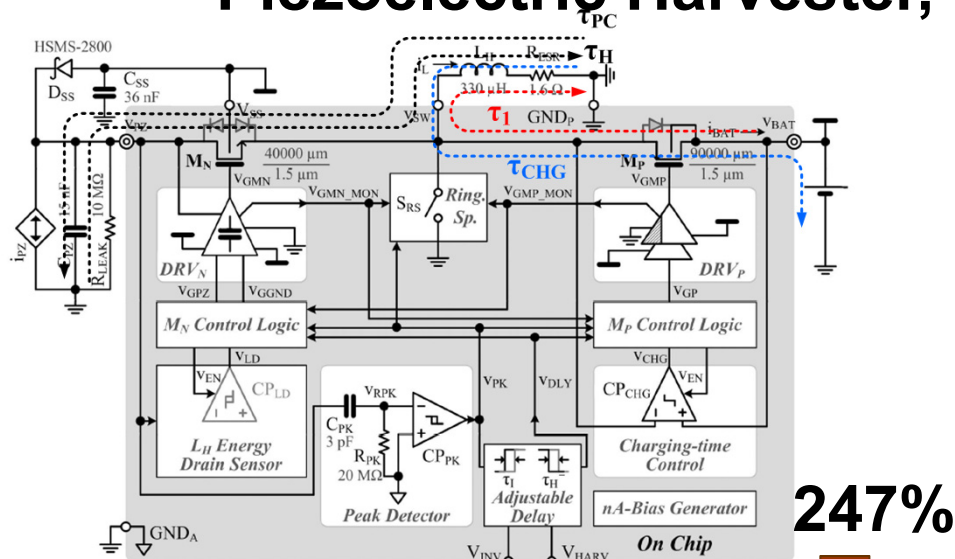


Figure 1. Energy-investing switched-inductor piezoelectric harvester.

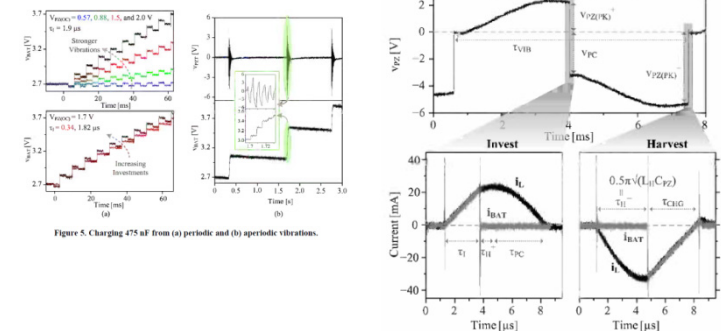
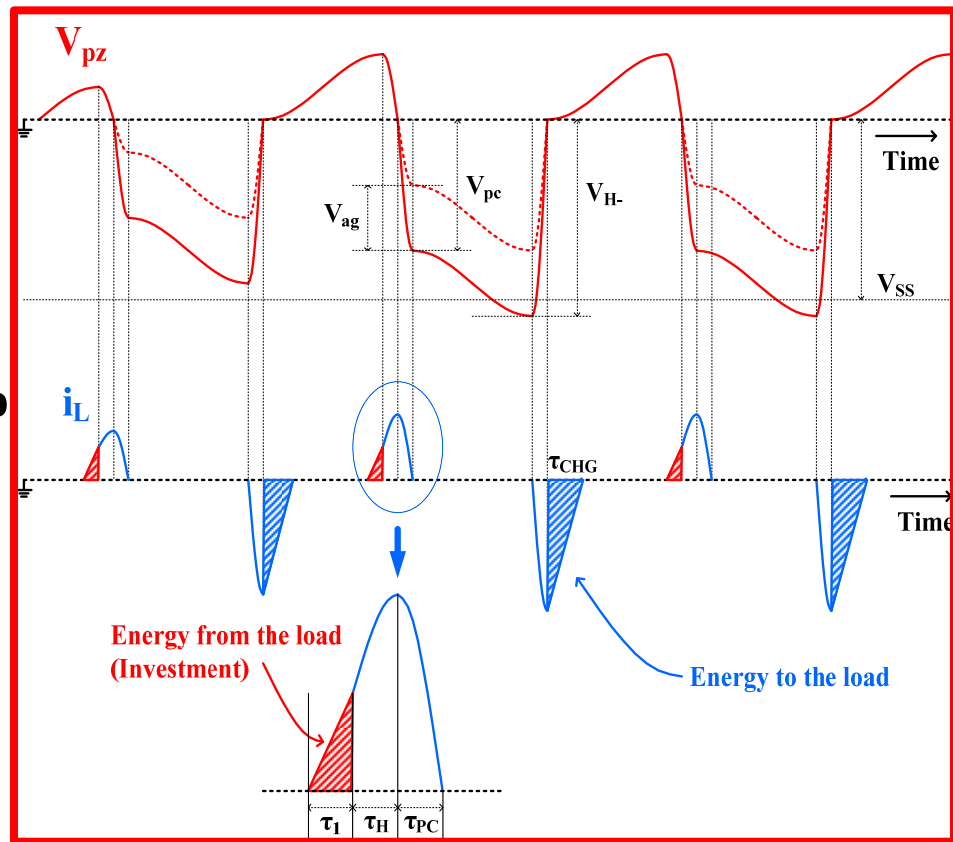


Figure 2. Measured waveforms of the piezoelectric voltage ( $v_{pz}$ ) and inductor ( $i_L$ ) and battery ( $i_{BAT}$ ) currents.



[Type 3]

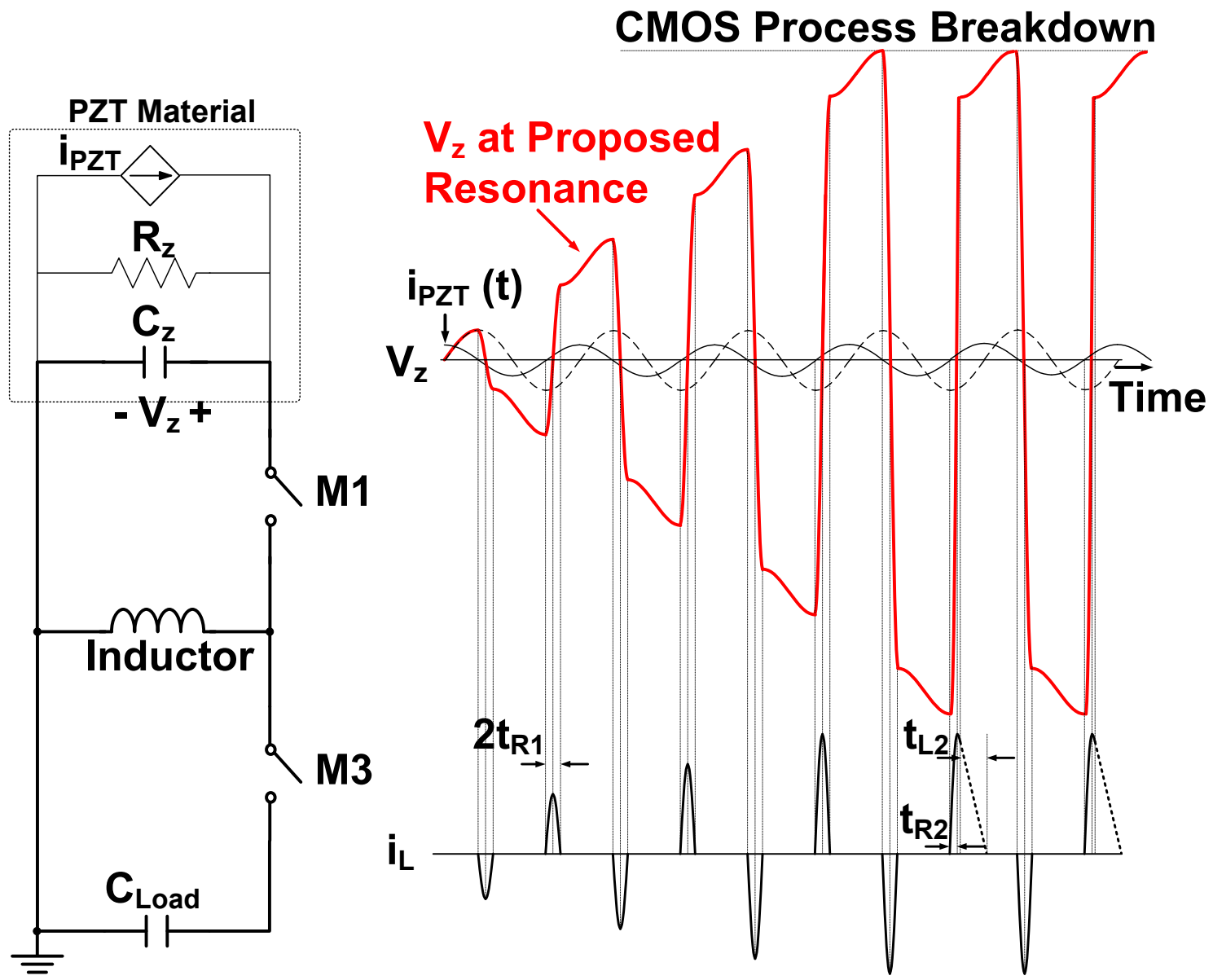


# Contents

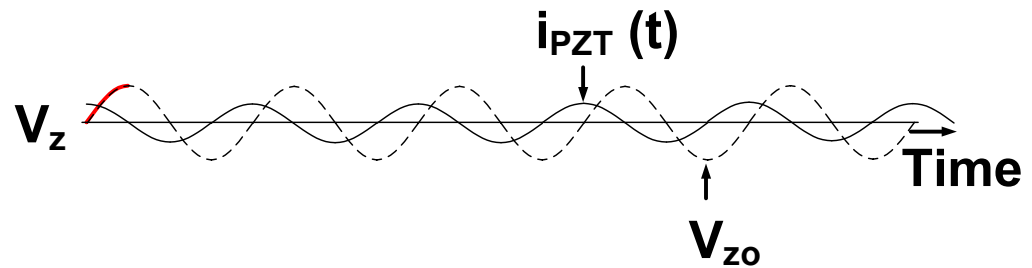
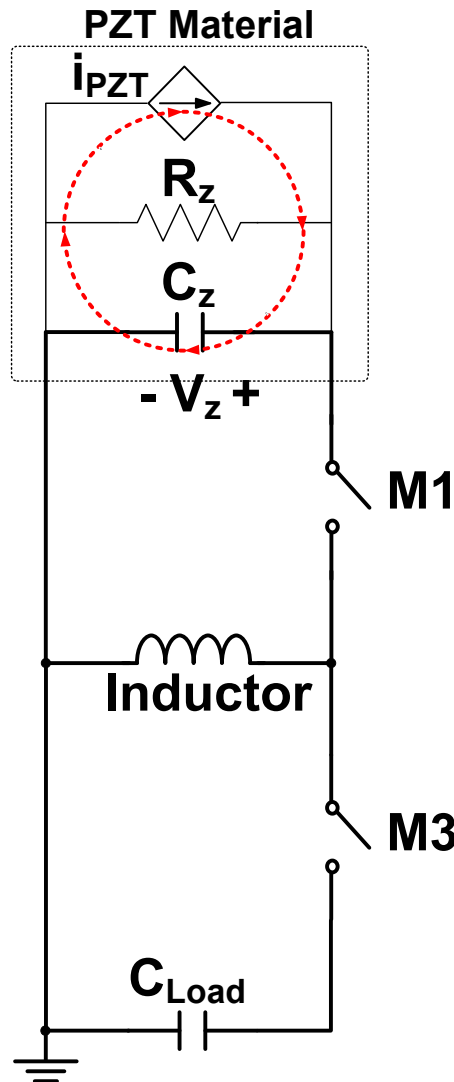
---

- Introduction about the Piezoelectric Transducer (PZT)
- The Previous works for Energy Extraction from PZT
- **A Proposed Energy Pile-up Resonance Technique**
- Chip Implementation
- Measurement Results
- Conclusion

# A Proposed Energy Pile-up Resonance Technique

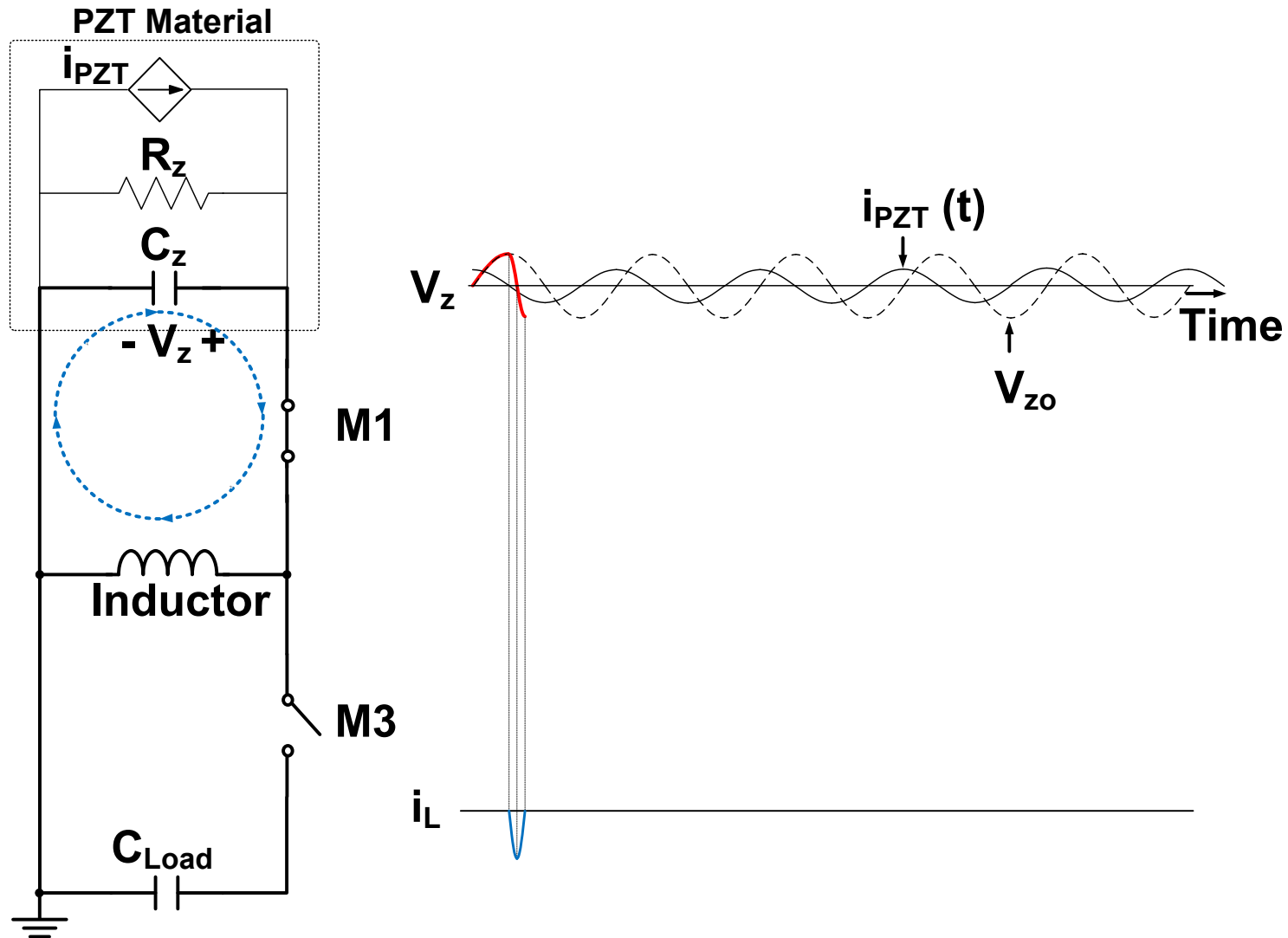


# How can the Energy Piles-up in the Capacitor ?

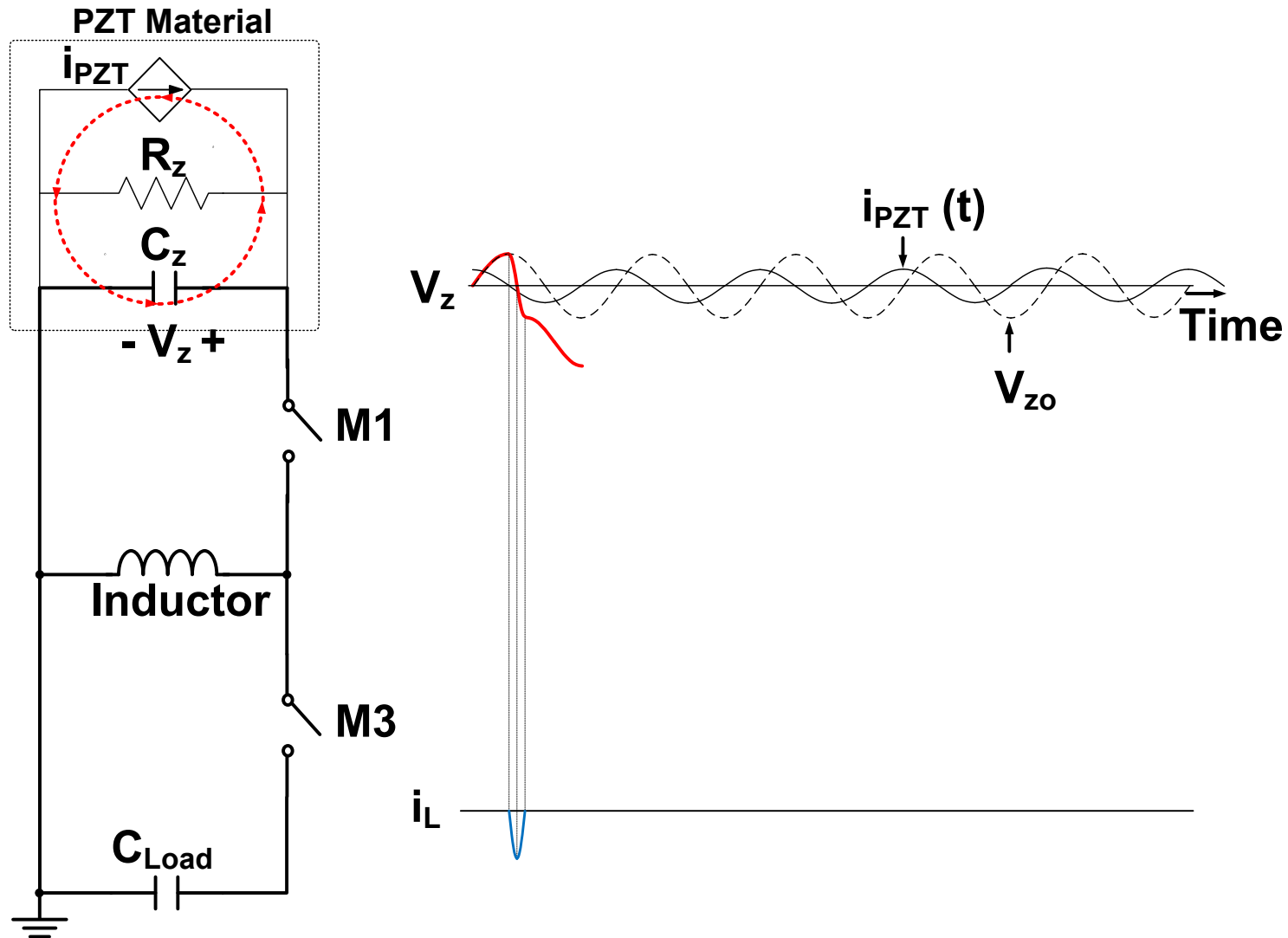


$i_L$  \_\_\_\_\_

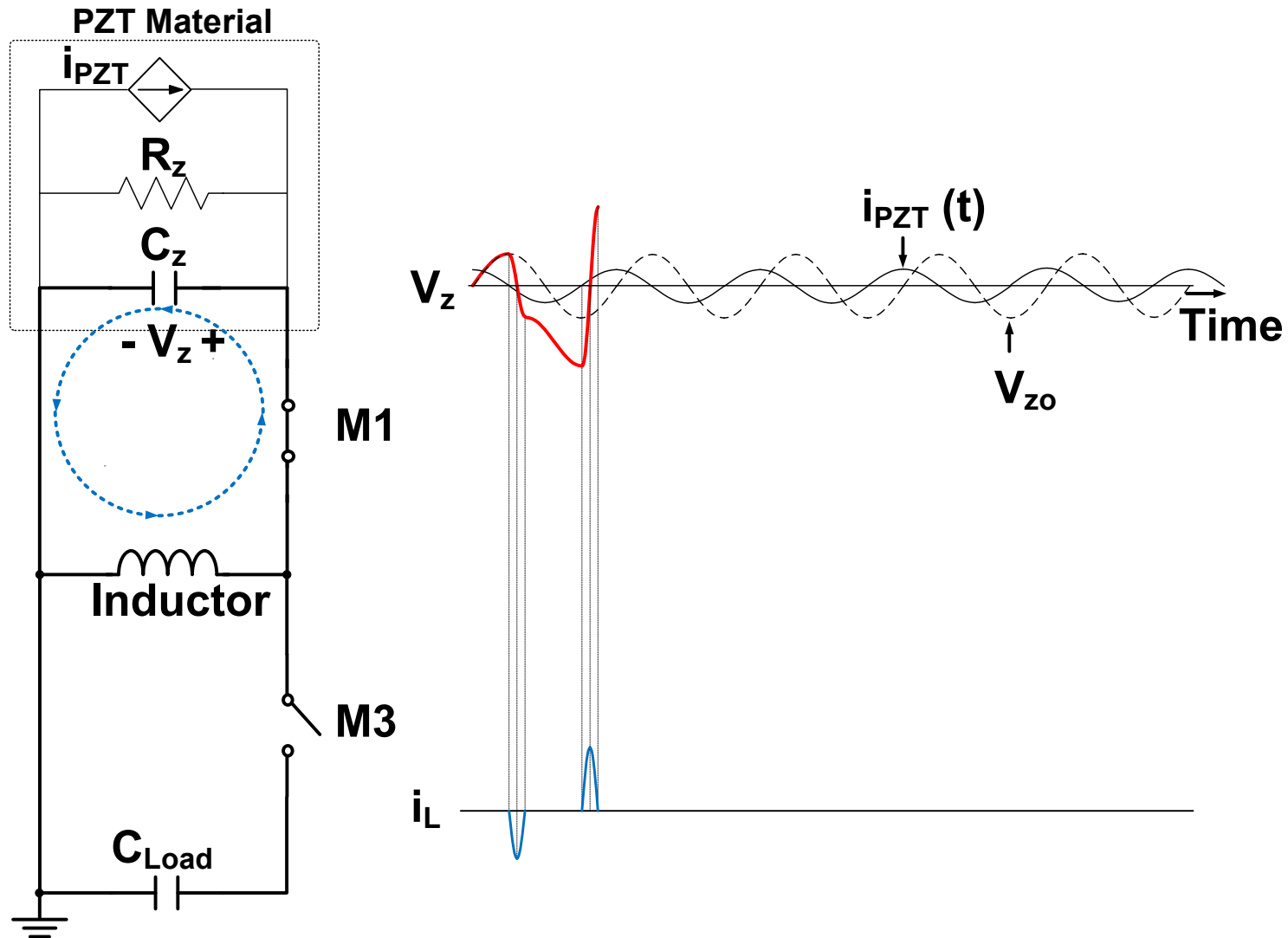
# How can the Energy Piles-up in the Capacitor ?



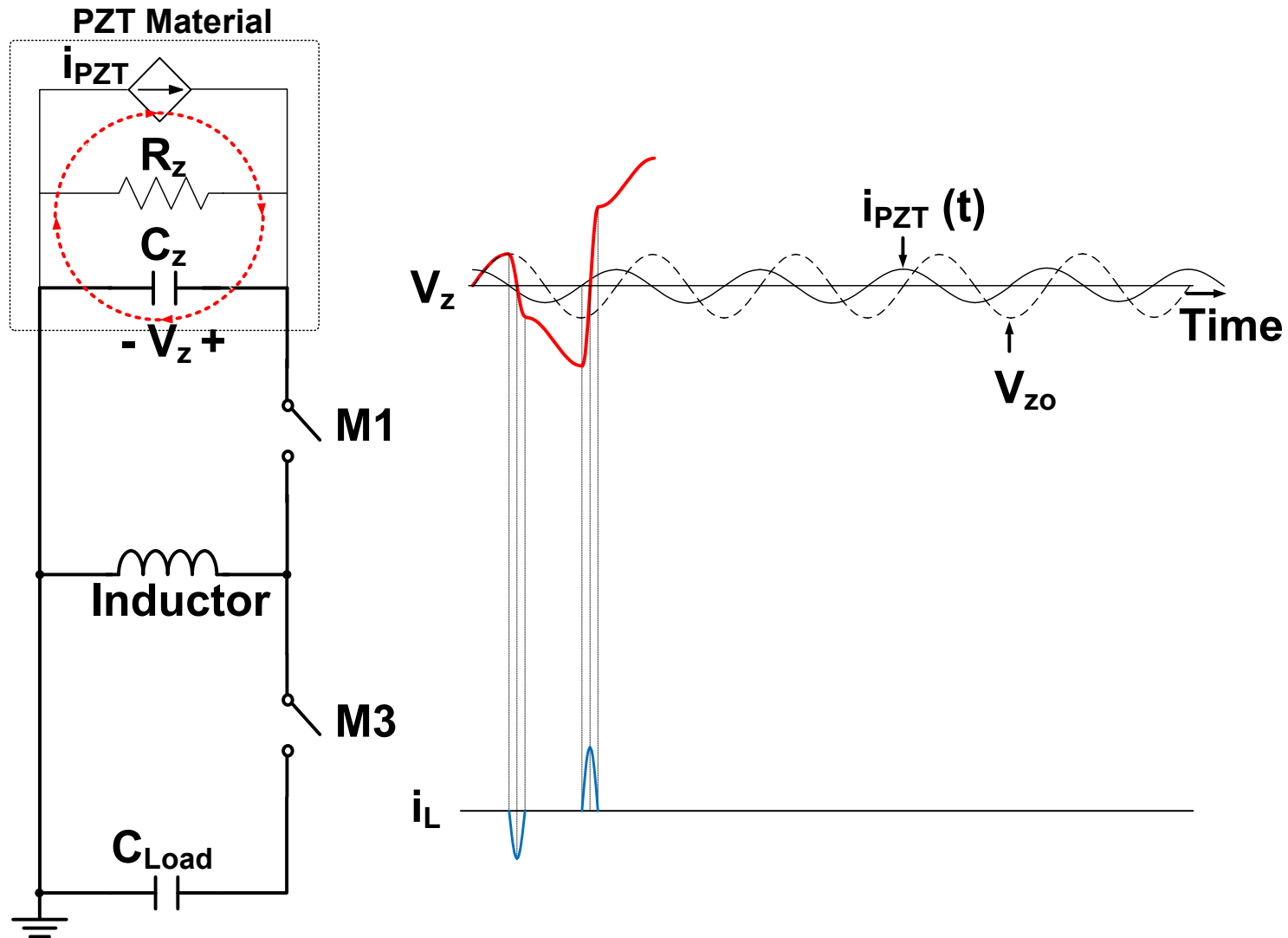
# How can the Energy Piles-up in the Capacitor ?



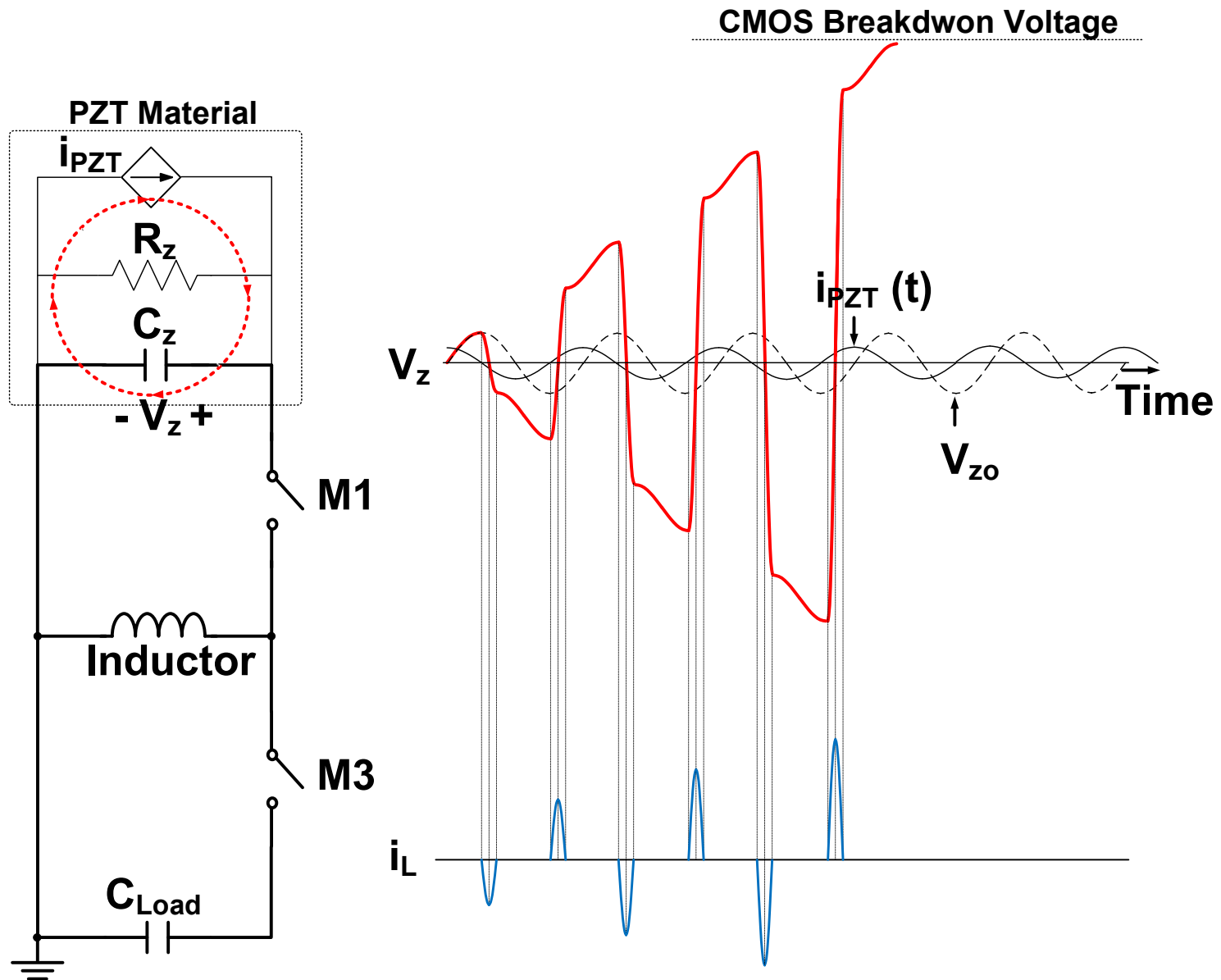
# How can the Energy Pile-up in the Capacitor ?



# How can the Energy Piles-up in the Capacitor ?

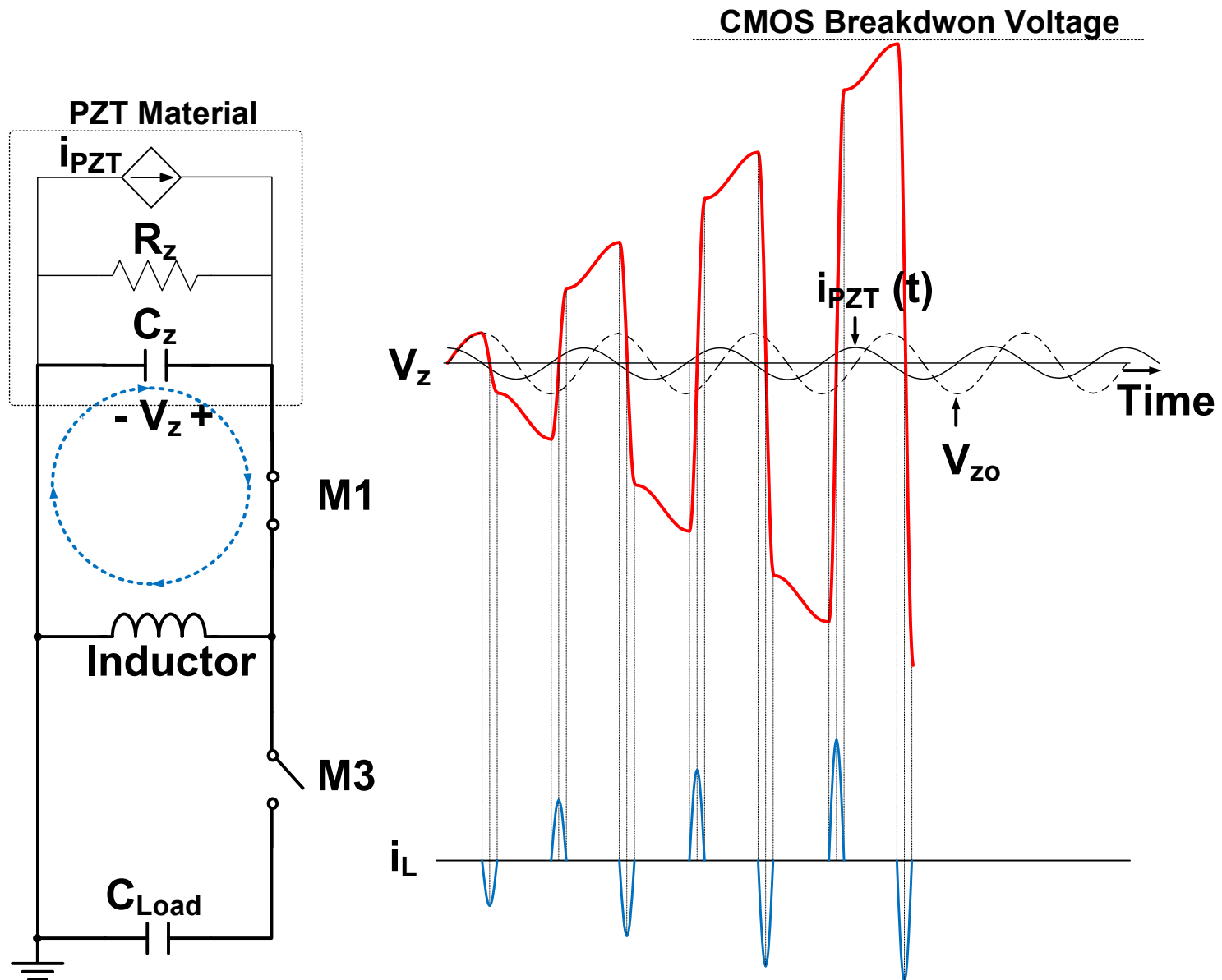


# How can the Energy Piles-up in the Capacitor ?

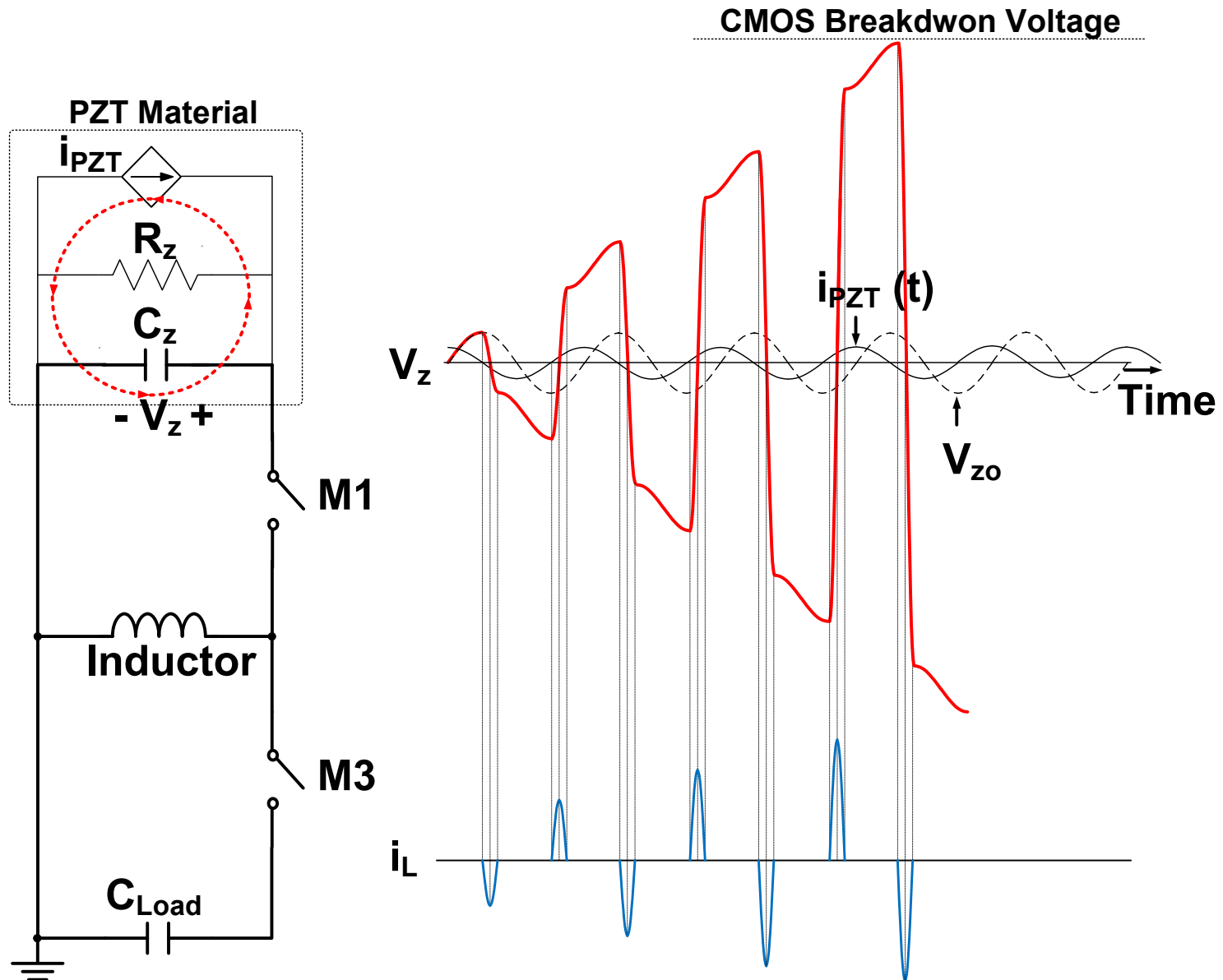




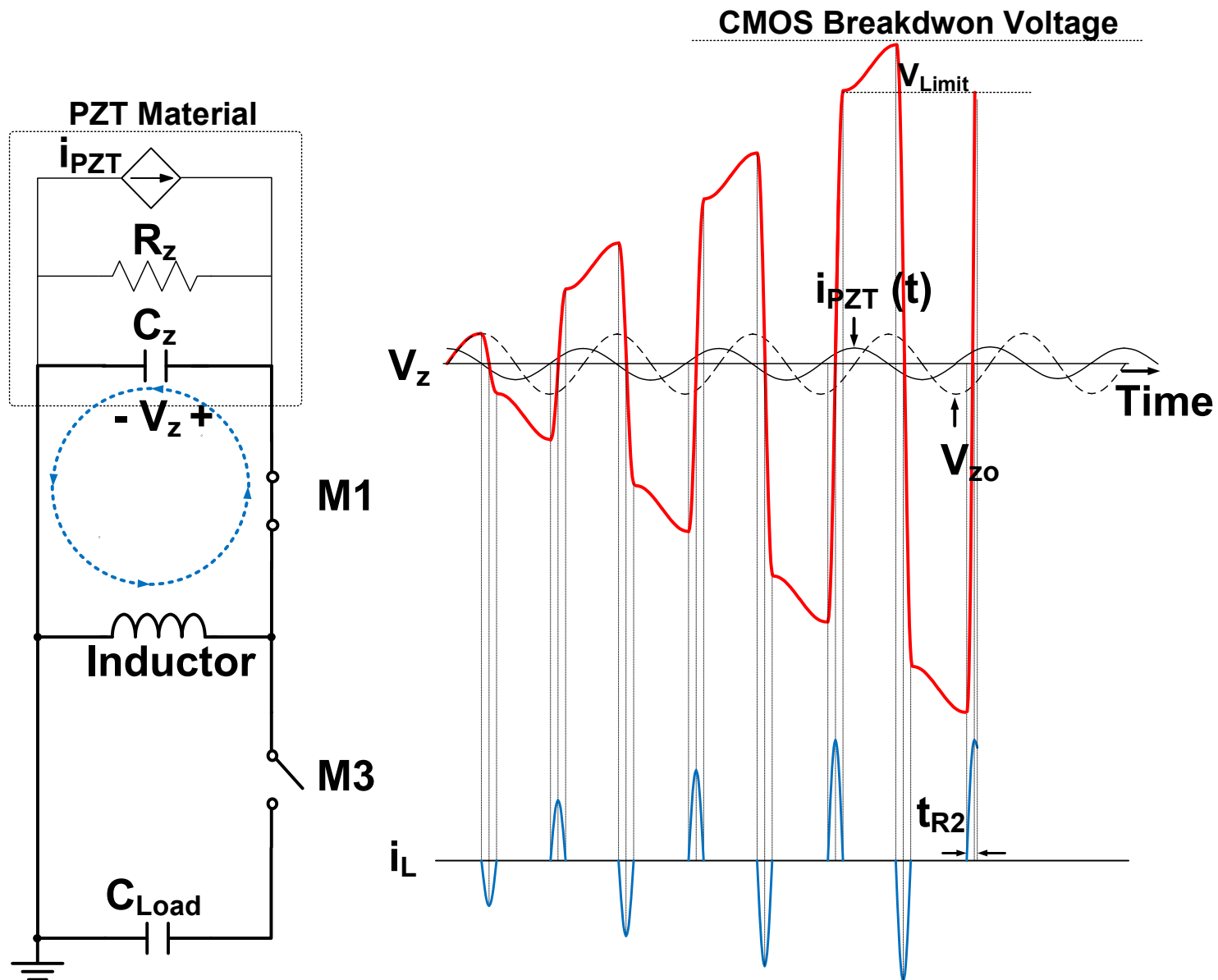
# How can the Energy be transferred to the Load ?



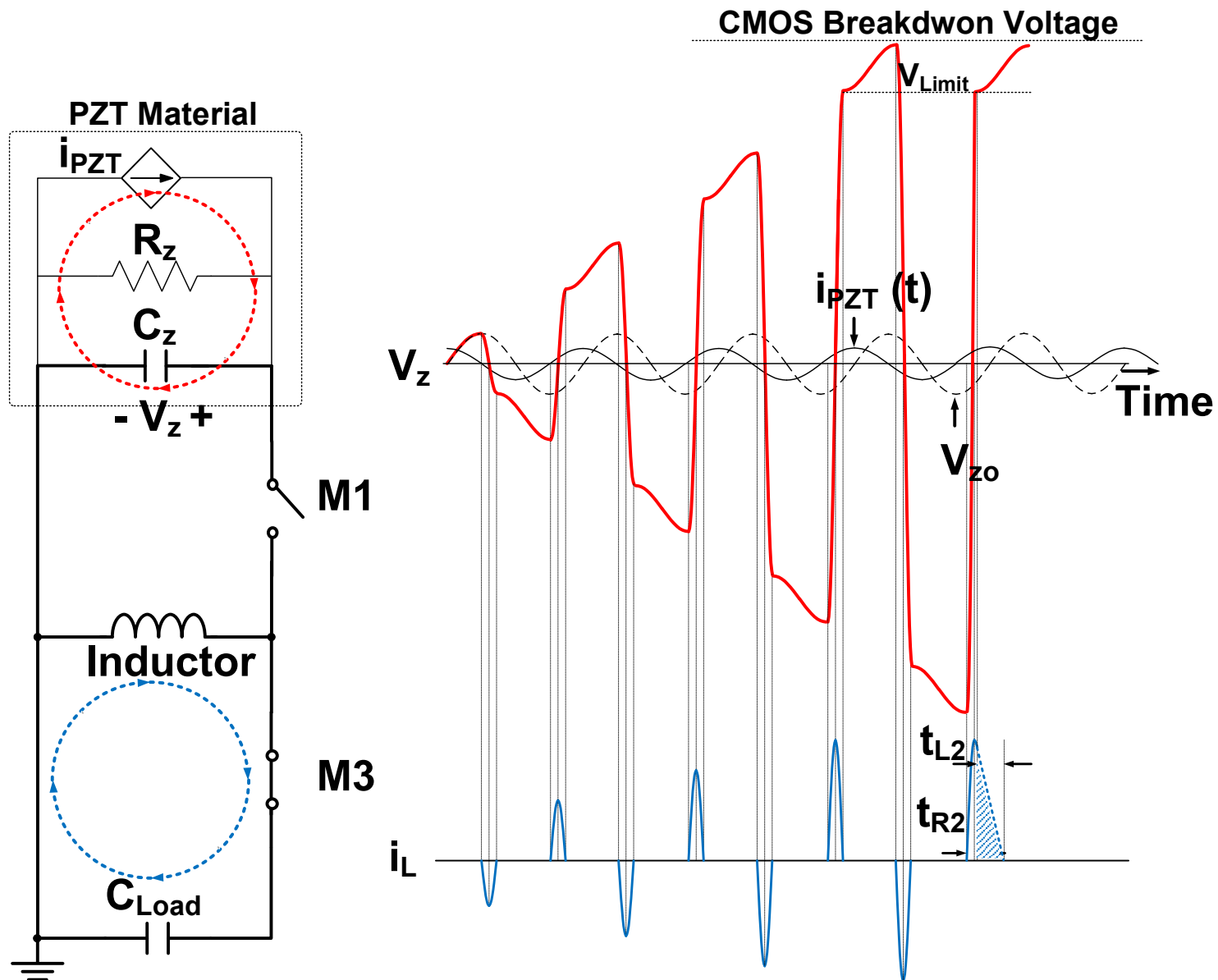
# How can the Energy be transferred to the Load ?



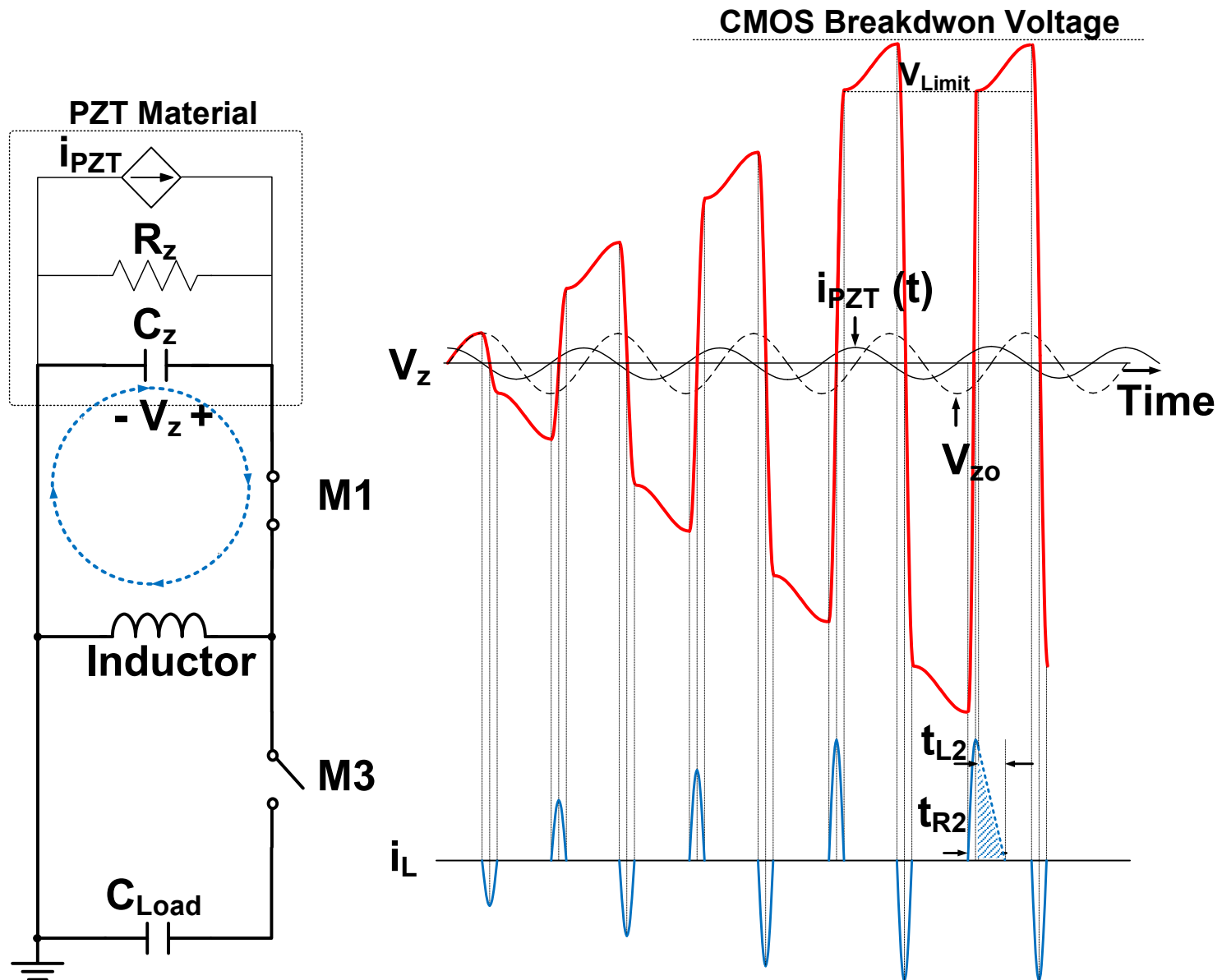
# How can the Energy be transferred to the Load ?



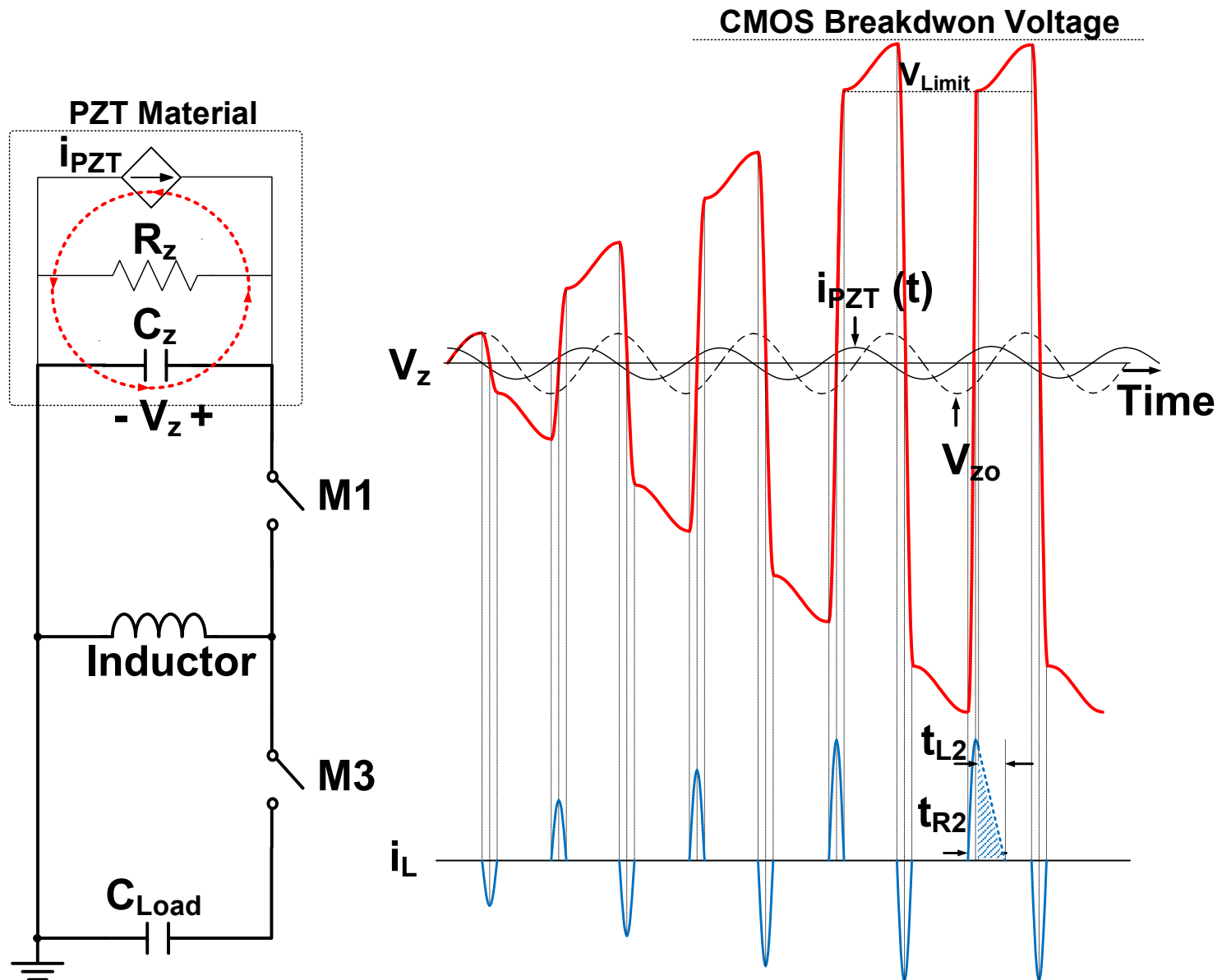
# How can the Energy be transferred to the Load ?



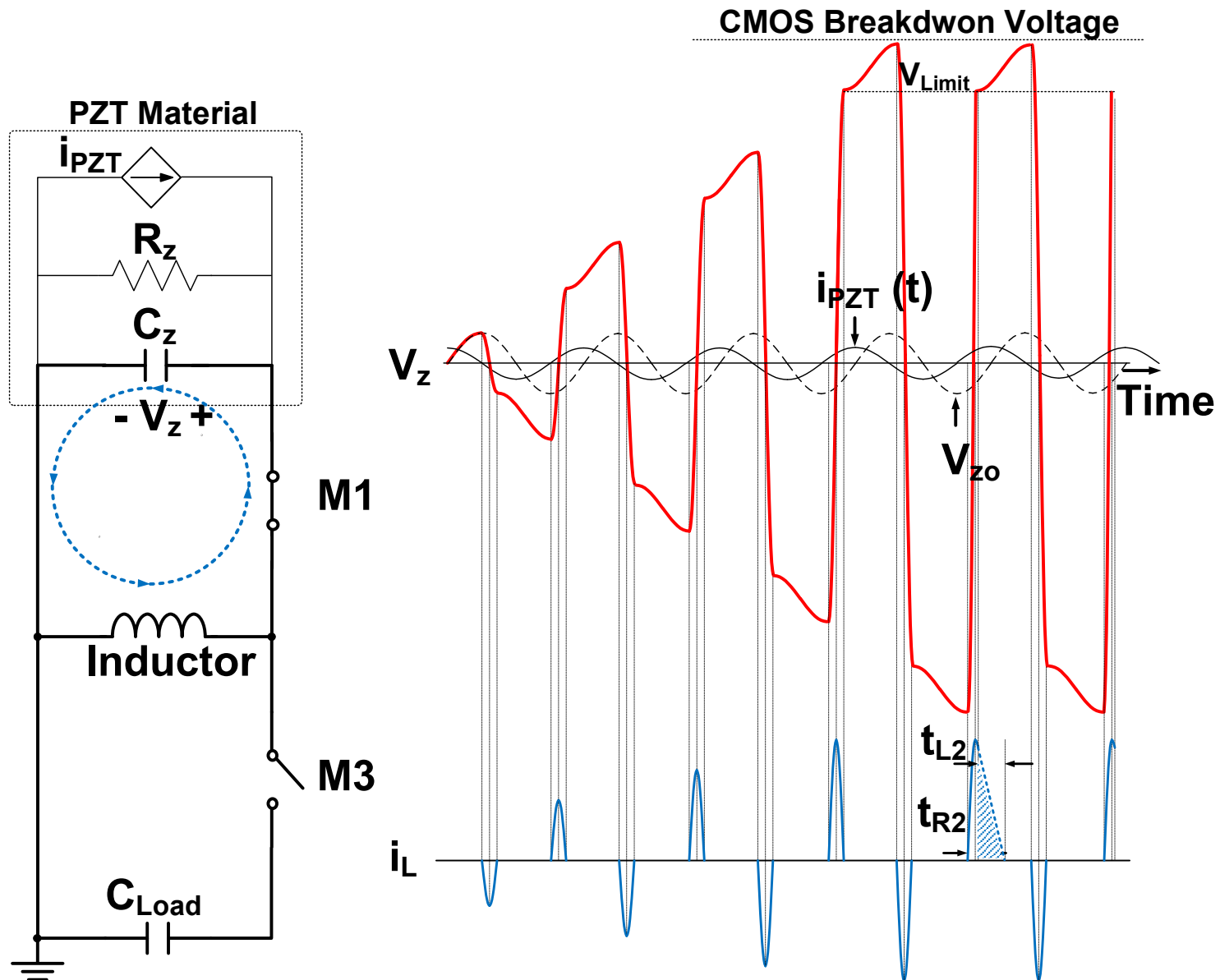
# How can the Energy be transferred to the Load ?



# How can the Energy be transferred to the Load ?

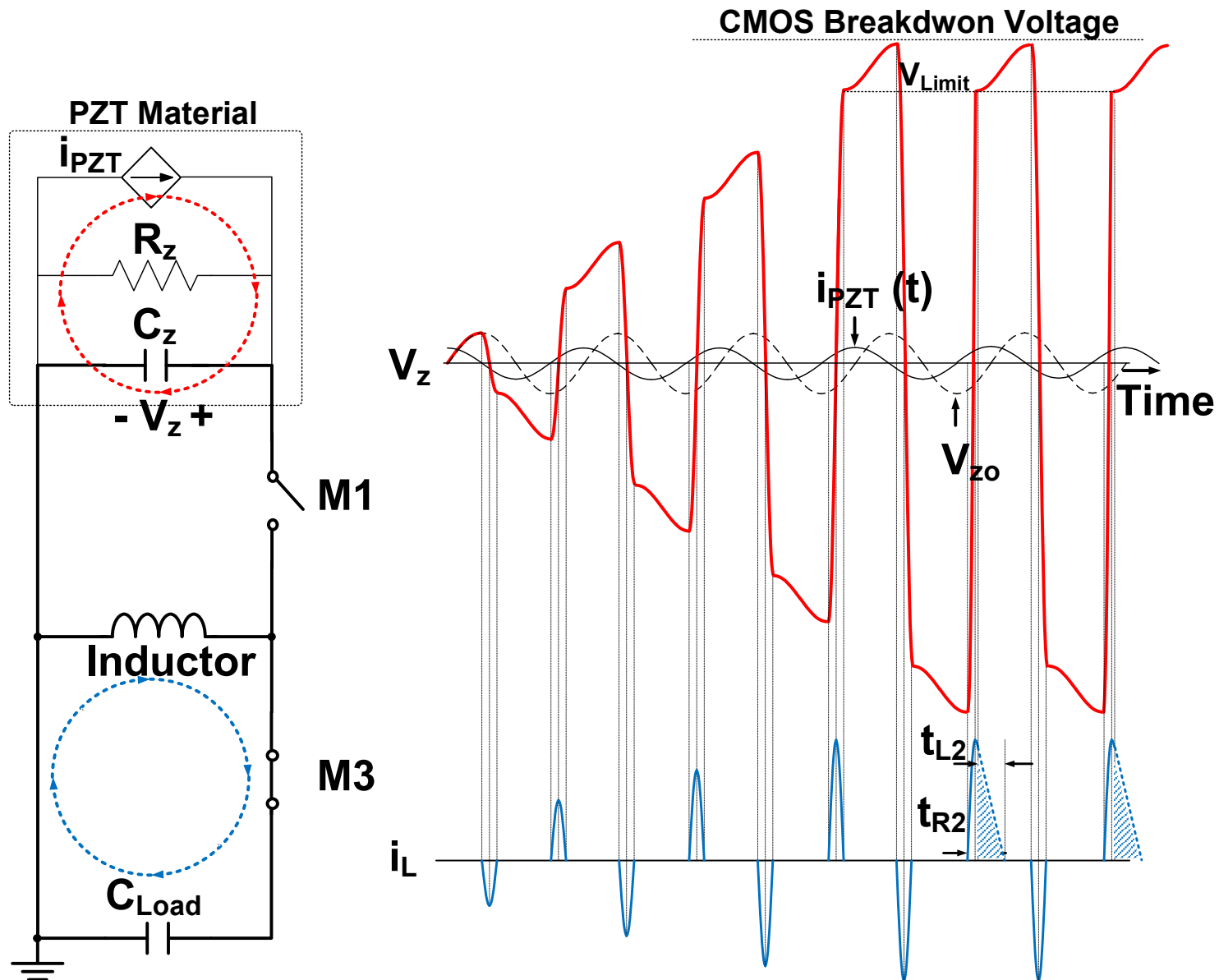


# How can the Energy be transferred to the Load ?



23.5: An Energy Pile-up Resonance Circuit Extracting Maximum 422% Energy from Piezoelectric Material in a Dual-Source Energy-Harvesting Interface

# How can the Energy be transferred to the Load ?

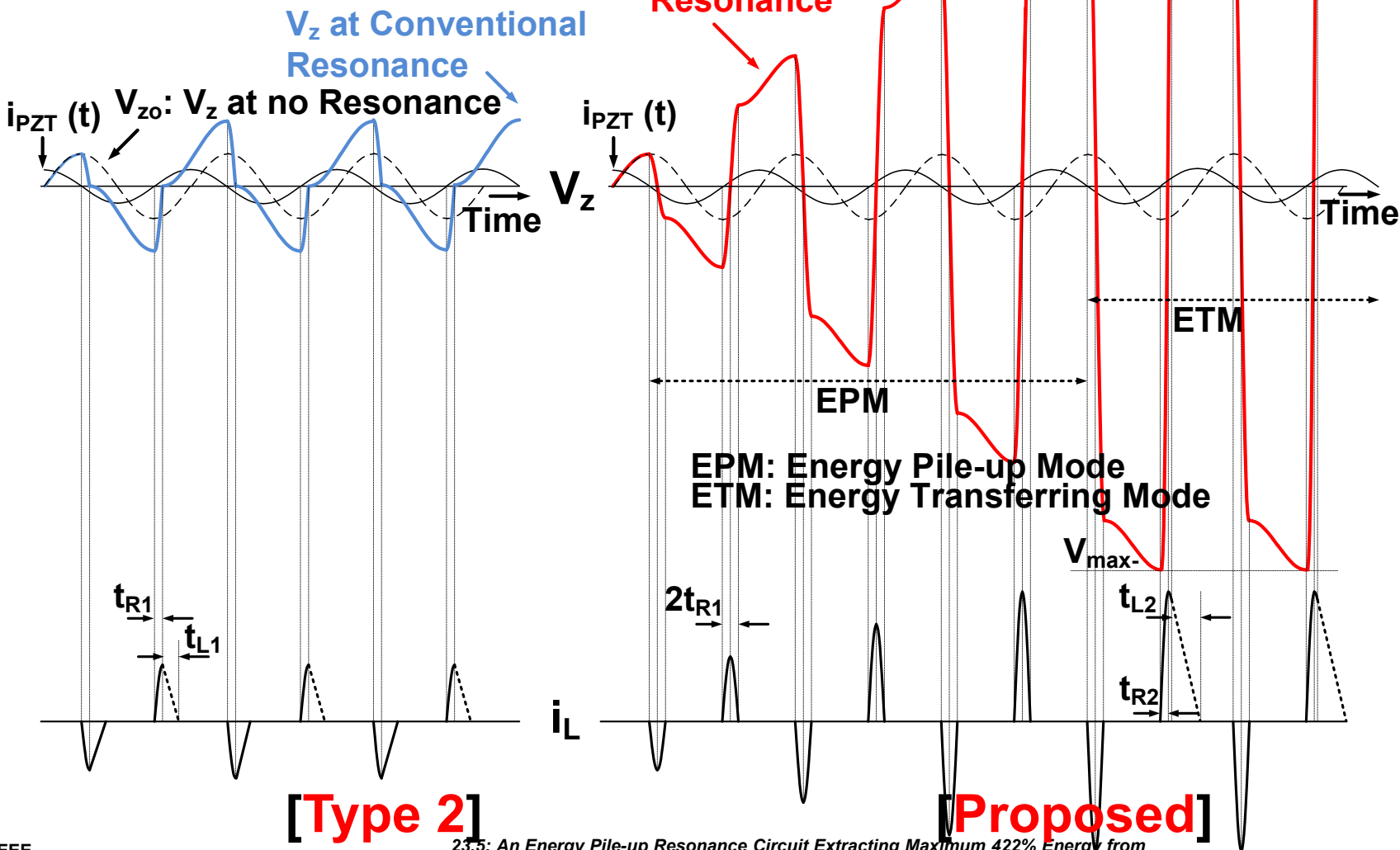




# A Proposed Energy Pile-up Resonance Technique

$$E_L = \frac{1}{2} \cdot C_z \cdot |V_{\max} -|^2 - \frac{1}{2} \cdot C_z \cdot V_{\text{Limit}}^2$$

Limited by CMOS Process Breakdown

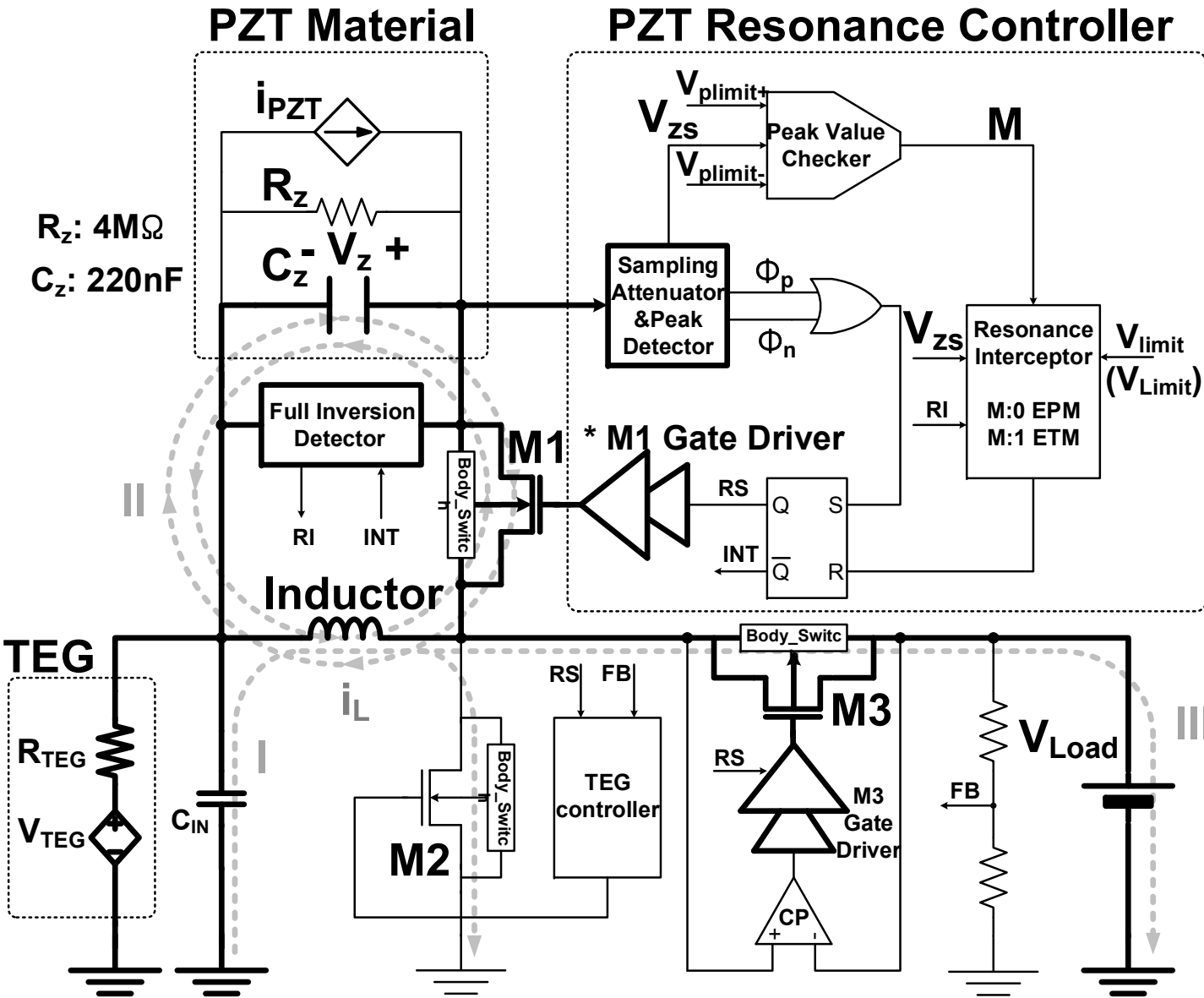


# Contents

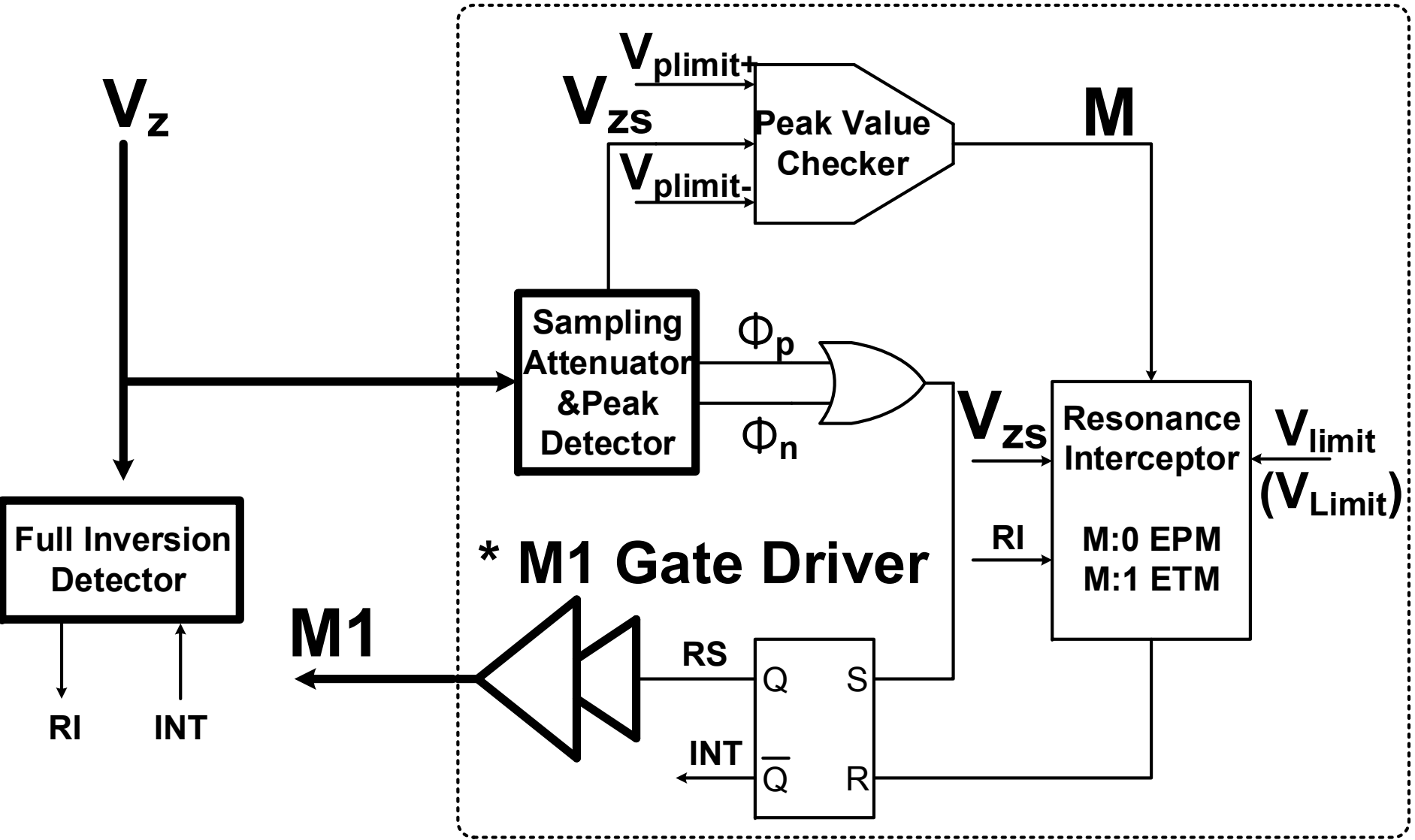
---

- Introduction about the Piezoelectric Transducer (PZT)
- The Previous works for Energy Extraction from PZT
- A Proposed Energy Pile-up Resonance Technique
- **Chip Implementation**
- Measurement Results
- Conclusion

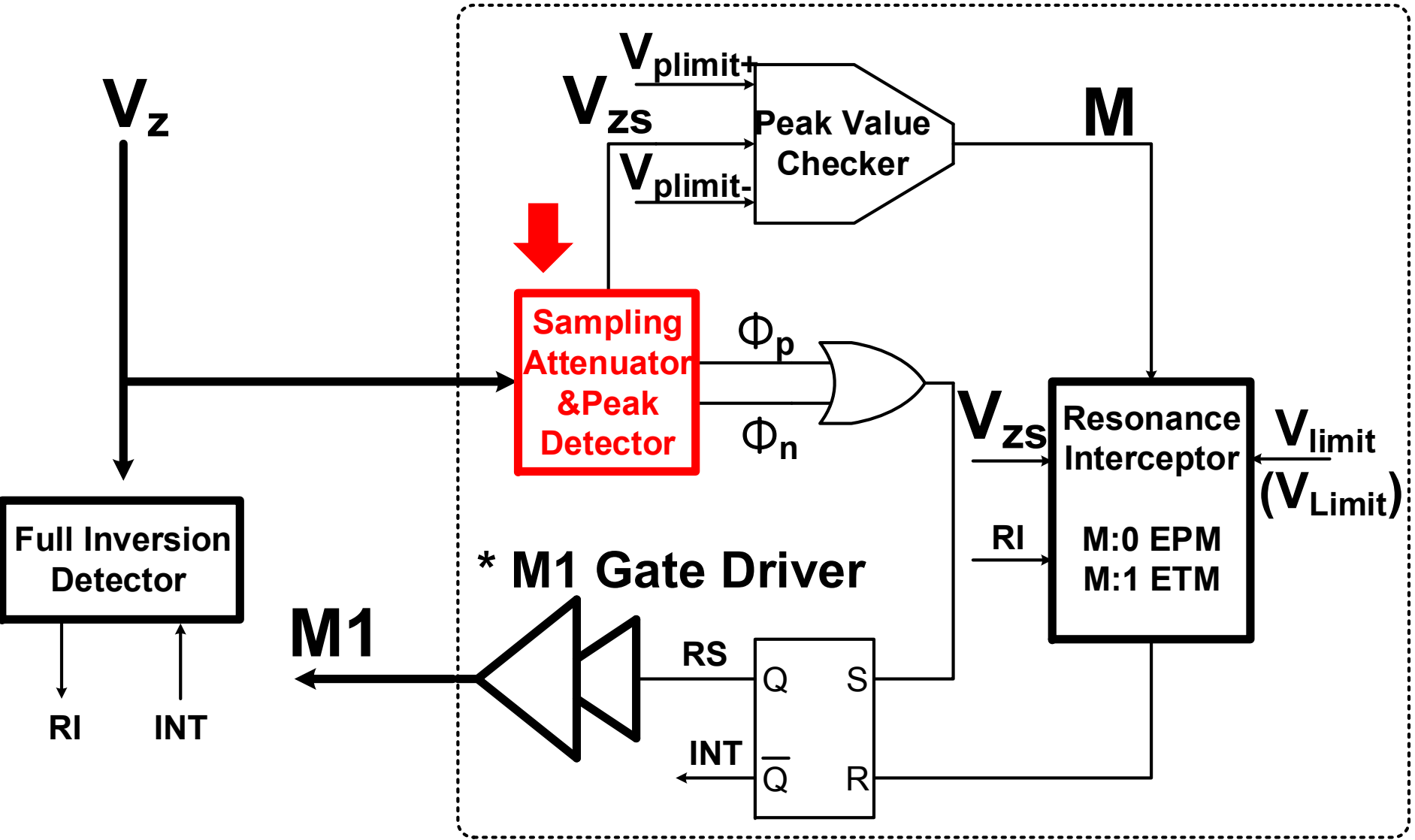
# 0.35um BCDMOS Energy Pile-up Resonance Circuit for PZT



# PZT Resonance Controller

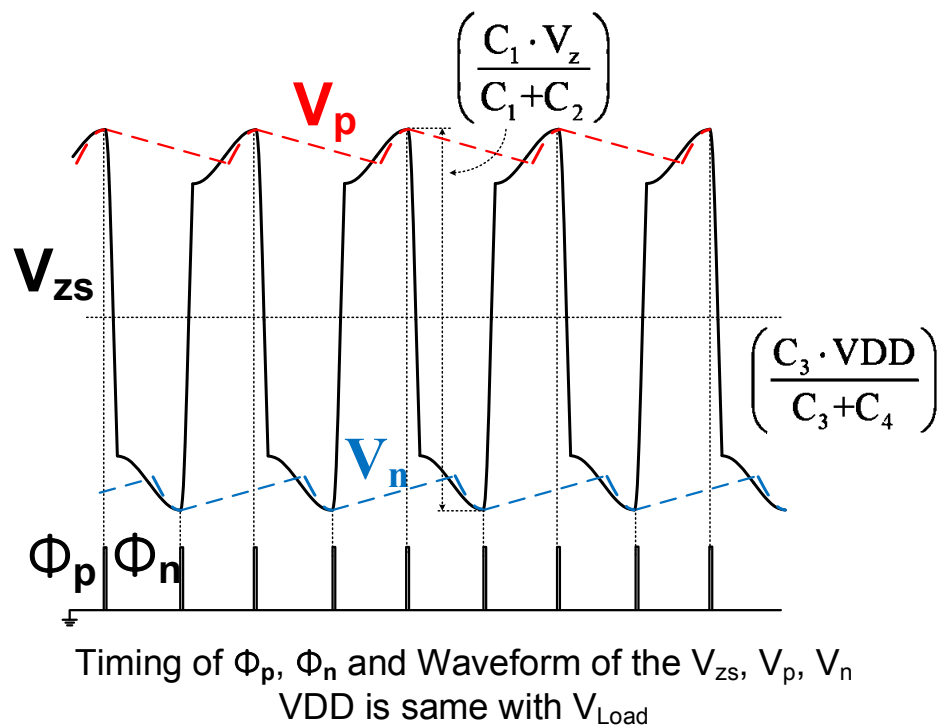
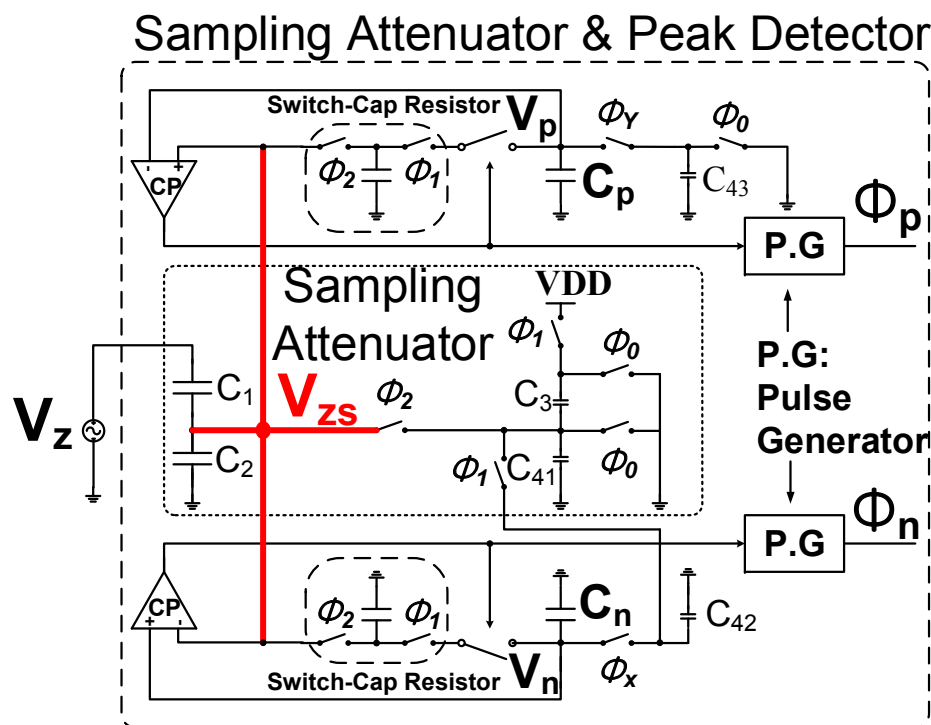


# PZT Resonance Controller

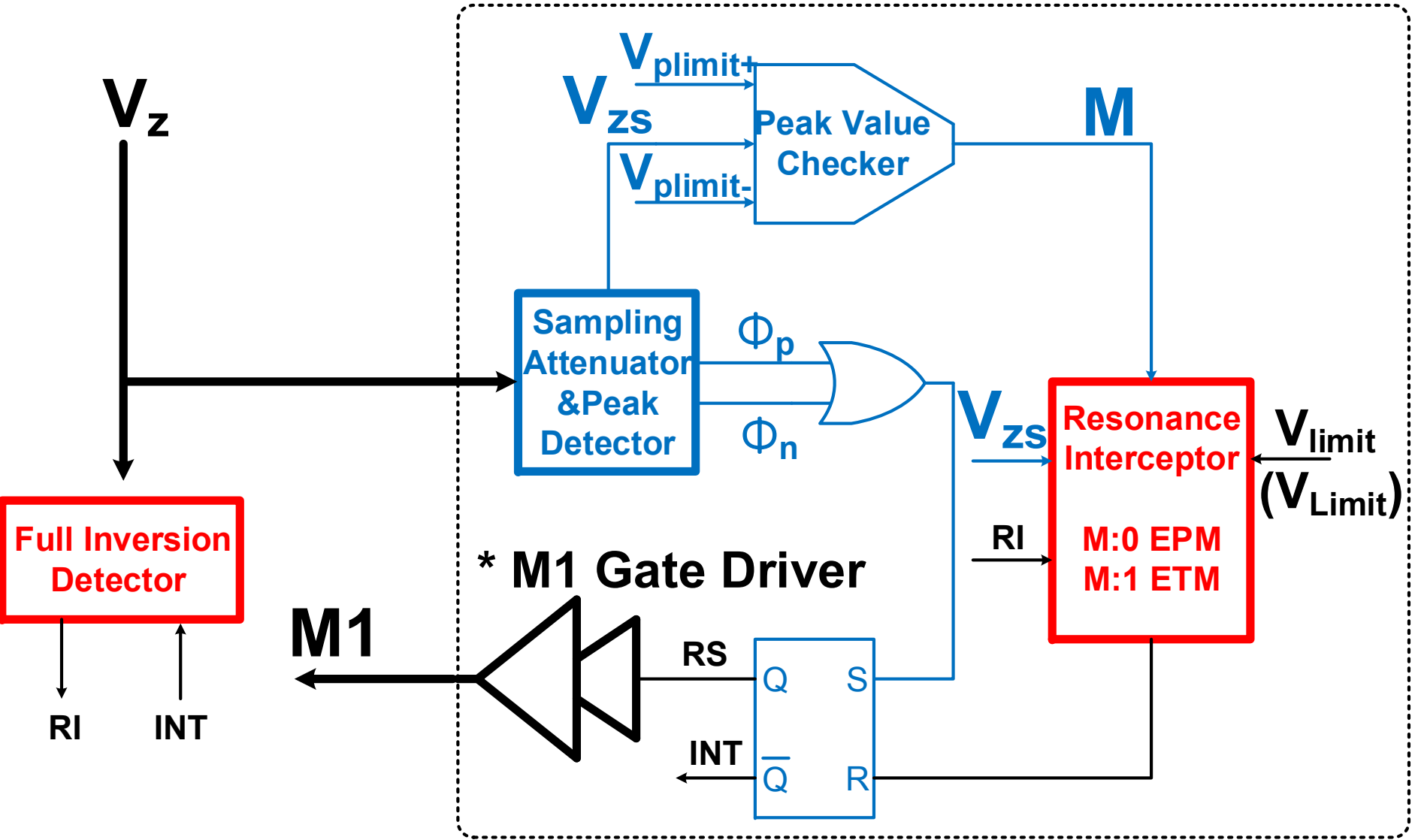


# Sampling Attenuator & Peak Detector

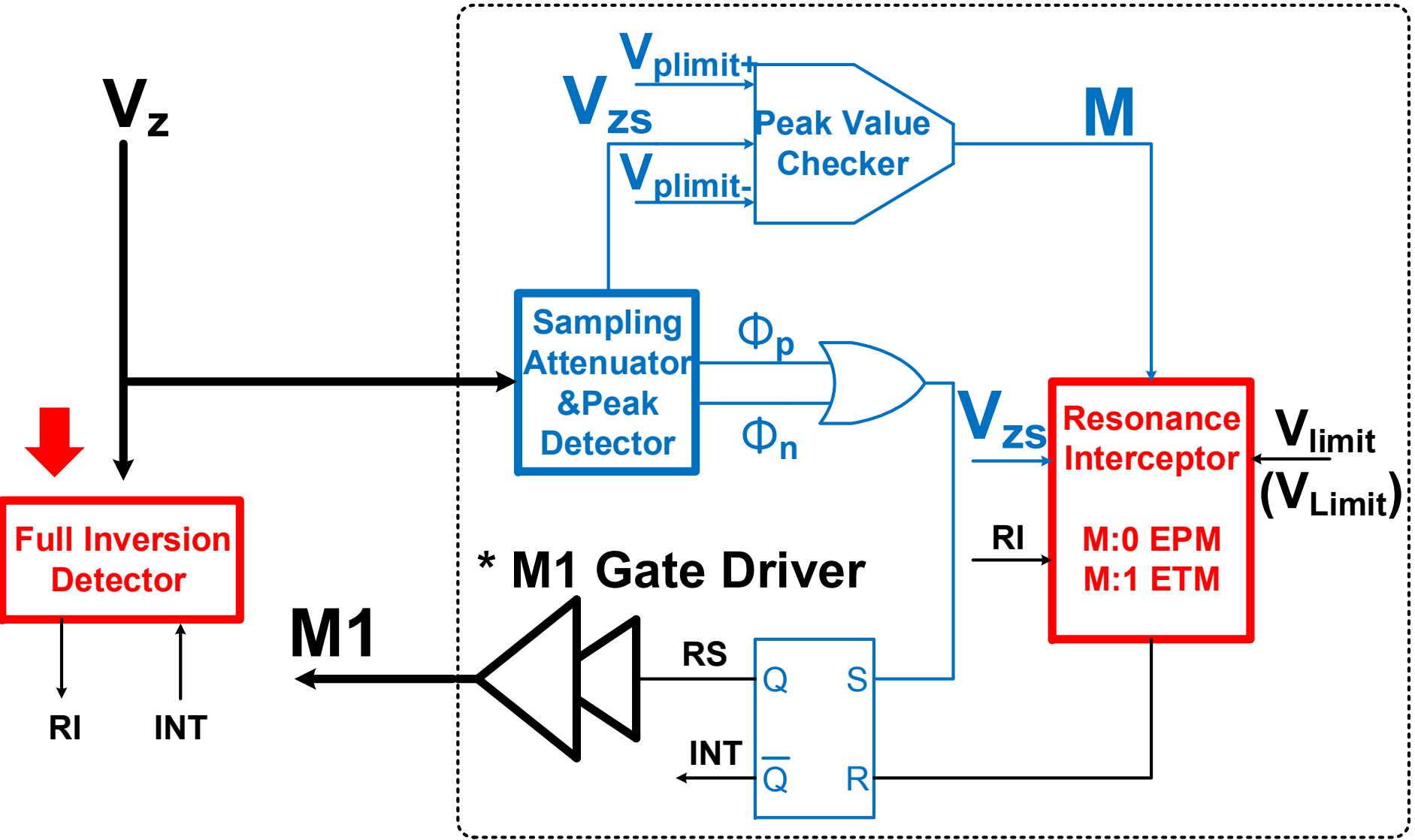
- Sensing the  $V_z$  and make a  $V_{zs}$  for resonance control
- DC voltage of the  $V_{zs}$  can be defined by  $C_3$  and  $C_4$  ( $C_{41}+C_{42}$ )



# PZT Resonance Controller

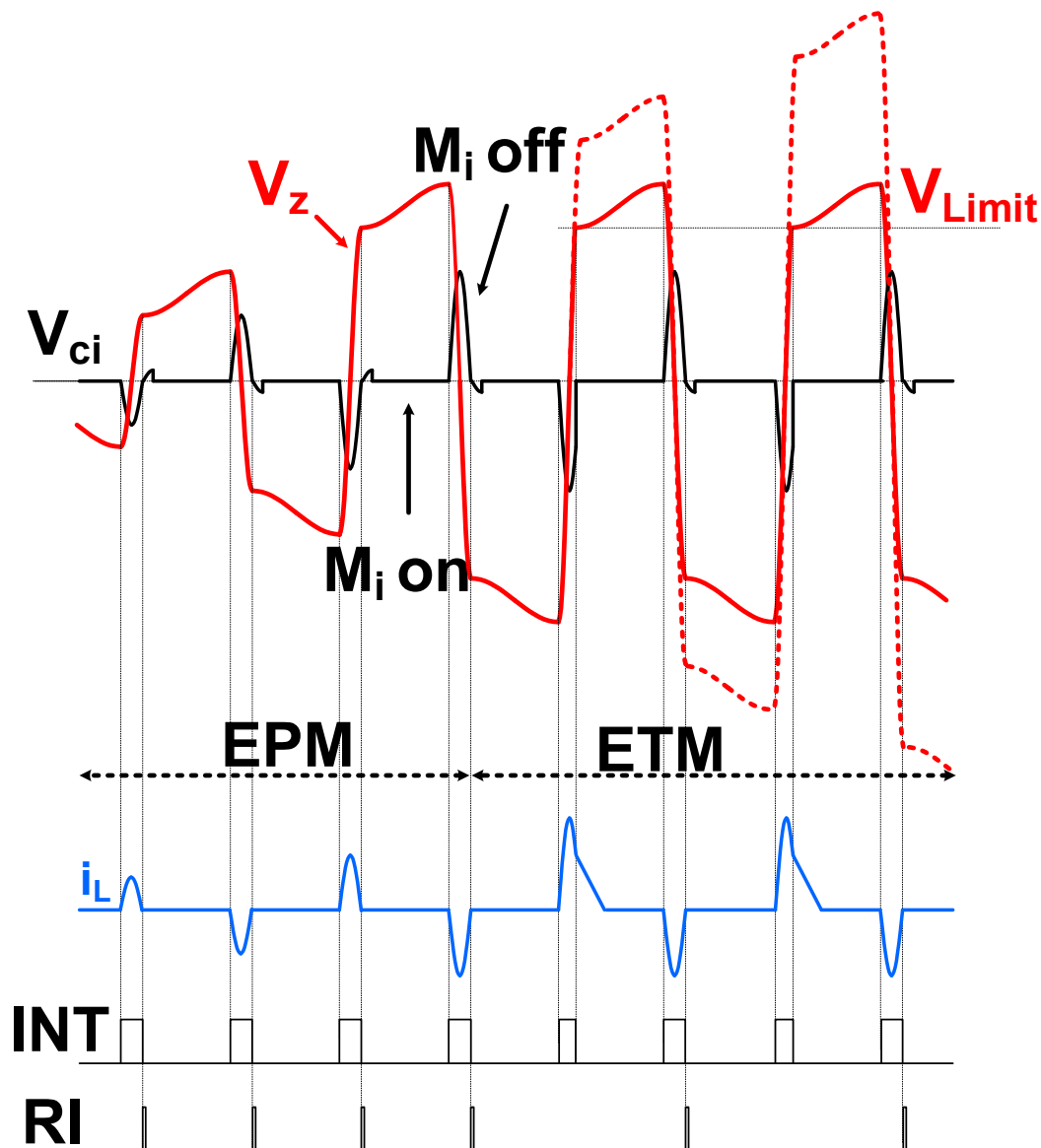
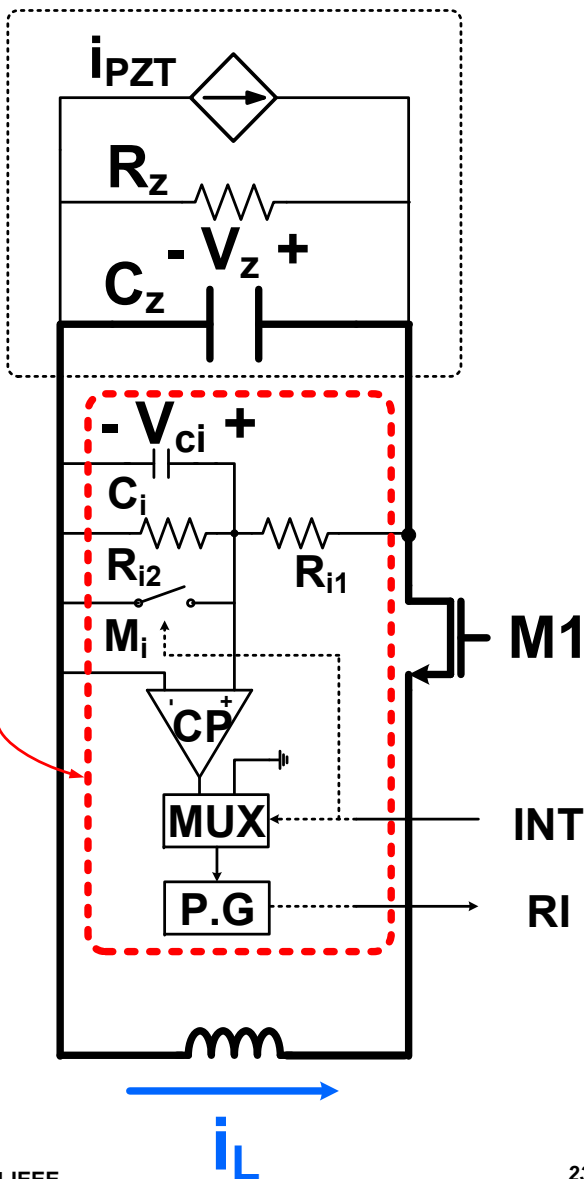


# PZT Resonance Controller

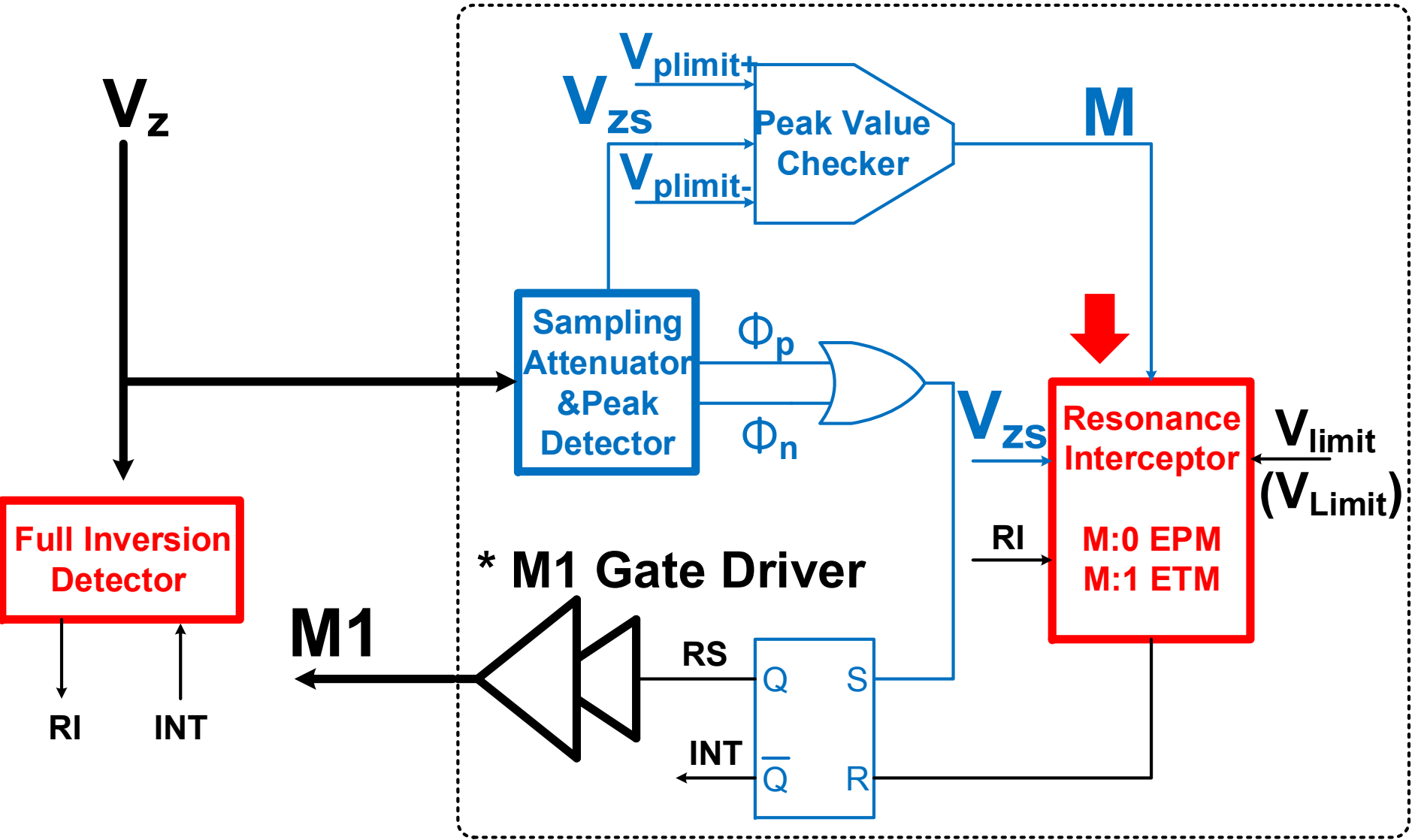




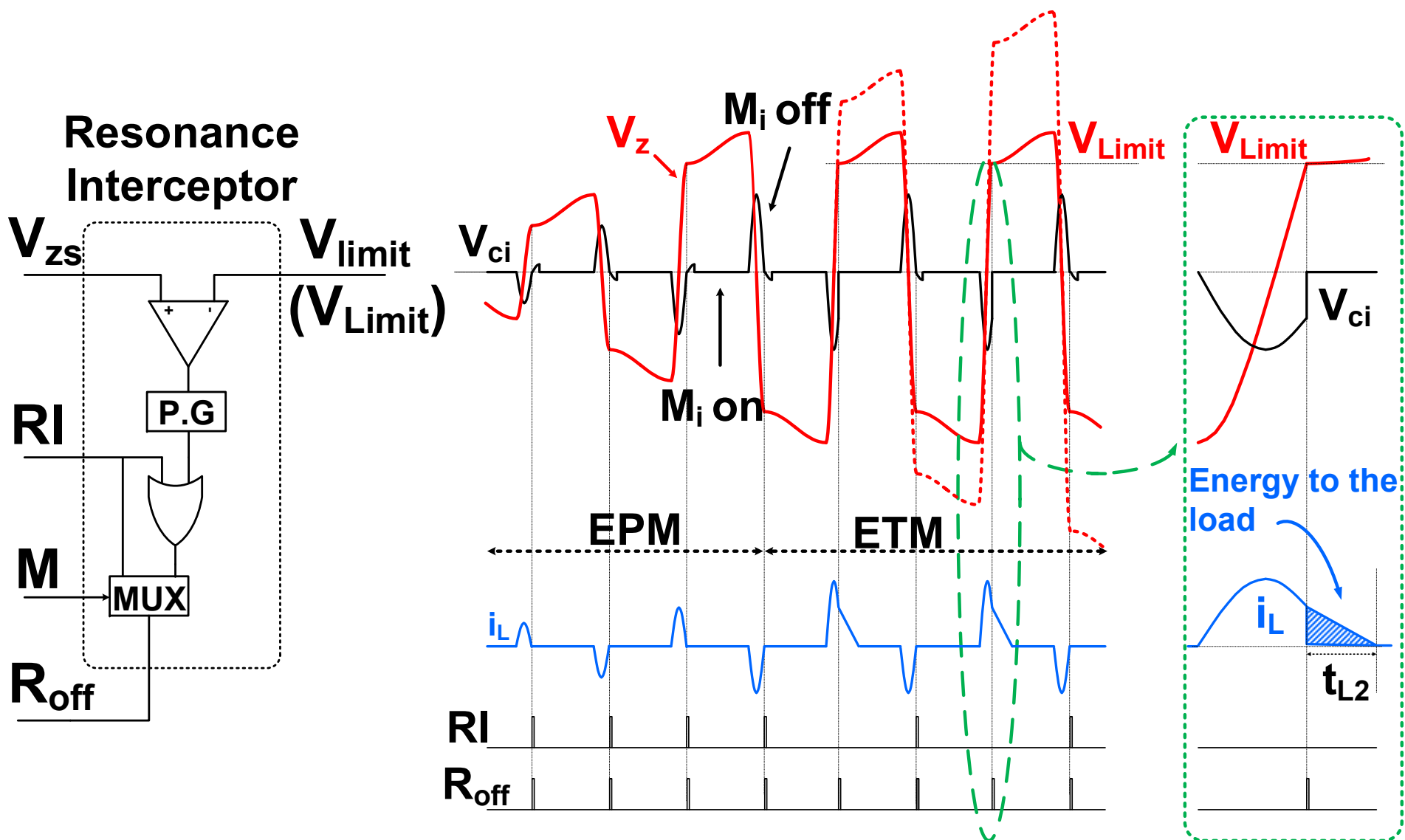
## Full Inversion Detector



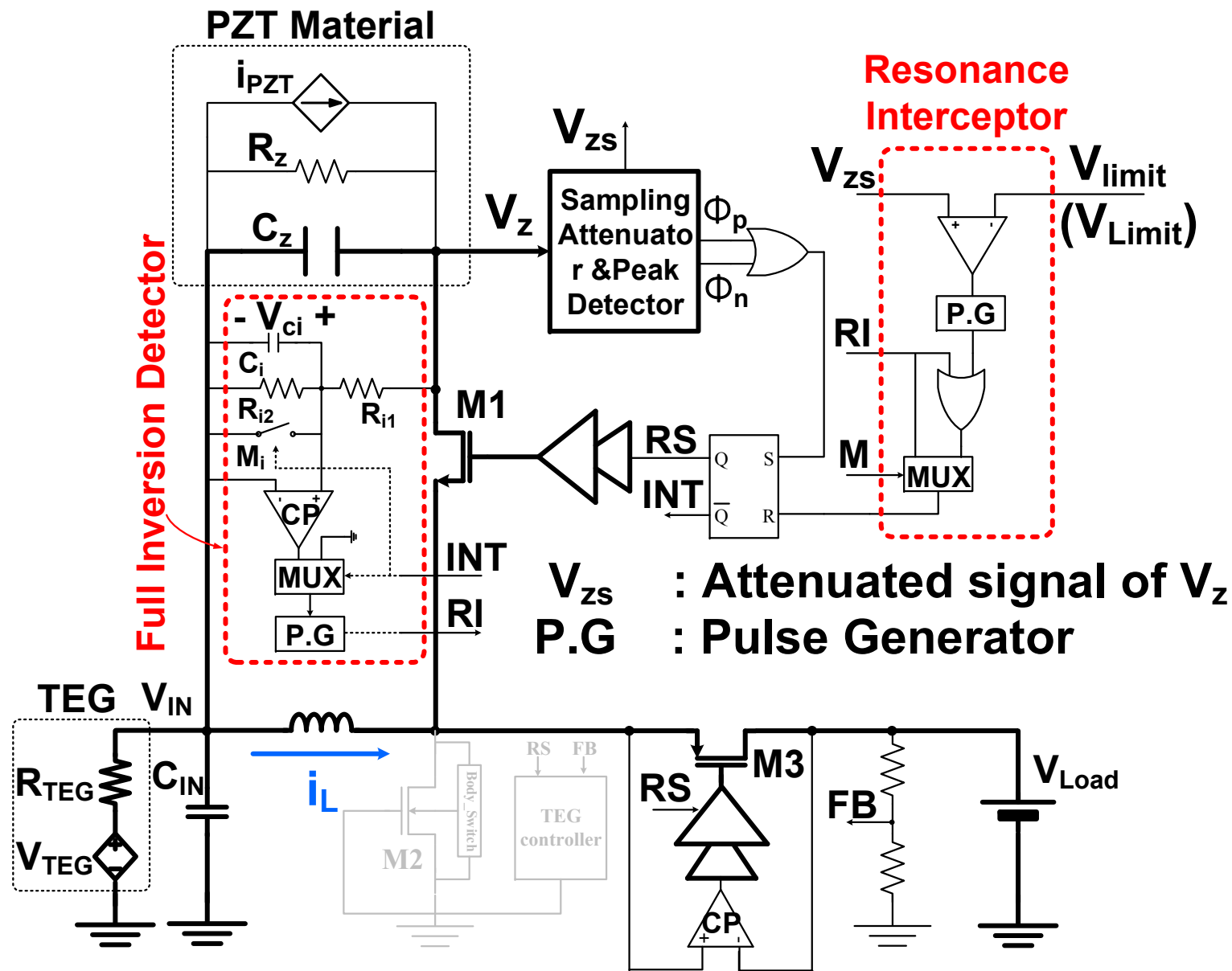
# PZT Resonance Controller



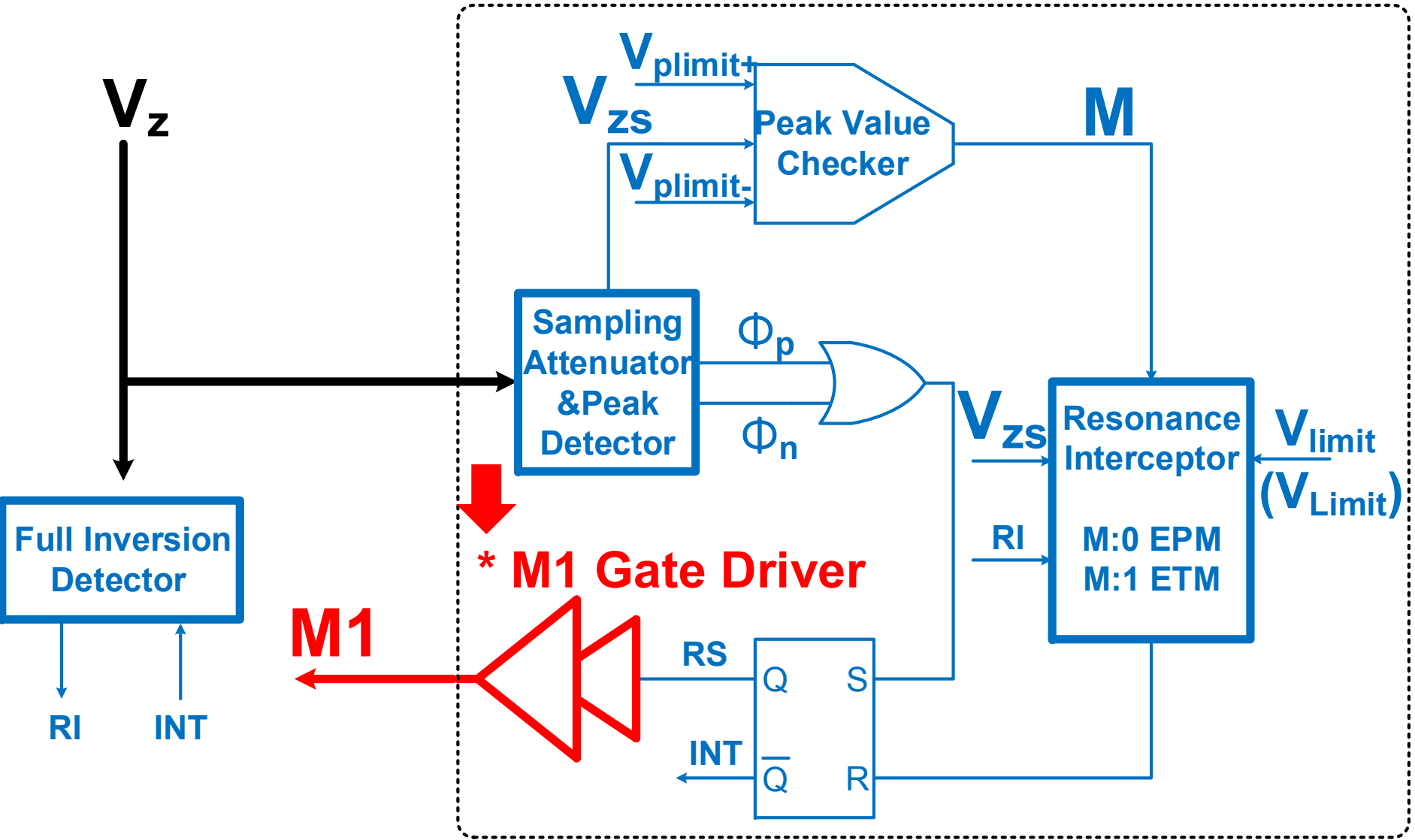
# Full Inversion Detector and Resonance Interceptor



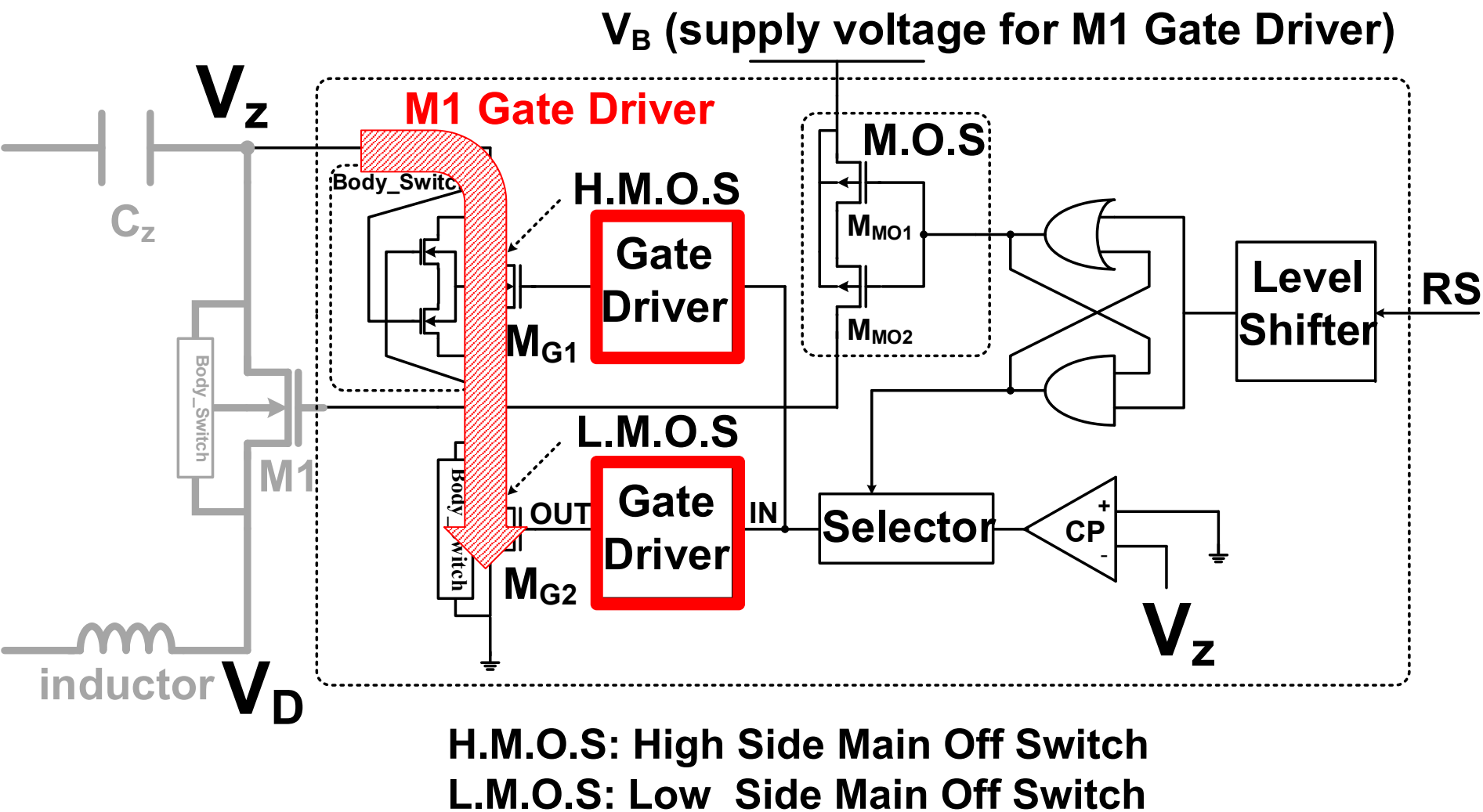
# Full Inversion Detector and Resonance Interceptor



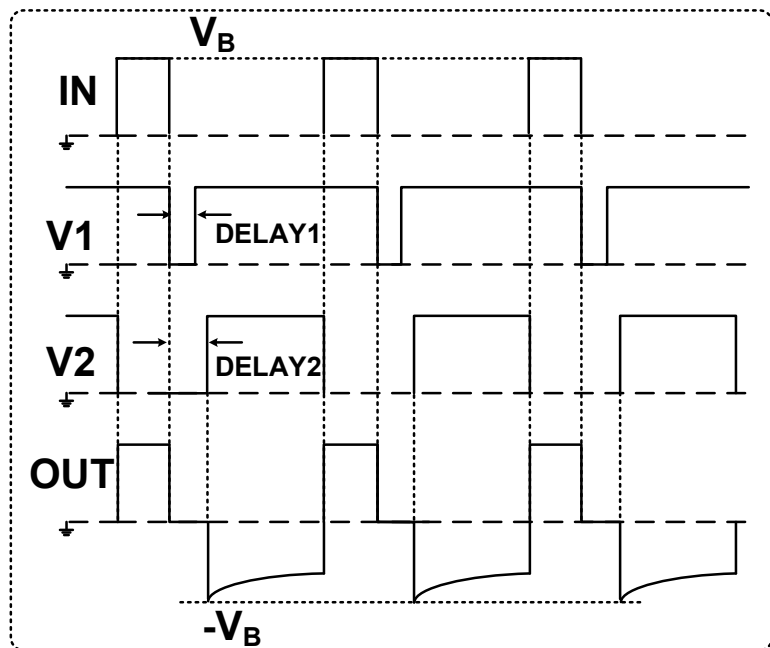
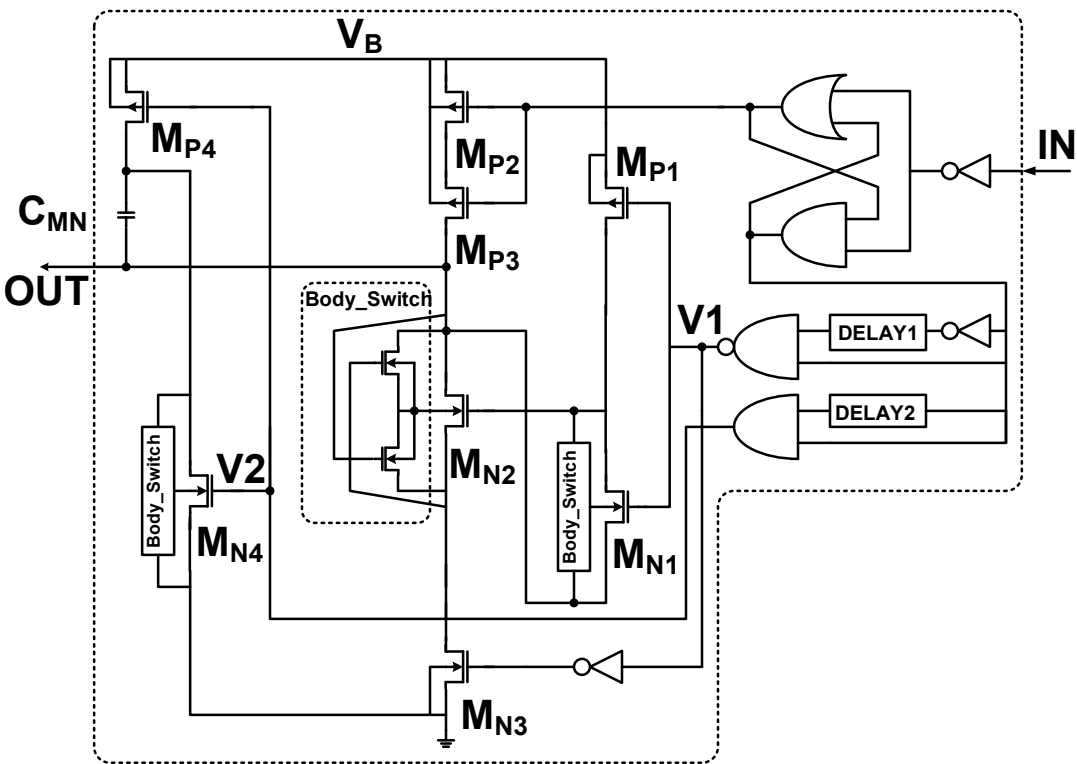
# PZT Resonance Controller



## Gate Driver for M1 switch



## Core Gate Driver for preventing the short circuit



Timing diagram of  $IN$ ,  $V1$ ,  $V2$  and  $OUT$

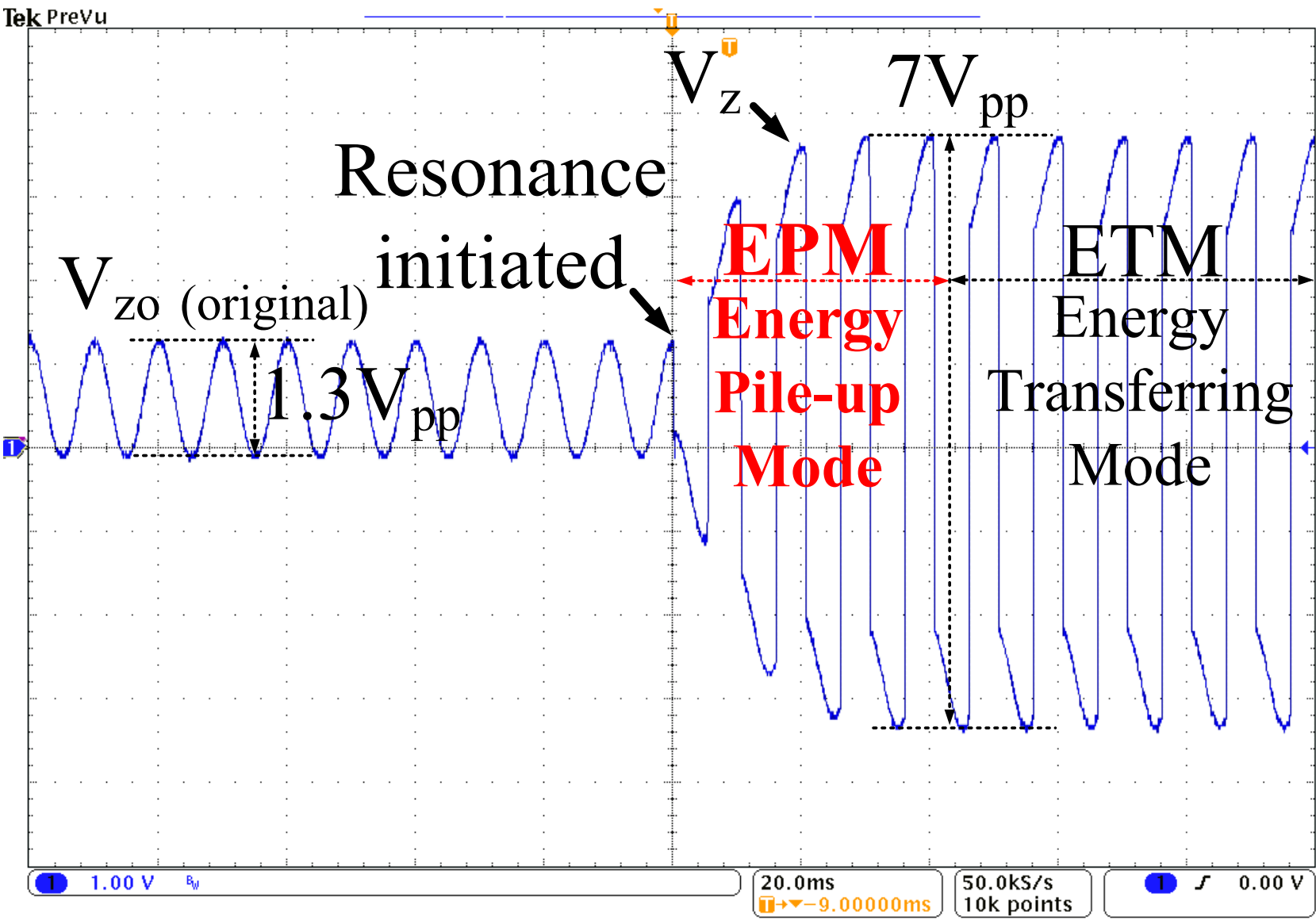
# Contents

---

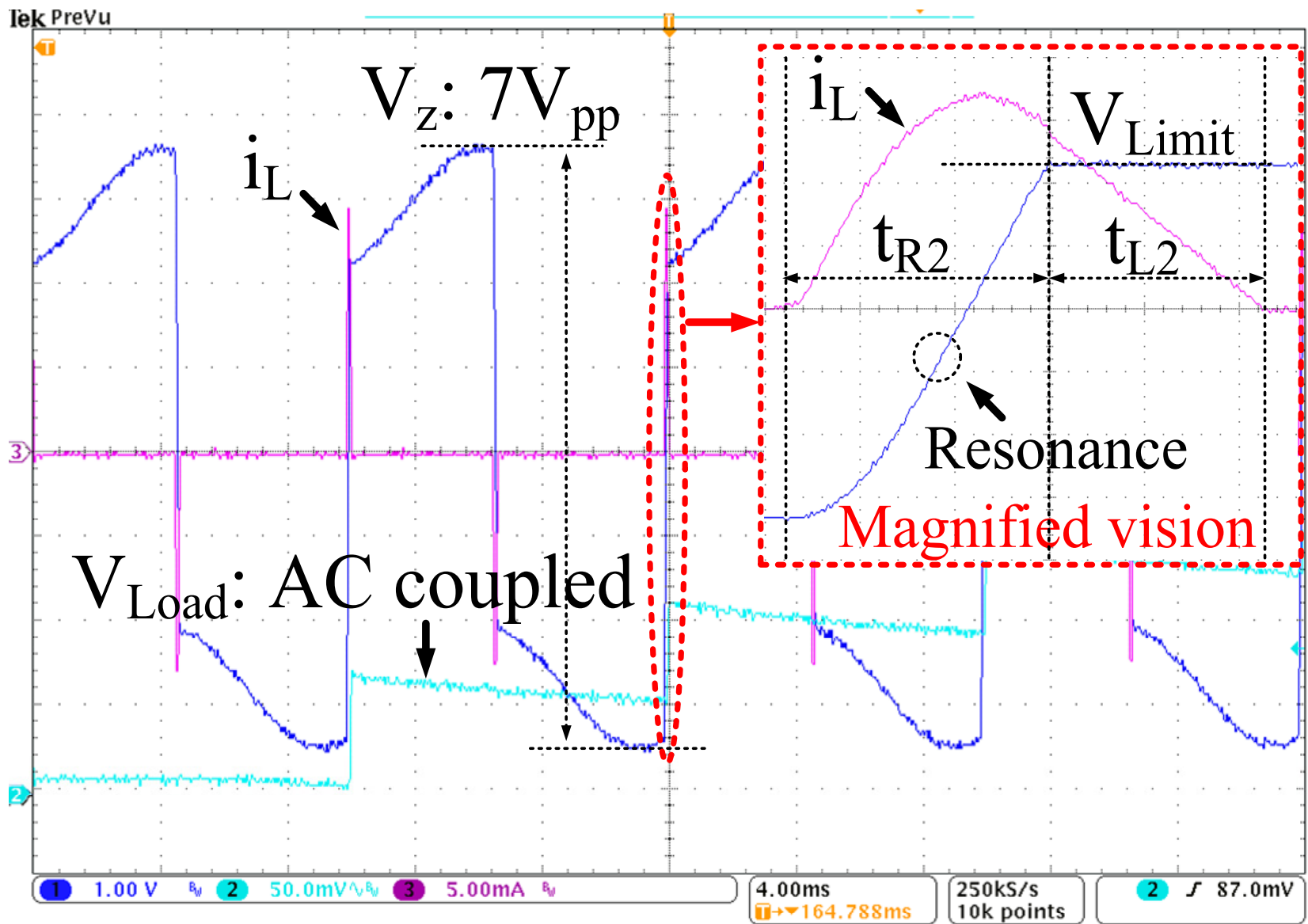
- Introduction about the Piezoelectric Transducer (PZT)
- The Previous works for Energy Extraction from PZT
- A Proposed Energy Pile-up Resonance Technique
- Chip Implementation
- **Measurement Results**
- Conclusion



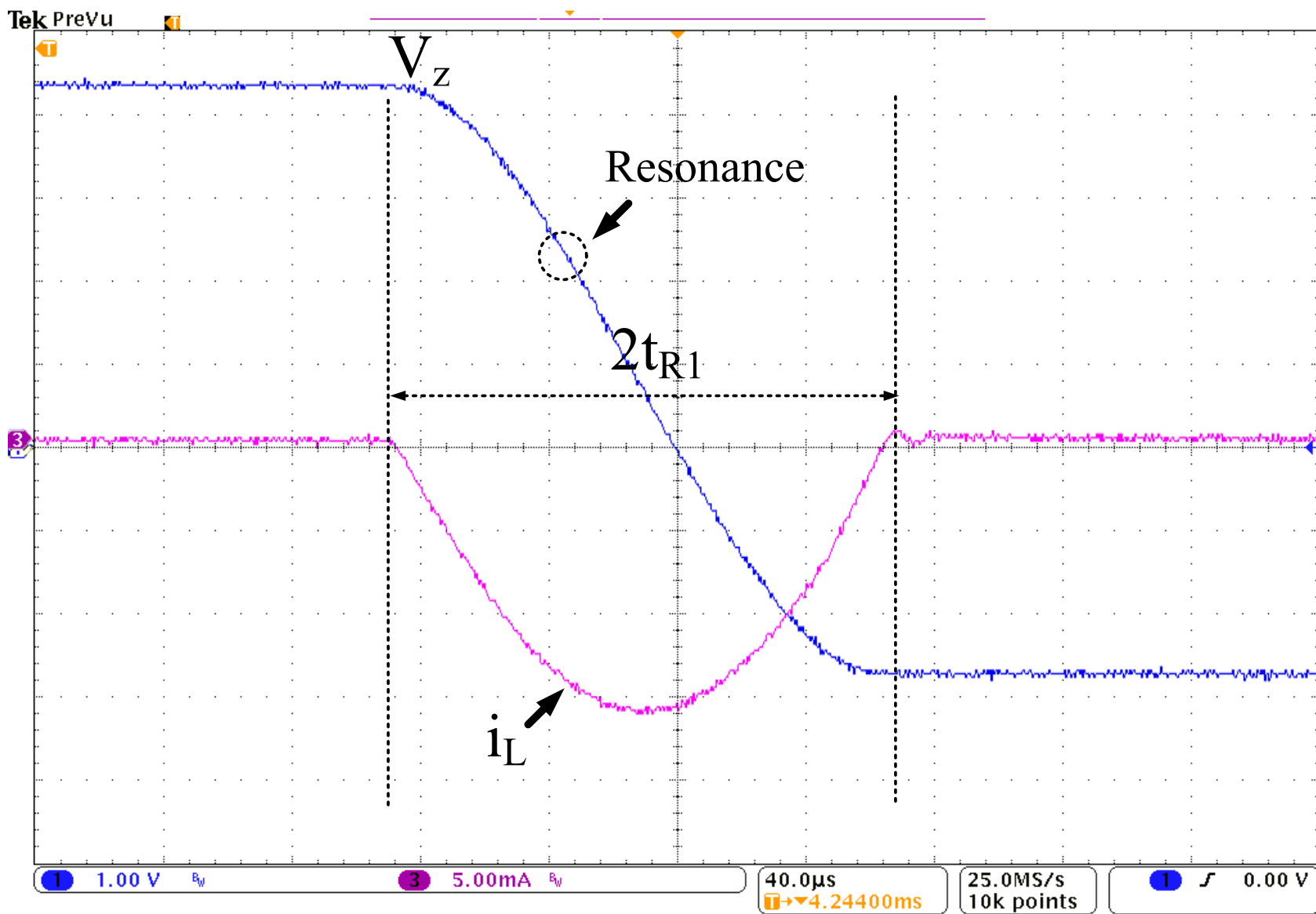
# Boosting $V_z$ by the Proposed Technique



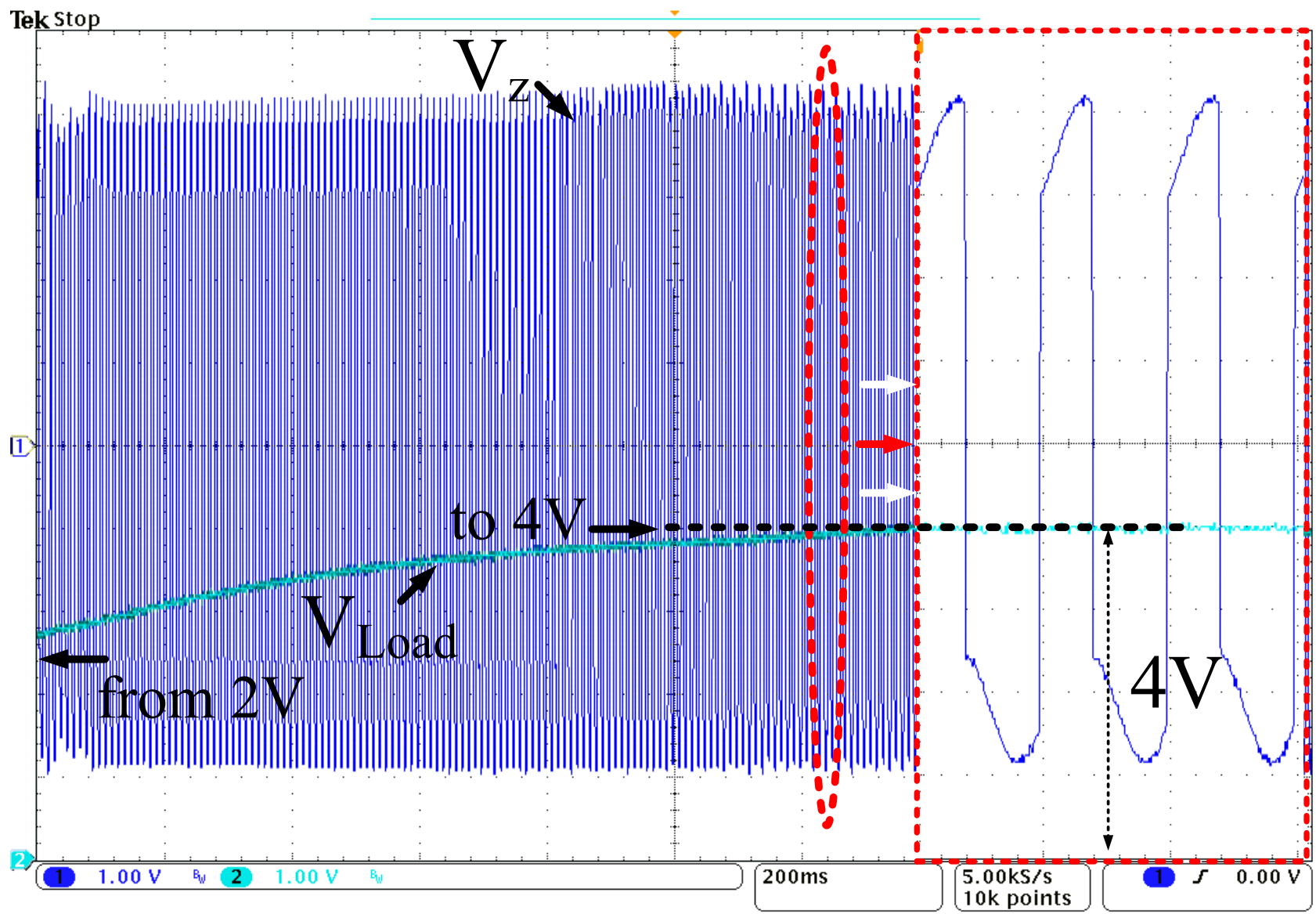
# Waveforms of the Energy Transferring Mode



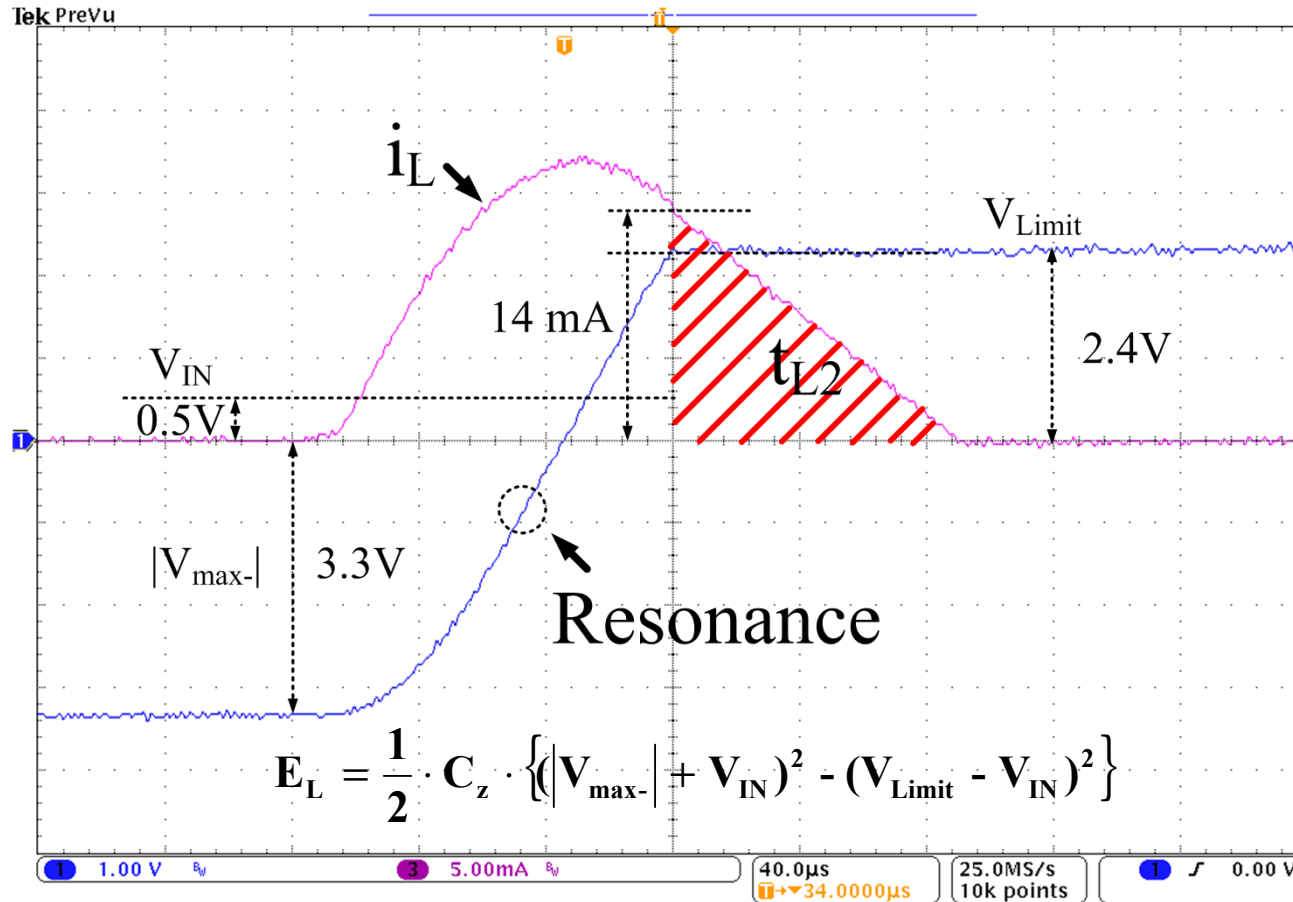
# Full Inversion of the $V_z$ at EPM and ETM



# Load Charging with Energy Pile-up Resonance Technique

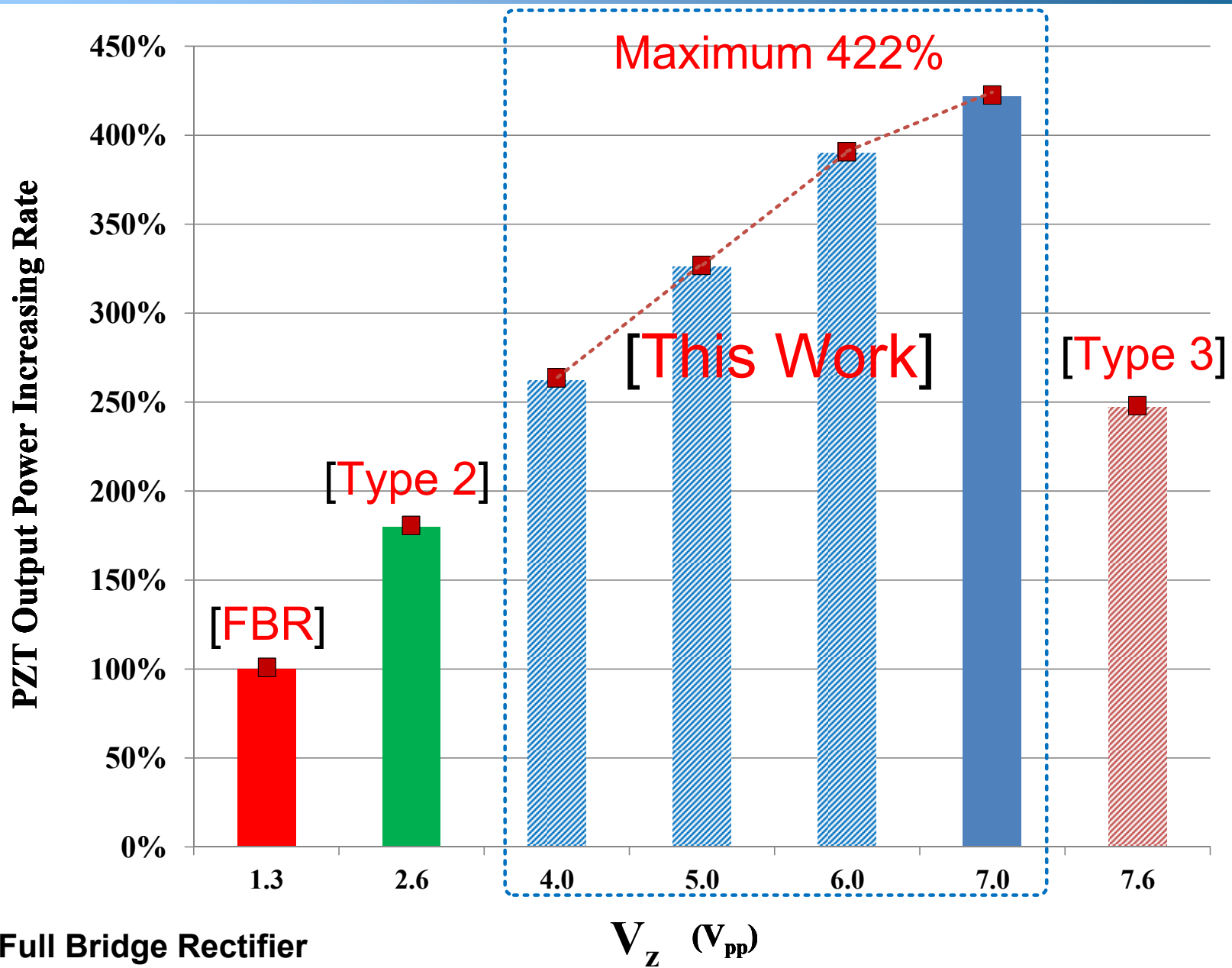


# Performance Analysis



- Theoretical output energy VS Real measured output energy
- Theoretical energy: 1.1913 μJ    Measured energy: 0.98 μJ
- **Real extracted energy is 82.2% of the expected energy**

# OPIR according to the amplitude of $V_z$



**FBR:** Full Bridge Rectifier

# Performance Summary

Parameter	[1]	[2]	[3]	This work
Input source	PZT	PZT	PZT	PZT&TEG
Load voltage	1.8V	4.5V	3.7V	4V
Extraction Technique	Resonance	Resonance	Investment Resonance	Energy Pile-up Resonance
*MOPIR (PZT)	280%**	180%**	247%** $\Omega$	422% $\Psi$
Efficiency (peak)	87% (Buck converter only)	49.9%	69.2%	74.9%
Process	0.35um	0.35um	0.35um	0.35um
Type	Rectifier with Buck converter	Battery Charger	Battery Charger	Battery Charger

\* : Maximum Output Power Increasing Rate    \*\*: calculated from the paper

$\Omega$ : When original PZT swing voltage  $2V_{pp}$

$\Psi$ : When original PZT swing voltage  $1.3V_{pp}$

# Conclusion

- $V_z$  is boosted until  $7 V_{pp}$  using original swing  $1.3 V_{pp}$ .
- With the  $V_z$  of  $7 V_{pp}$ , the EHI charges the load from 2V to 4V.
- When the  $V_z$  is  $7 V_{pp}$ , the 422% energy is extracted compared to the conventional technique (full bridge).
- Real extracted energy is 82.2% of the expected energy extraction and the amount of extracted energy is maximum 1  $\mu$ J



Thank you

---

**Thank You**

# **A 43V 400mW-to-21W Global-Search-Based Photovoltaic Energy Harvester with 350 $\mu$ s Transient Time, 99.9% MPPT Efficiency, and 94% Power Efficiency**

**Sandip Uprety, Hoi Lee**

**Integrated Power Laboratory  
The University of Texas at Dallas, USA**



# Outline

---

- **Background and Motivation**
- Proposed Energy Harvester Architecture and Algorithm
- Irradiance Aware Adaptive Frequency Power Controller (IAAFPC) and Gate Driver
- Pulse-Integration Based Maximum Power Point Tracker (PI-MPPT)
- Measurement Results
- Conclusion

# Solar Energy Harvesting



Solar Powered Lighting



Remote Monitoring Stations



Mobile Devices Charging Platforms



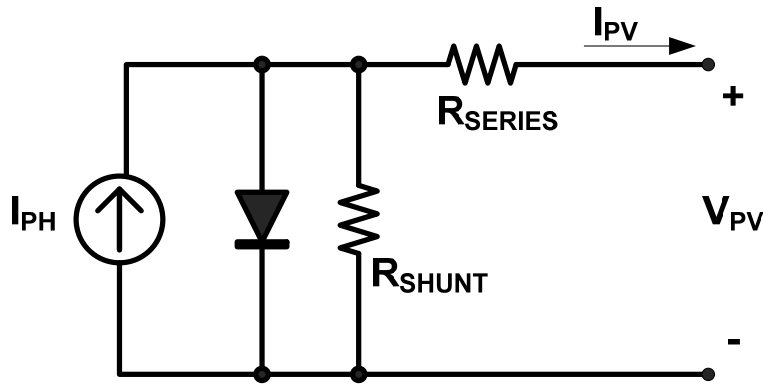
Emergency Systems



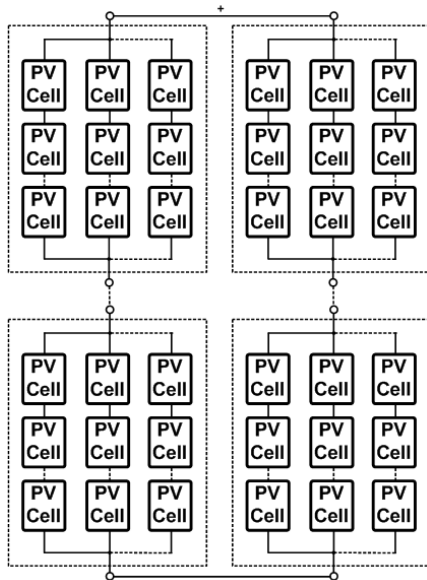
Various applications of 10's of Watt Solar Panels

- Photovoltaic cells have the **highest energy density**.
- Many **standalone systems** can be solar-powered.

# Solar Panel Characteristics

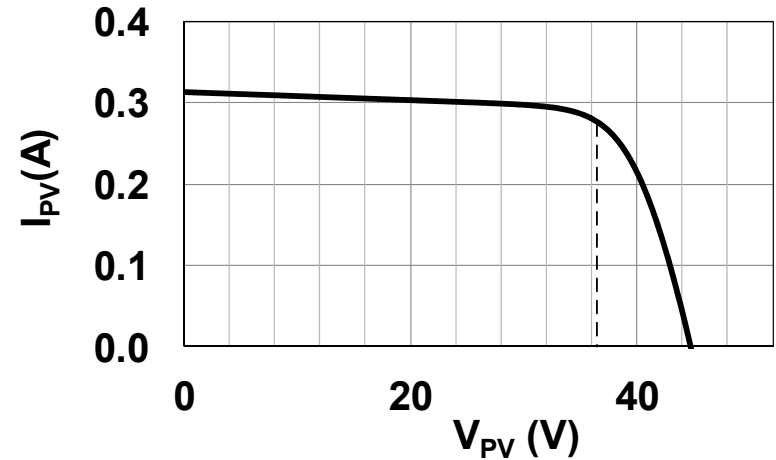


Lumped electrical model of a **PV cell**

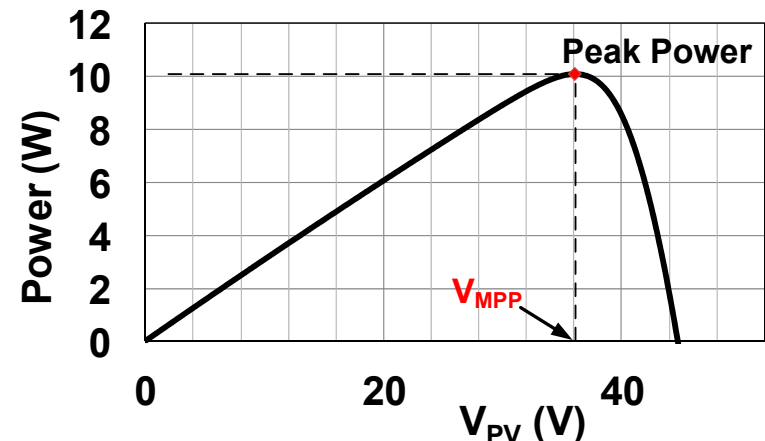


PV modules forming a **Solar Panel**

**SP I-V** Characteristic Curve

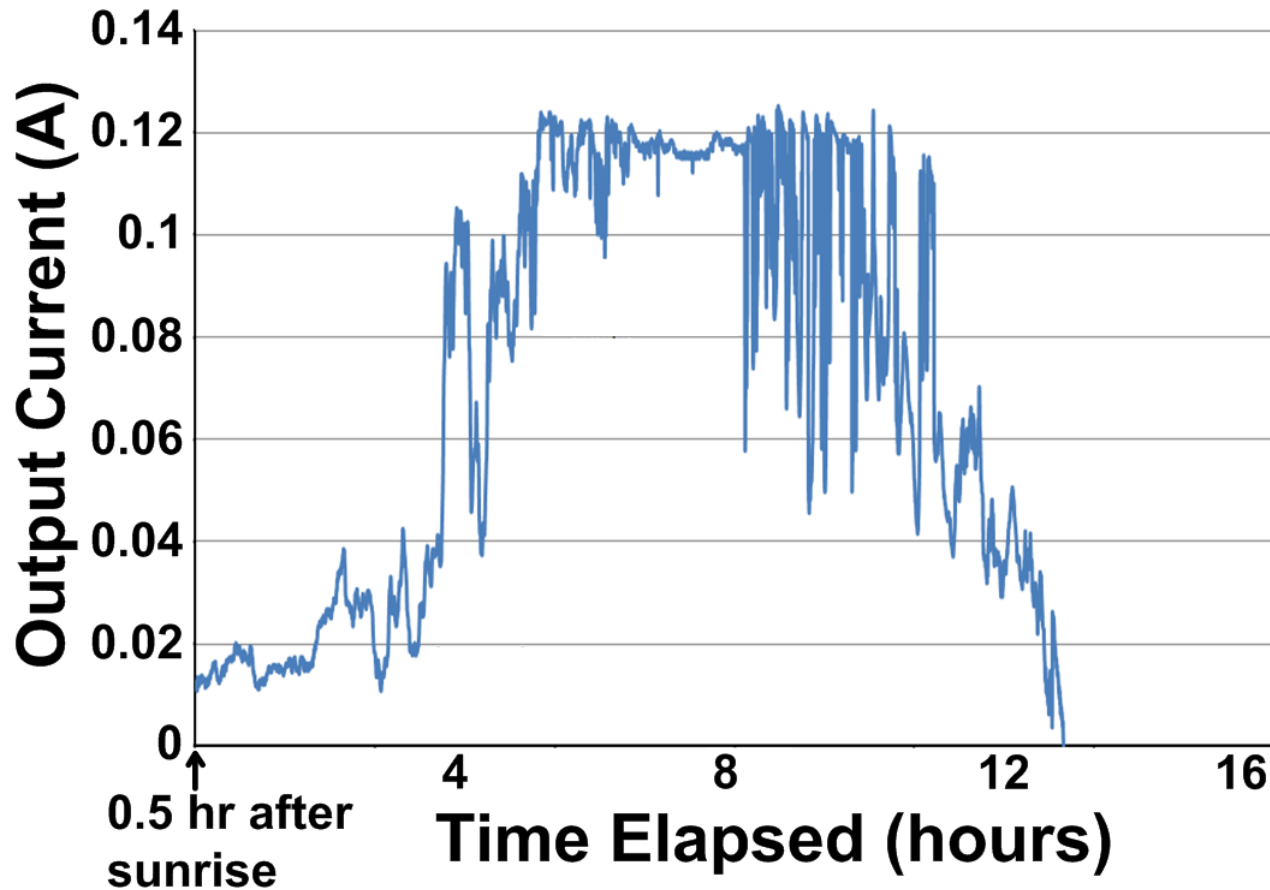


**SP P-V** Characteristic Curve



**Maximum Power Point Tracking (MPPT)**

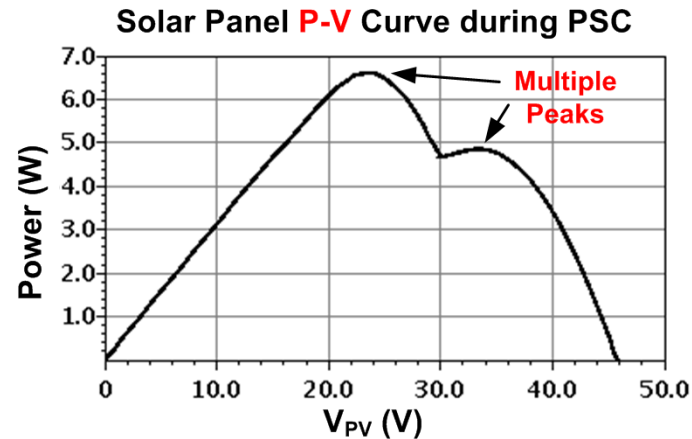
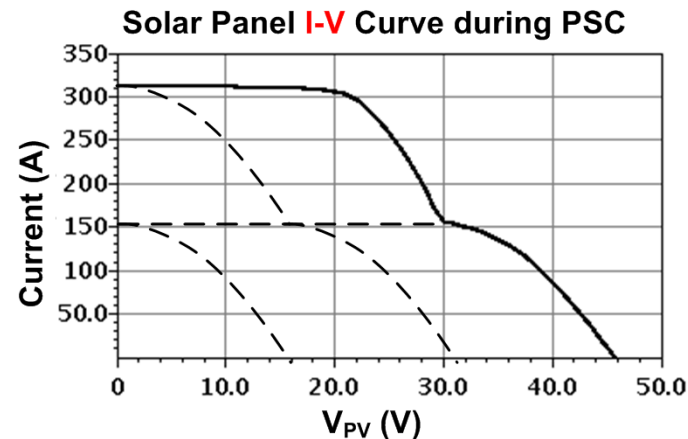
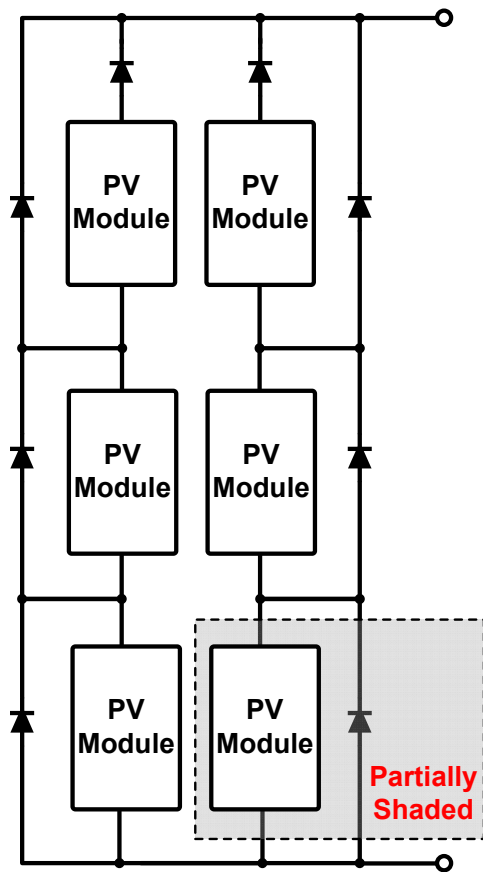
# Variation of SP Output during the Day



- **High MPPT efficiency and high power efficiency across wide input-power range are indispensable.**

Source: [www.vernier.com/innovate/the-effect-of-sky-conditions-on-solar-panel-power-output/](http://www.vernier.com/innovate/the-effect-of-sky-conditions-on-solar-panel-power-output/)

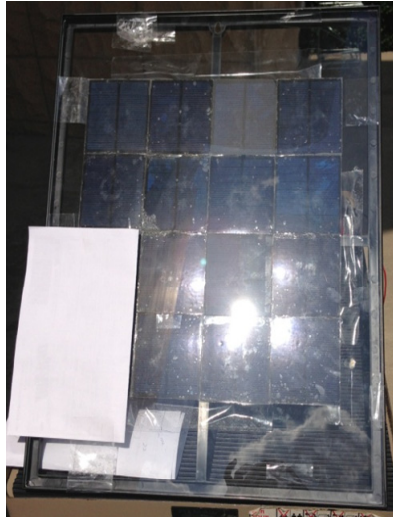
# Effect of Partial Shading on PV Modules



- For a large size SP, **Partial Shading Conditions (PSC)** can occur due to birds, trees, buildings and other objects.
- **Multiple local maxima** are present during PSC.

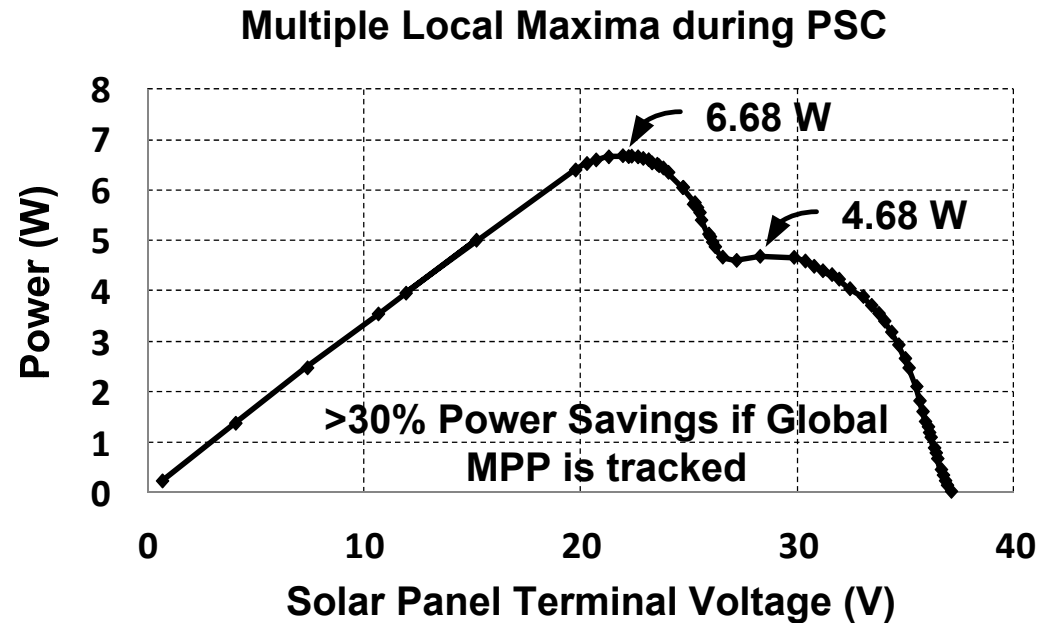


# Design Challenges due to PSC



Measured SP  
characteristic  
curve during PSC

2 strings in parallel  
2/8 modules of one string  
shaded for PSC test



- P&O and hill-climbing algorithms get **stuck at the lower local maximum.**
- The state-of-the-art integrated EHs **cannot perform Global MPPT (GMPPT).**

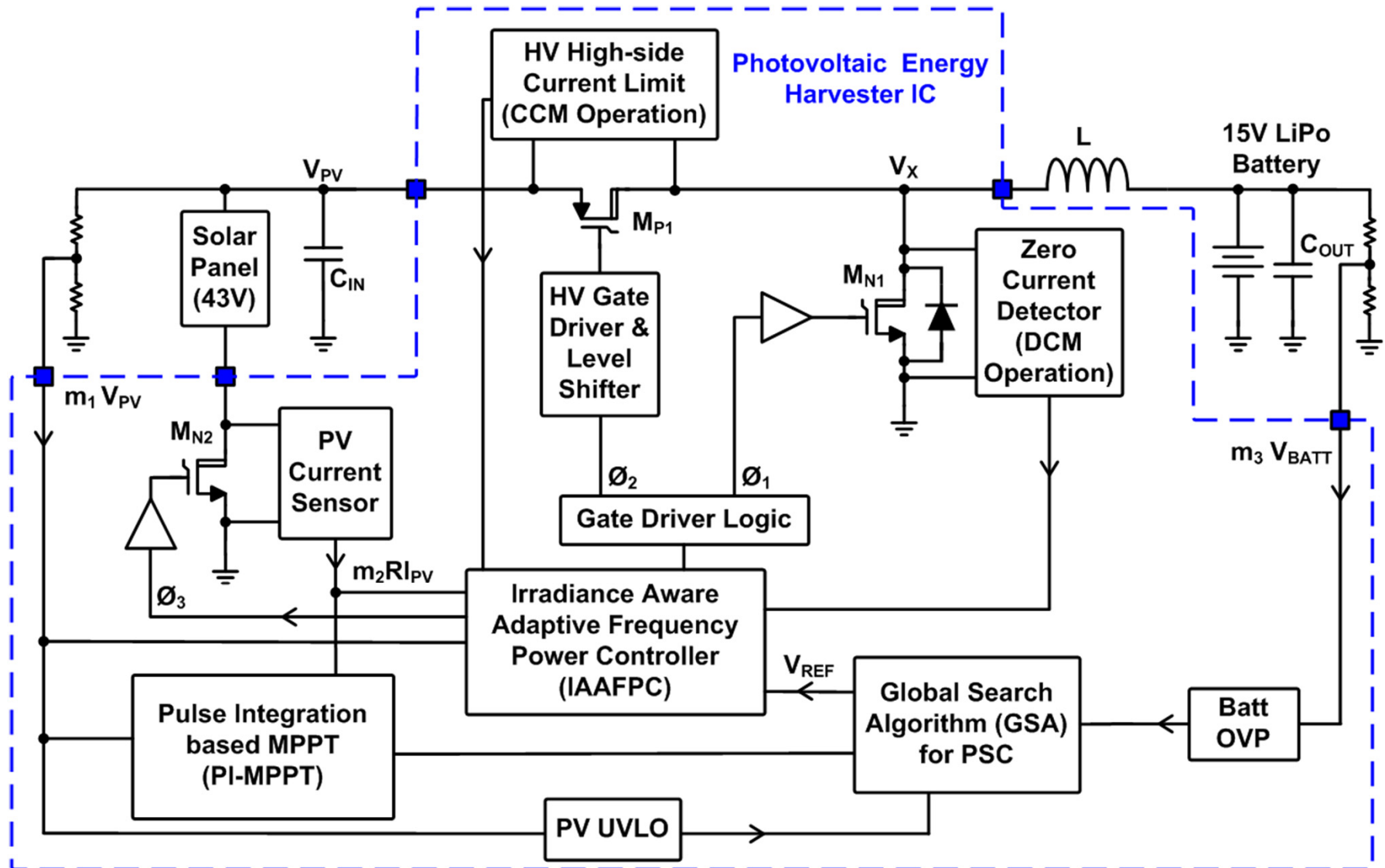


# Outline

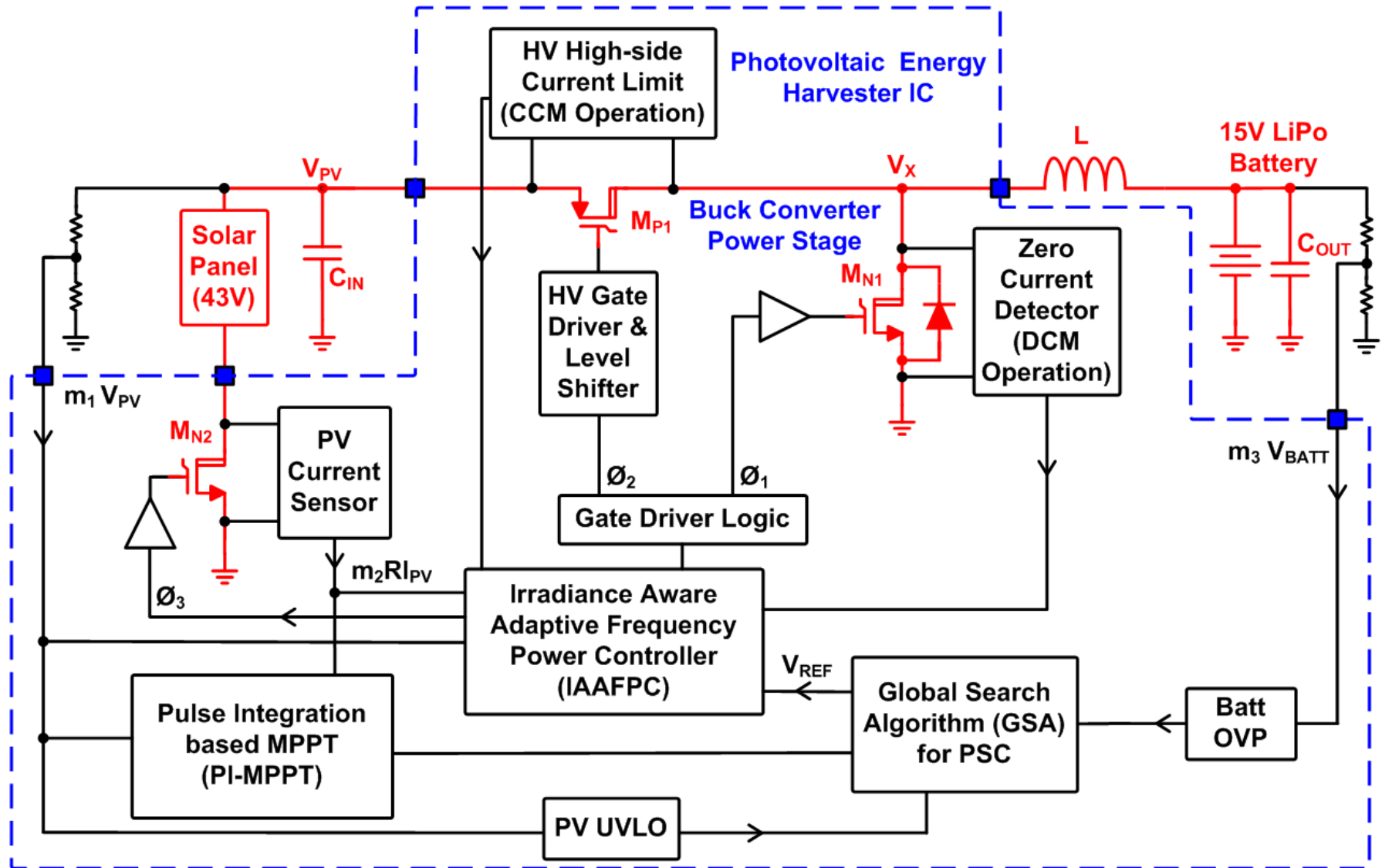
---

- Background and Motivation
- **Proposed Energy Harvester Architecture and Algorithm**
- Irradiance Aware Adaptive Frequency Power Controller (IAAFPC) and Gate Driver
- Pulse-Integration Based Maximum Power Point Tracker (PI-MPPT)
- Measurement Results
- Conclusion

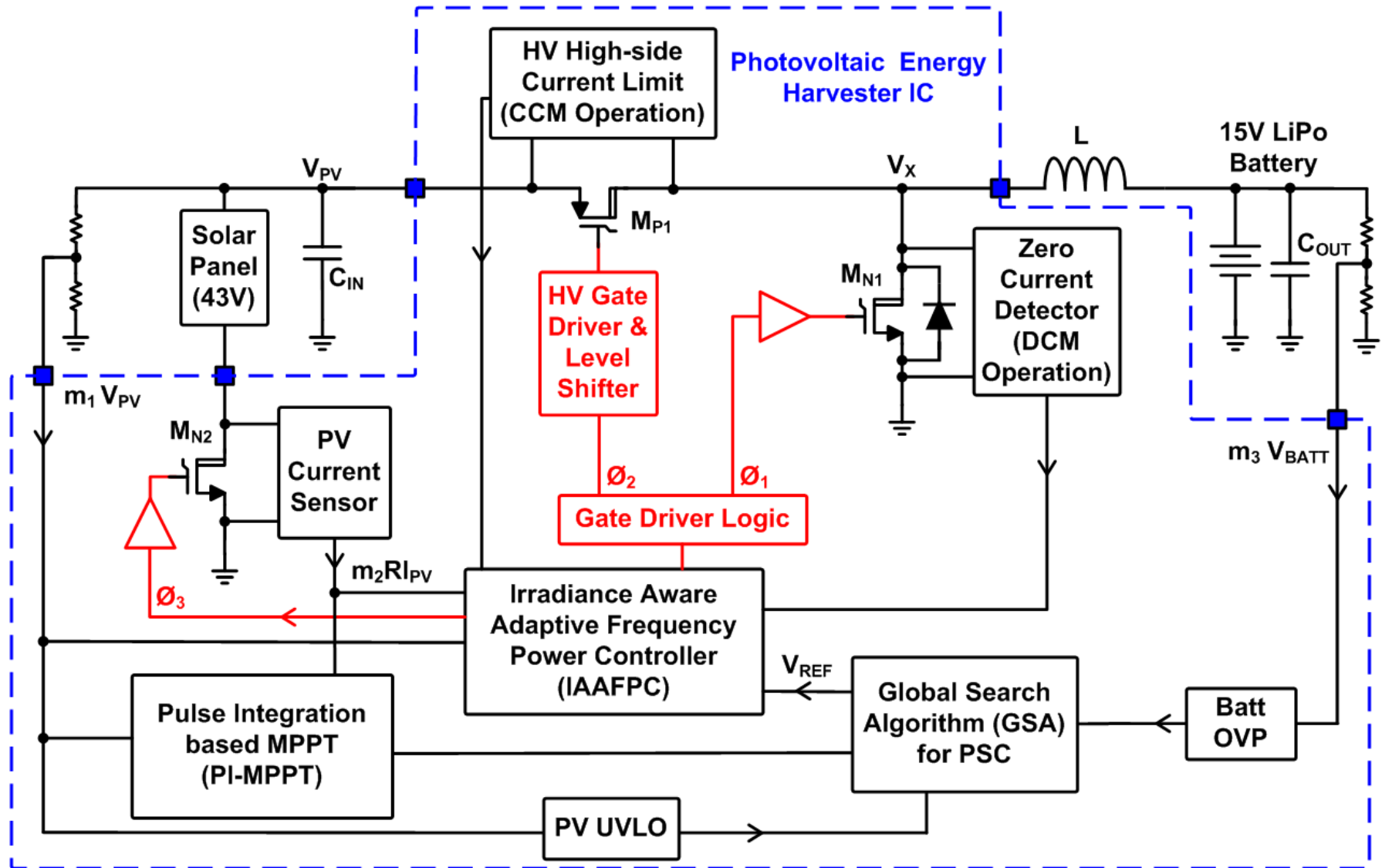
# Proposed Energy Harvester Architecture



# Proposed Energy Harvester Architecture

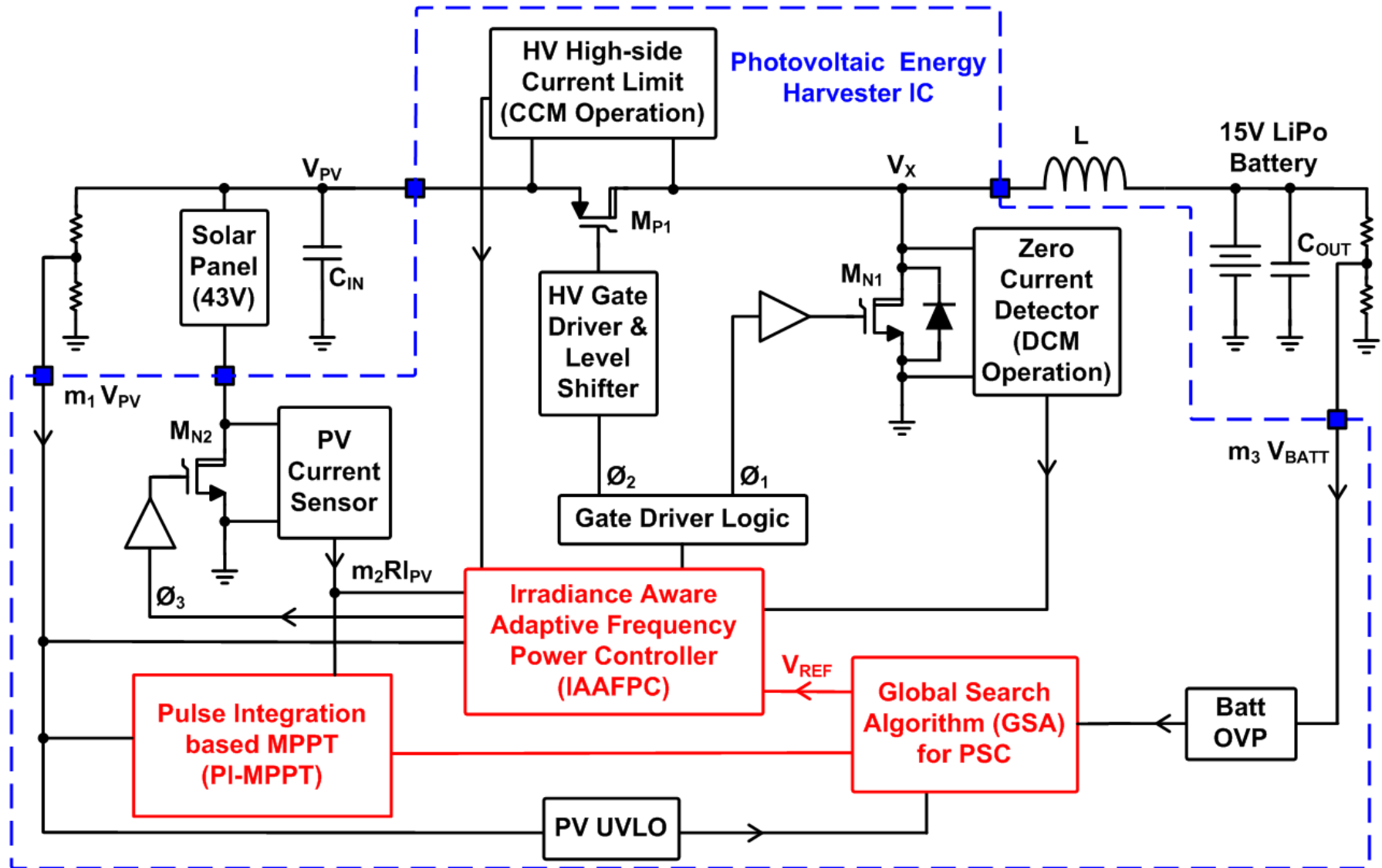


# Proposed Energy Harvester Architecture

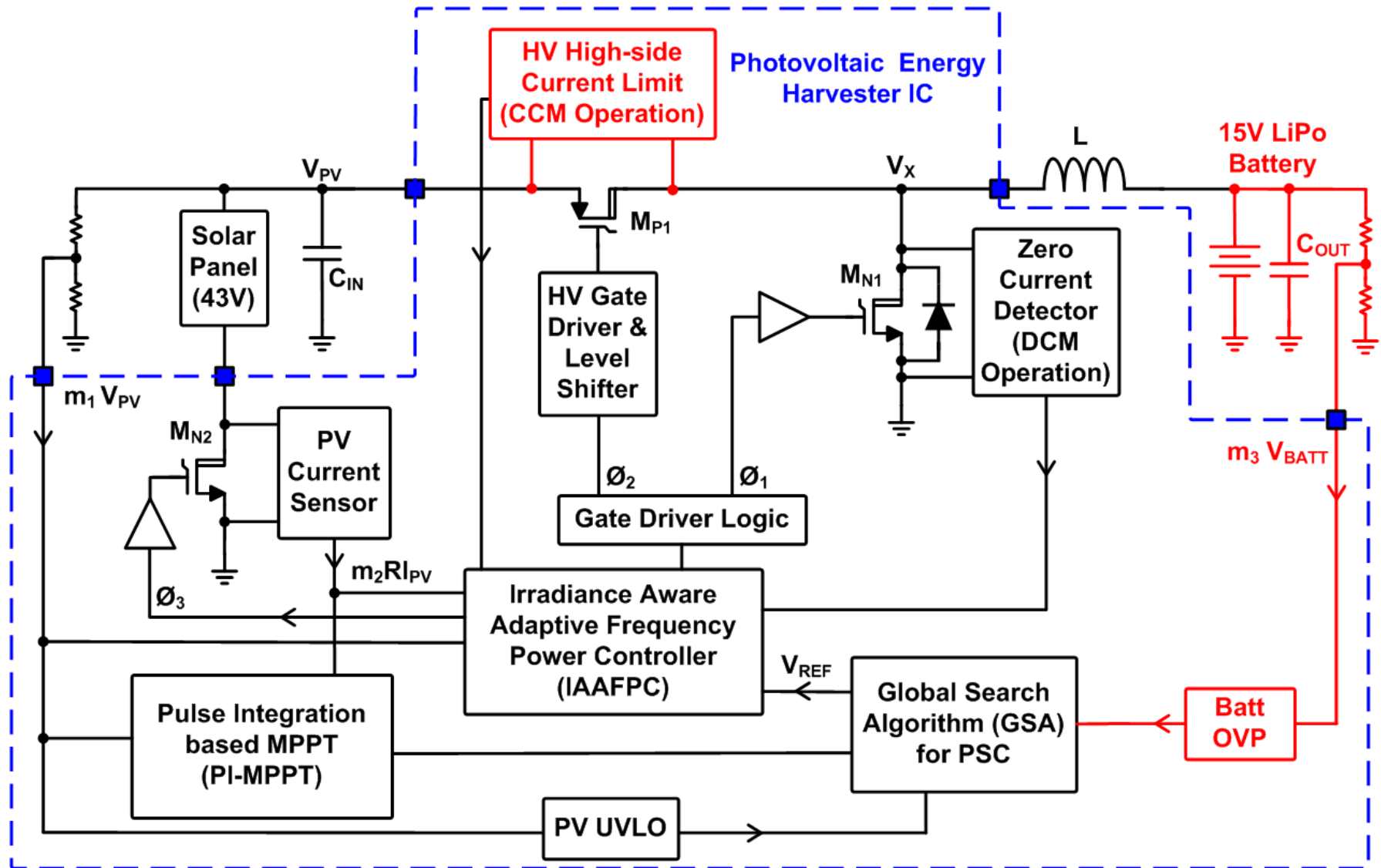


23.6: A 43V 400mW-to-21W Global-Search-Based Photovoltaic Energy Harvester with 350 $\mu$ s Transient Time, 99.9% MPPT Efficiency, and 94% Power Efficiency

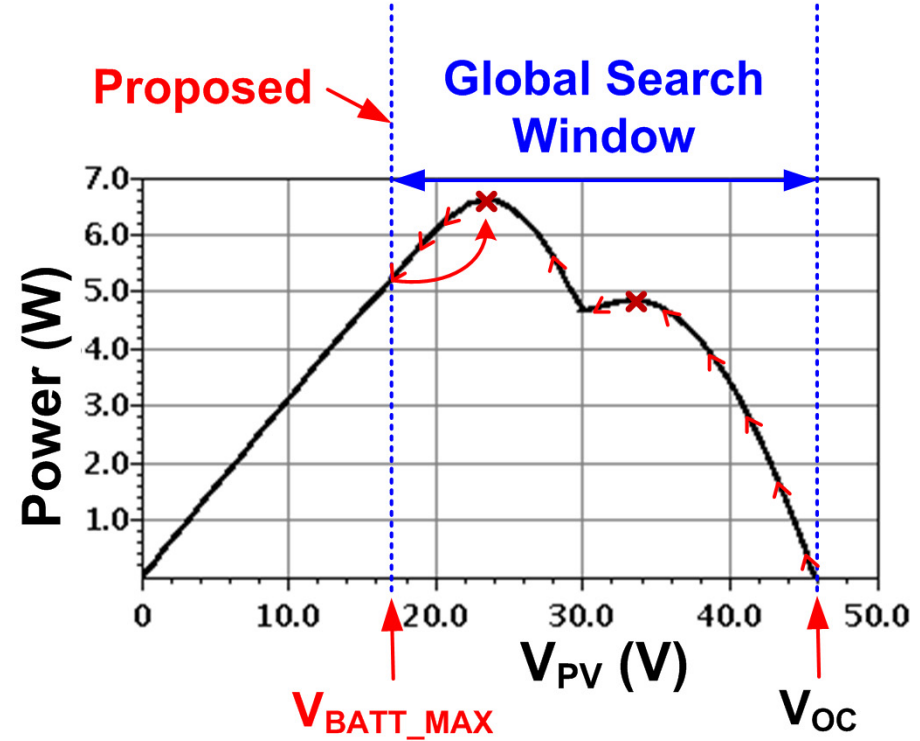
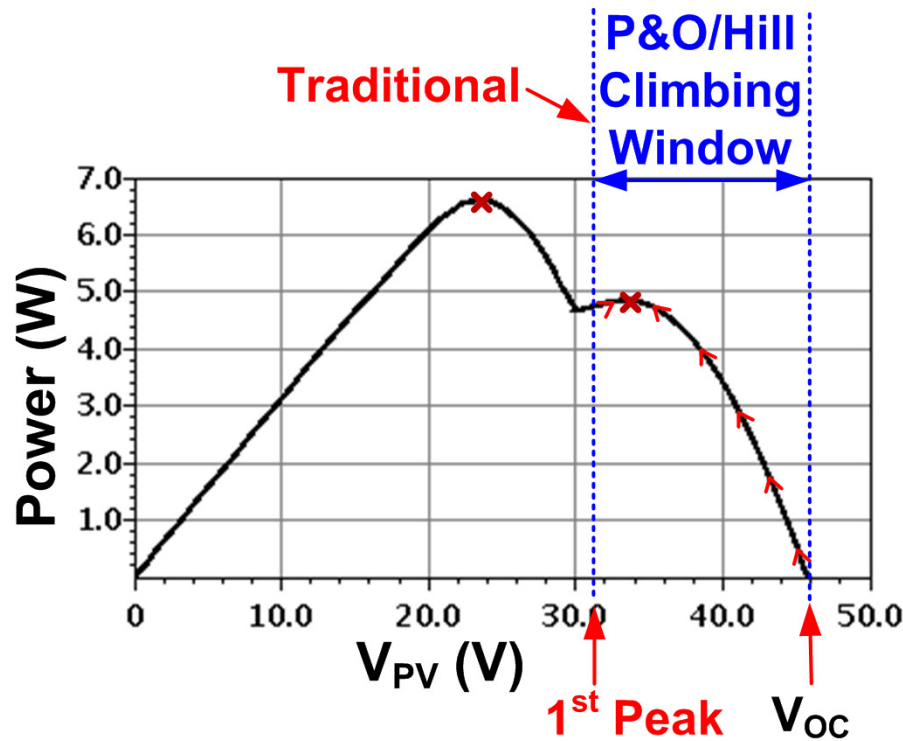
# Proposed Energy Harvester Architecture



# Proposed Energy Harvester Architecture

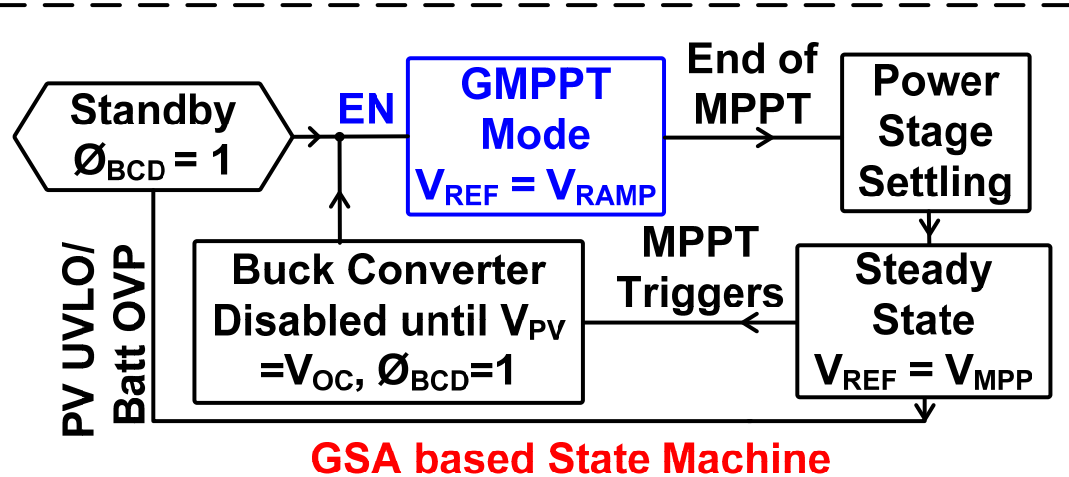


# Global Search Algorithm (GSA)

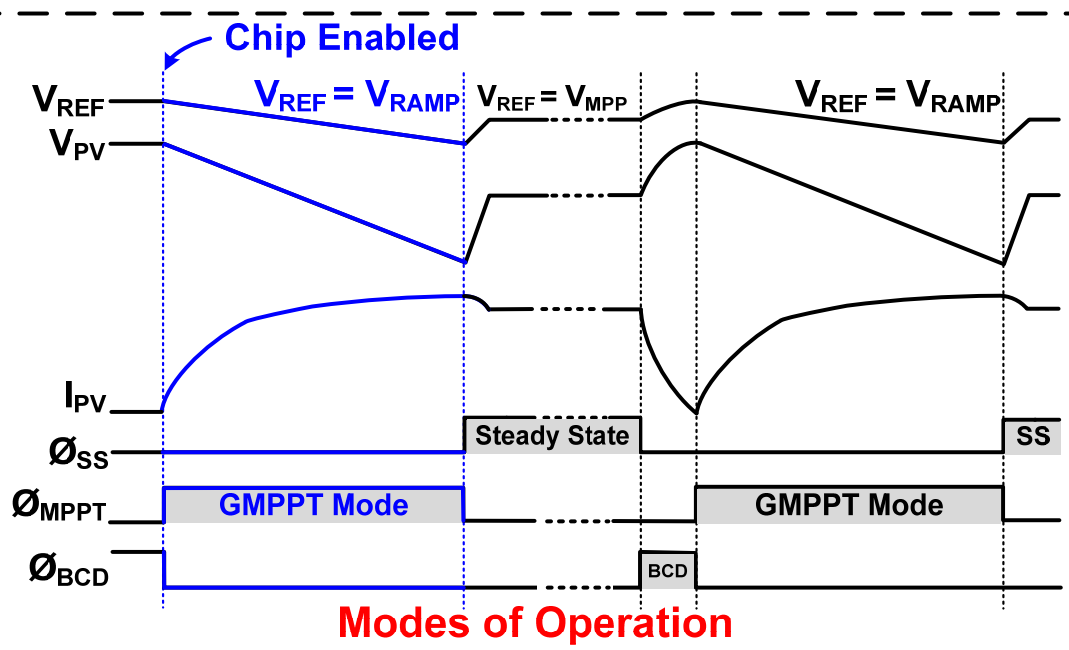


- GSA provides **extended search window**.
- GSA enables **instantaneous power computation** in GMPPT mode.
- **Ripple-based IAAFPC**, low  $C_{IN}$  and **high-operation-frequency EH** allows  $V_{PV}$  to ramp down quickly.

# Global Search Algorithm (1)



➤ After startup and in periodic normal operation, system enters **GMPPT mode**.

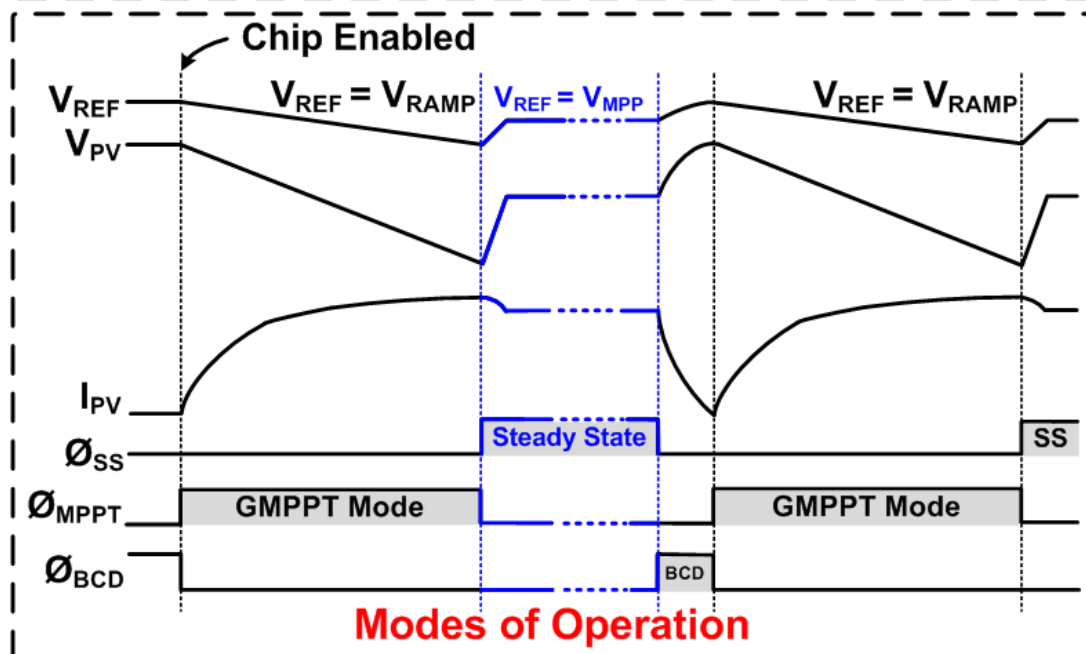
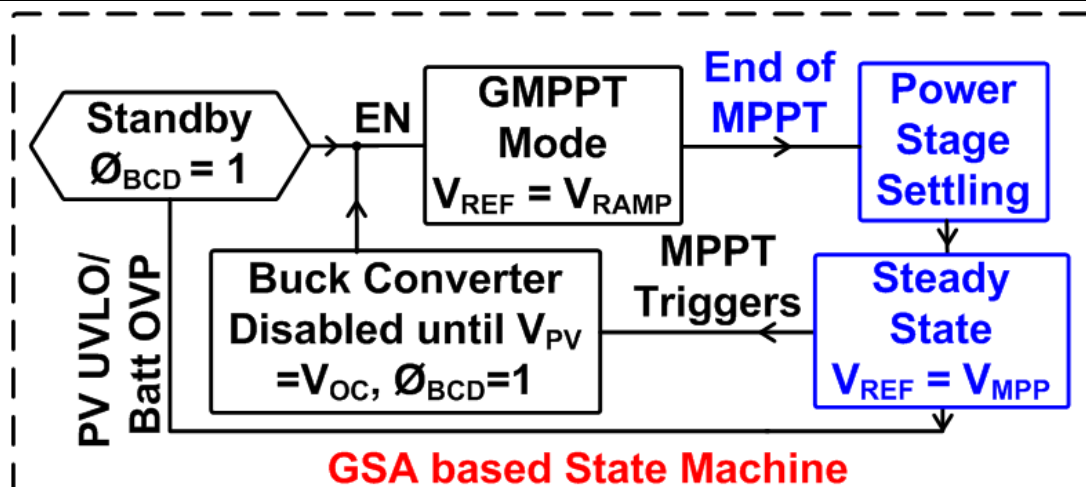


➤ A closed-loop feedback controls  $V_{PV}$  using  $V_{REF}$ .

➤ **Instantaneous SP output power** is calculated using  $V_{PV}$  and  $I_{PV}$  information.

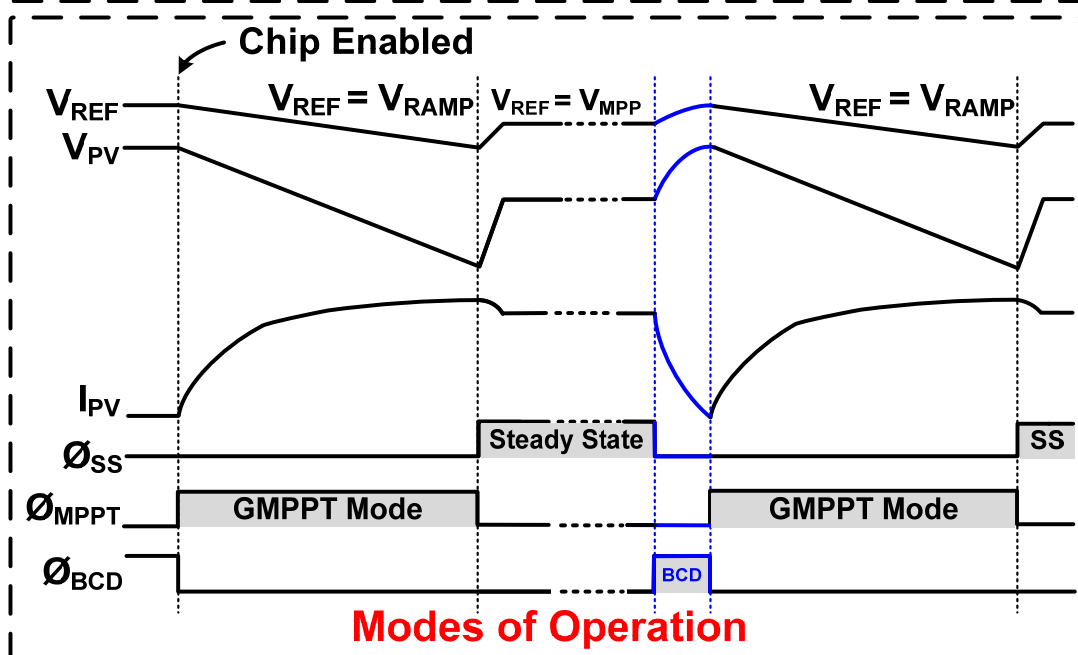
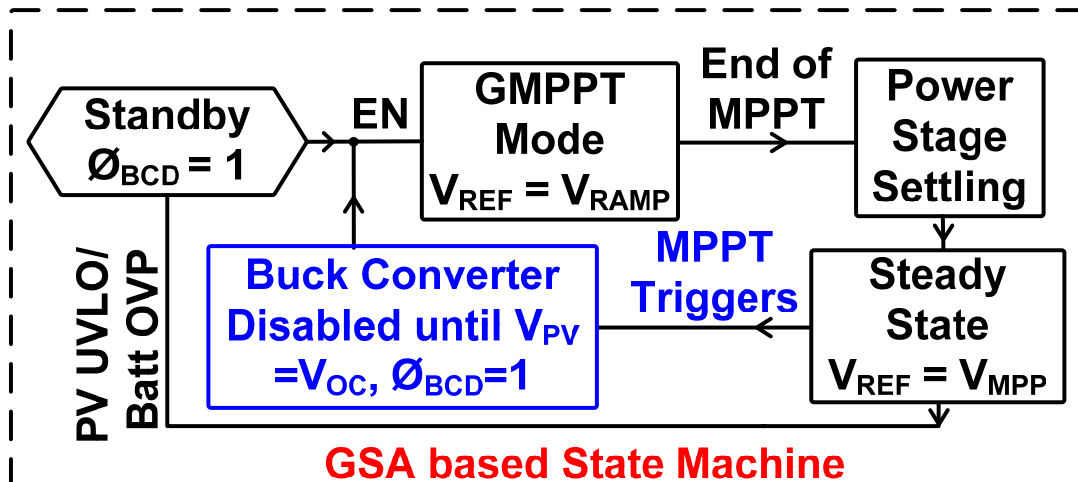


# Global Search Algorithm (2)



- After the GMPPT mode,  $V_{REF} = V_{MPP}$ .
- The power stage settles and transitions to the **steady-state operation**.
- The EH extracts power from the **SP** at its **GMPP**.
- The duration of steady-state is programmable.

# Global Search Algorithm (3)

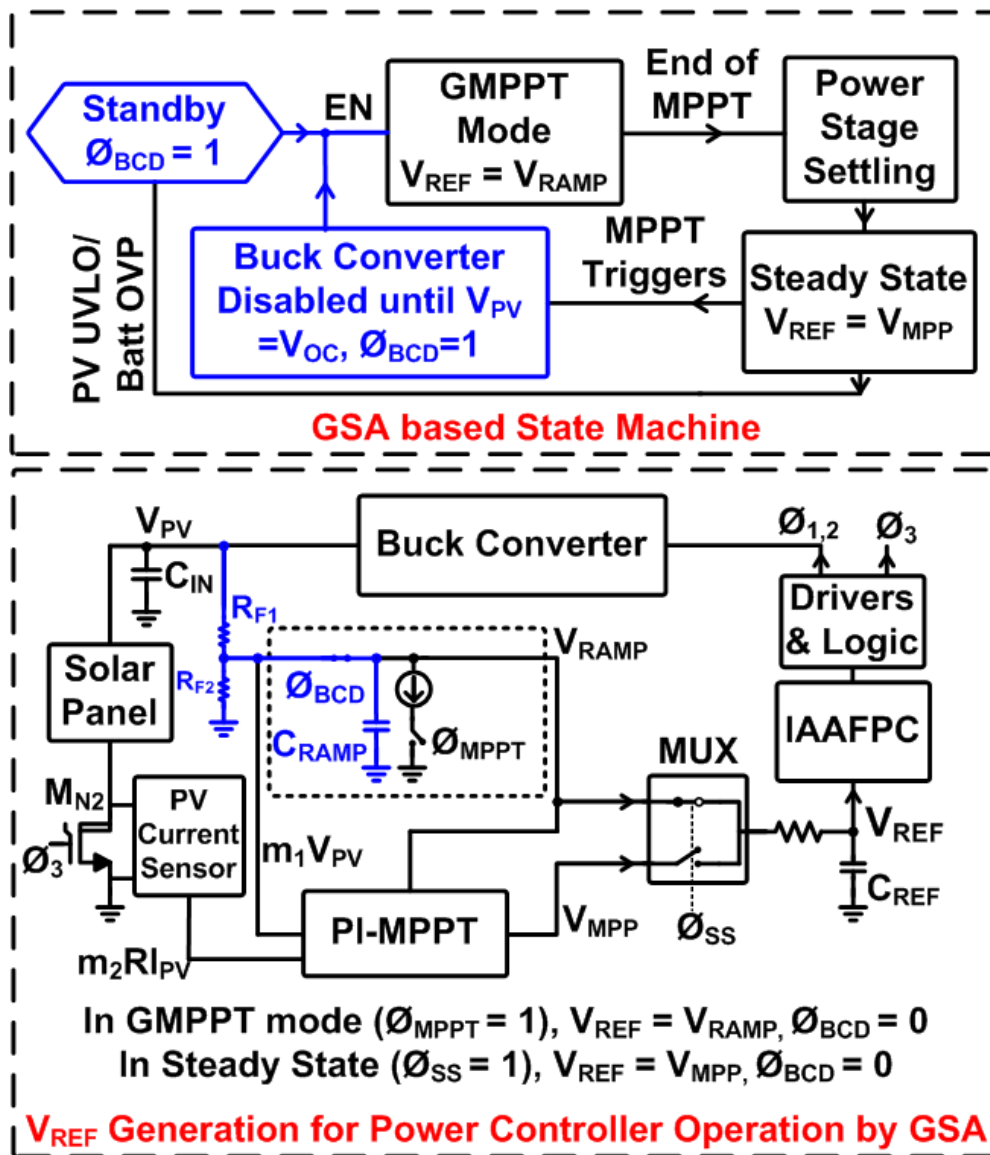


➤ After the steady-state timer expires, **MPPT is triggered**.

➤  $V_{PV}$  is charged to  $V_{OC}$  during **Buck Converter Disabled (BCD)** mode.

➤ EH then goes to **GMPPT mode** unless **SP UVLO** or  $V_{BATT}$  over-voltage protection is triggered.

# $V_{REF}$ Generation during BCD Mode



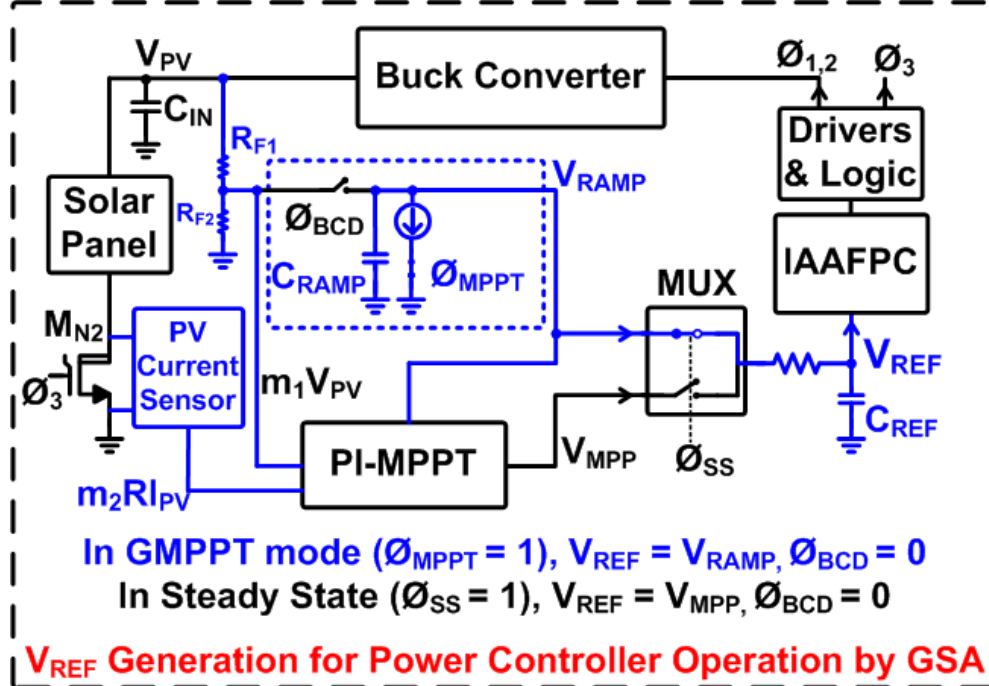
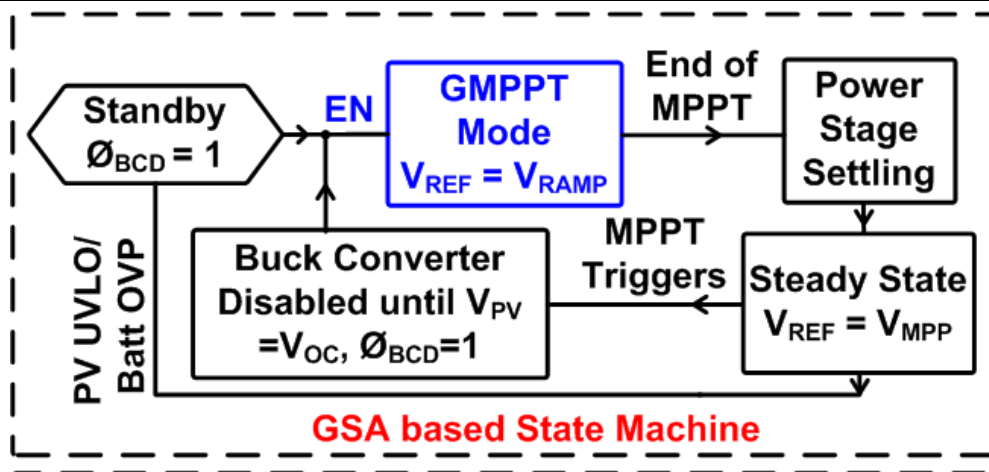
➤ In Buck Converter Disabled (**BCD**) mode:  
 $\emptyset_{BCD} = 1$  and  $\emptyset_{MPPT} = 0$ .

➤ 
$$V_{RAMP} = \frac{R_{F2}}{R_{F1} + R_{F2}} V_{PV}$$

➤  $\emptyset_{SS} = 0$ , and  $V_{REF} = V_{RAMP}$ .

➤  $V_{REF}$  is updated to Solar Panel's open cell voltage.

# $V_{REF}$ Generation during GMPPT mode



➤ In **GMPPT** mode:

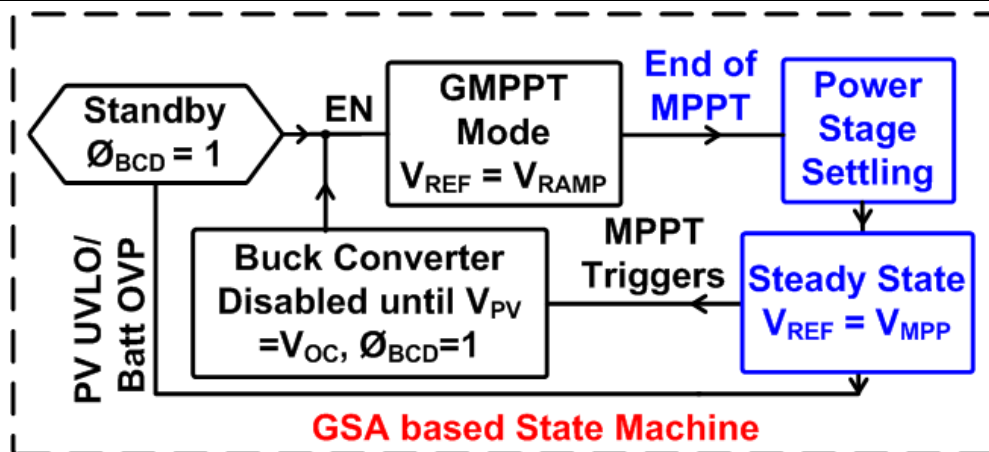
$\emptyset_{SS} = 0$ , and  $V_{REF} = V_{RAMP}$ .

➤  $\emptyset_{BCD} = 0$  and  $\emptyset_{MPPT} = 1$ .

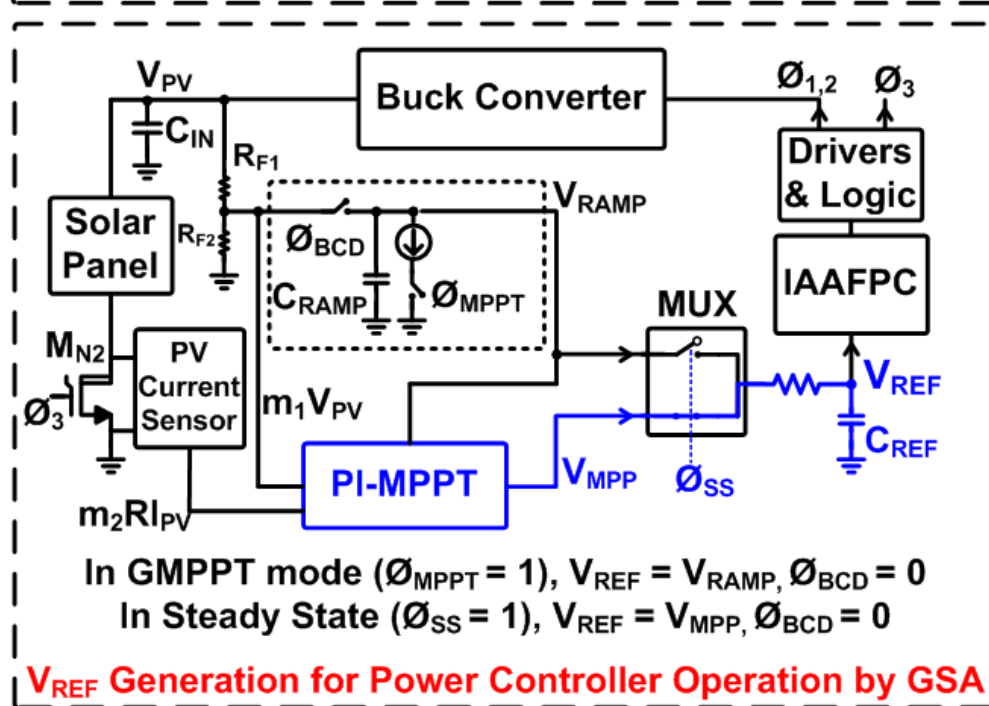
➤ C<sub>RAMP</sub> is discharged by a constant current source.

➤ **PI-MPPT** calculates instantaneous Solar Panel output **power**.

# $V_{REF}$ during Steady-State Operation



GSA based State Machine



$V_{REF}$  Generation for Power Controller Operation by GSA

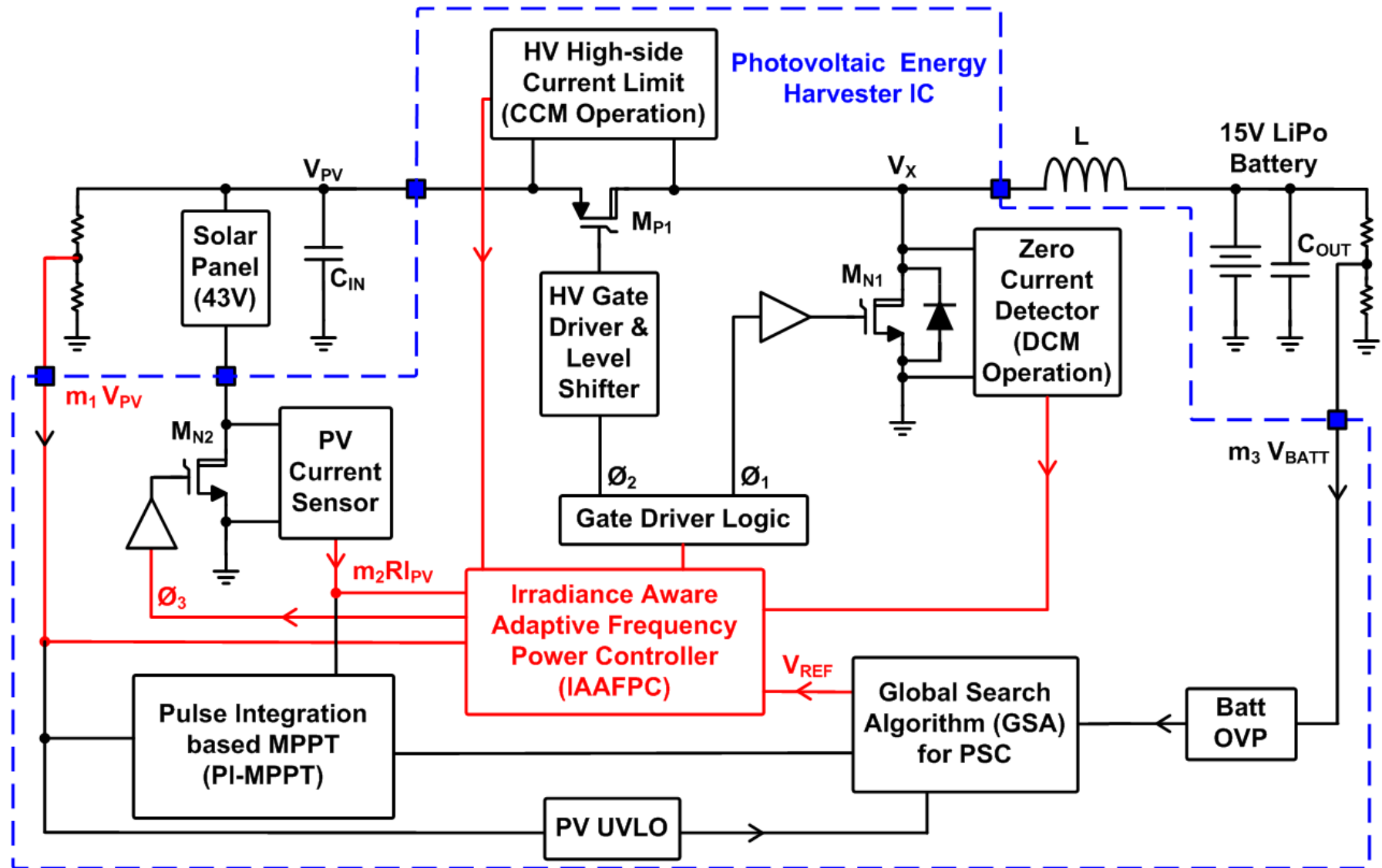
- In **steady state**:  
 $\emptyset_{SS} = 1$ , and  $V_{REF} = V_{MPP}$ .
- $\emptyset_{BCD} = 0$  and  $\emptyset_{MPPT} = 0$ .
- IAAFPC uses  $V_{REF}$  to operate Solar Panel its global peak power.

# Outline

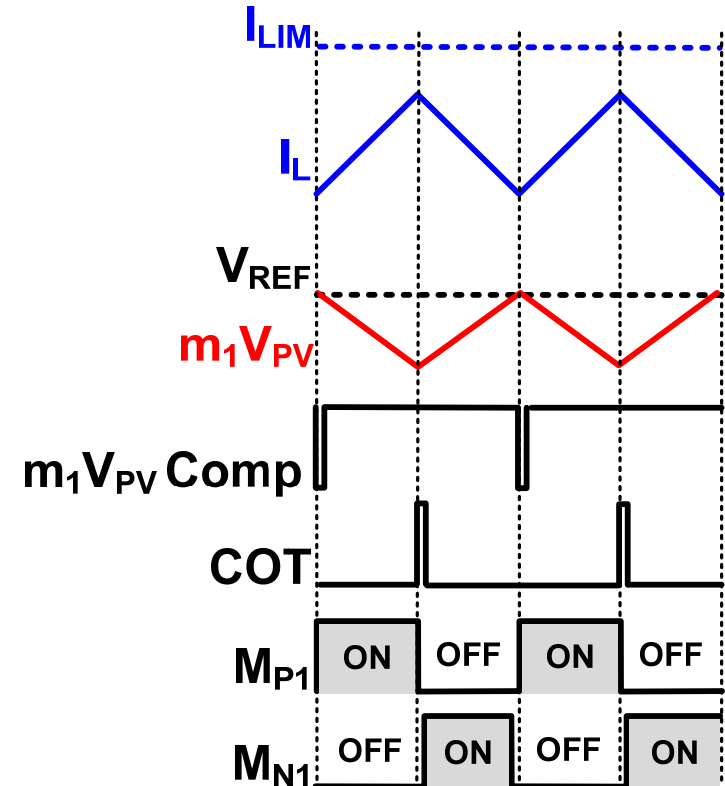
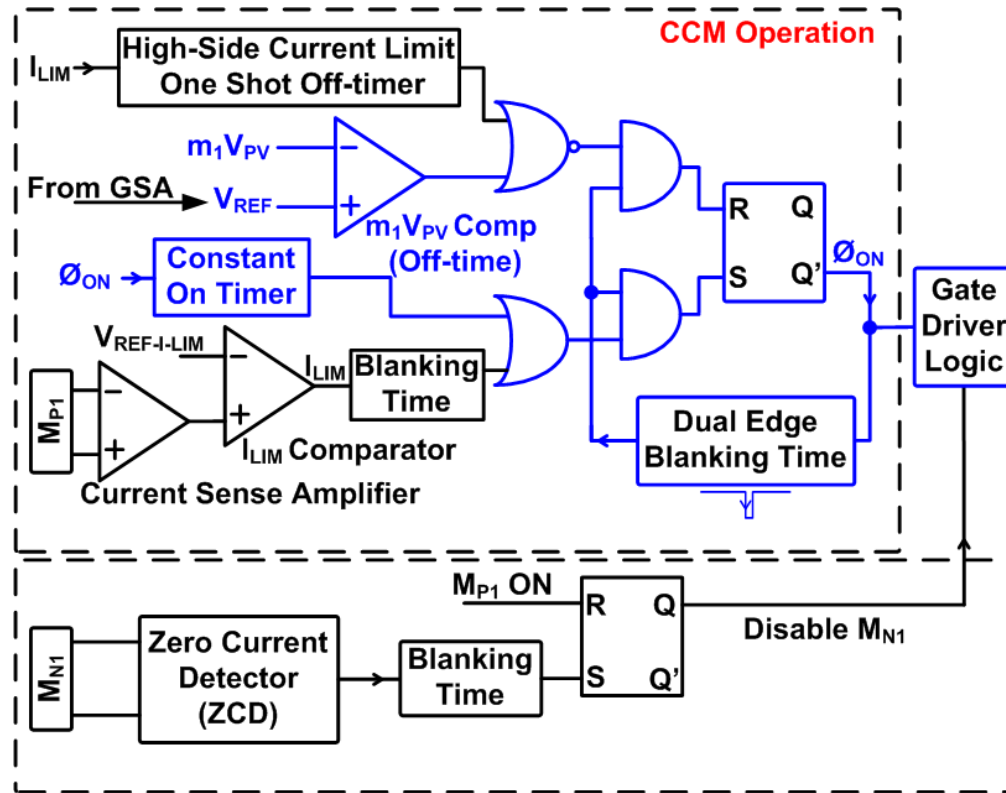
---

- Background and Motivation
- Proposed Energy Harvester Architecture and Algorithm
- **Irradiance Aware Adaptive Frequency Power Controller (IAAFPC) and Gate Driver**
- Pulse-Integration Based Maximum Power Point Tracker (PI-MPPT)
- Measurement Results
- Conclusion

# Irradiance Aware Adaptive Frequency Power Controller Operation



# IAAFPC Operation: High Irradiance

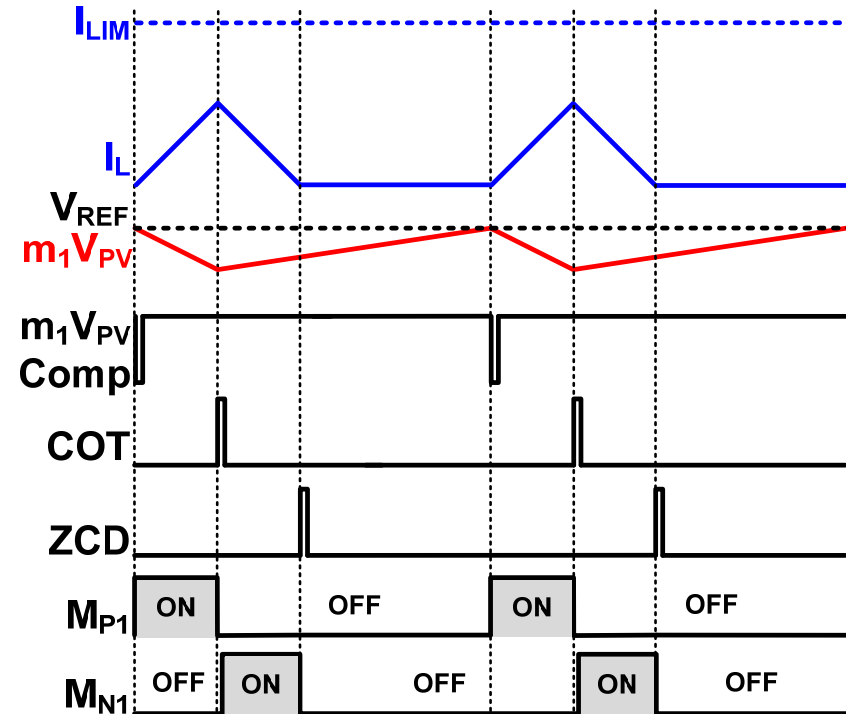
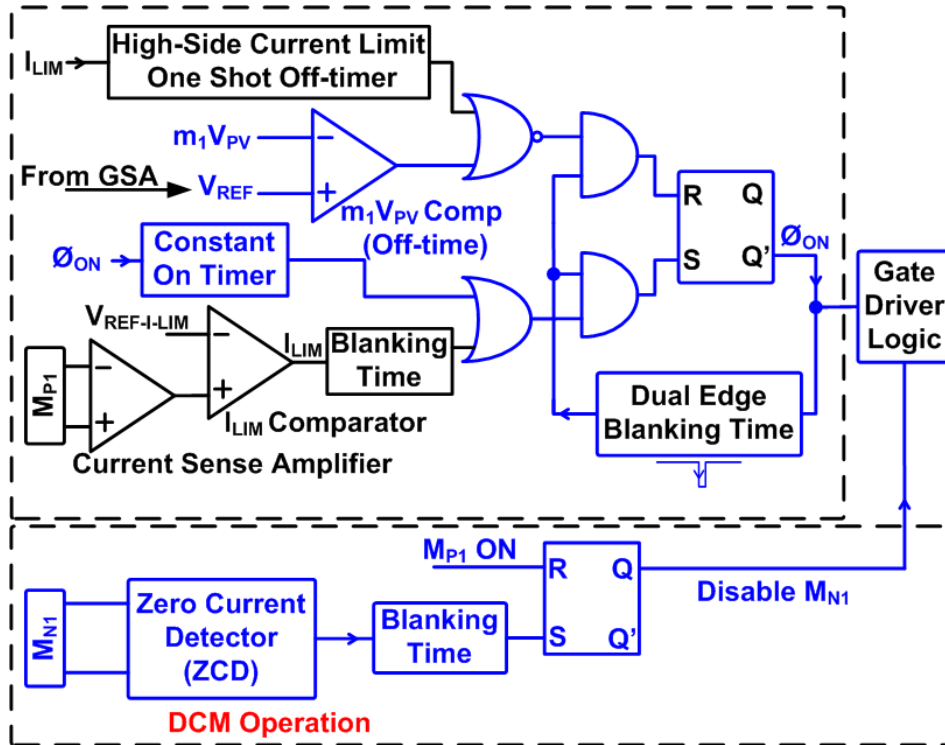


- EH operates in **CCM** with **constant on-time** of switch  $M_{P1}$ .
- $m_1V_{PV}$  is **compared** with  $V_{REF}$  to determine  $t_{OFF}$  of buck converter:

$$t_{OFF} = \left( \frac{V_{PV} \eta_P}{V_{BATT}} - 1 \right) T_{ON} \approx \text{constant.}$$

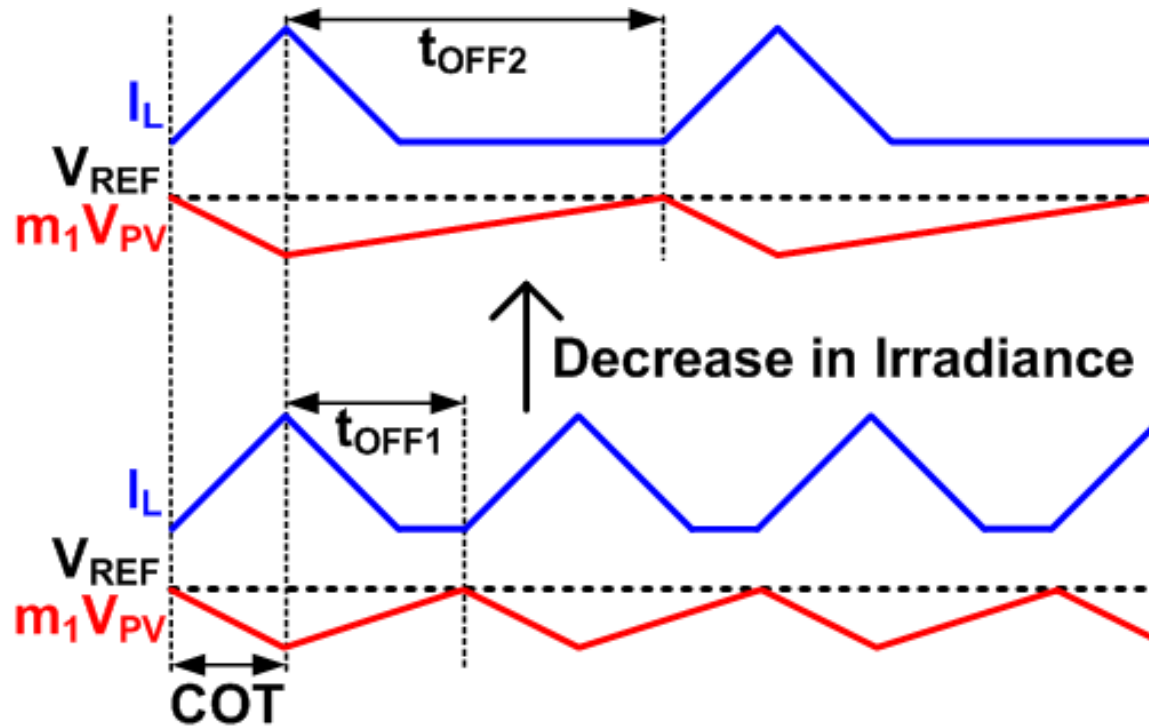


# IAAFPC Operation: Low Irradiance



➤ **Constant on-time** and  $t_{OFF} = \left[ \frac{(V_{PV} - V_{BATT}) T_{ON}}{2 L I_{PV}} - 1 \right] T_{ON} \propto \frac{1}{I_{PV}}$

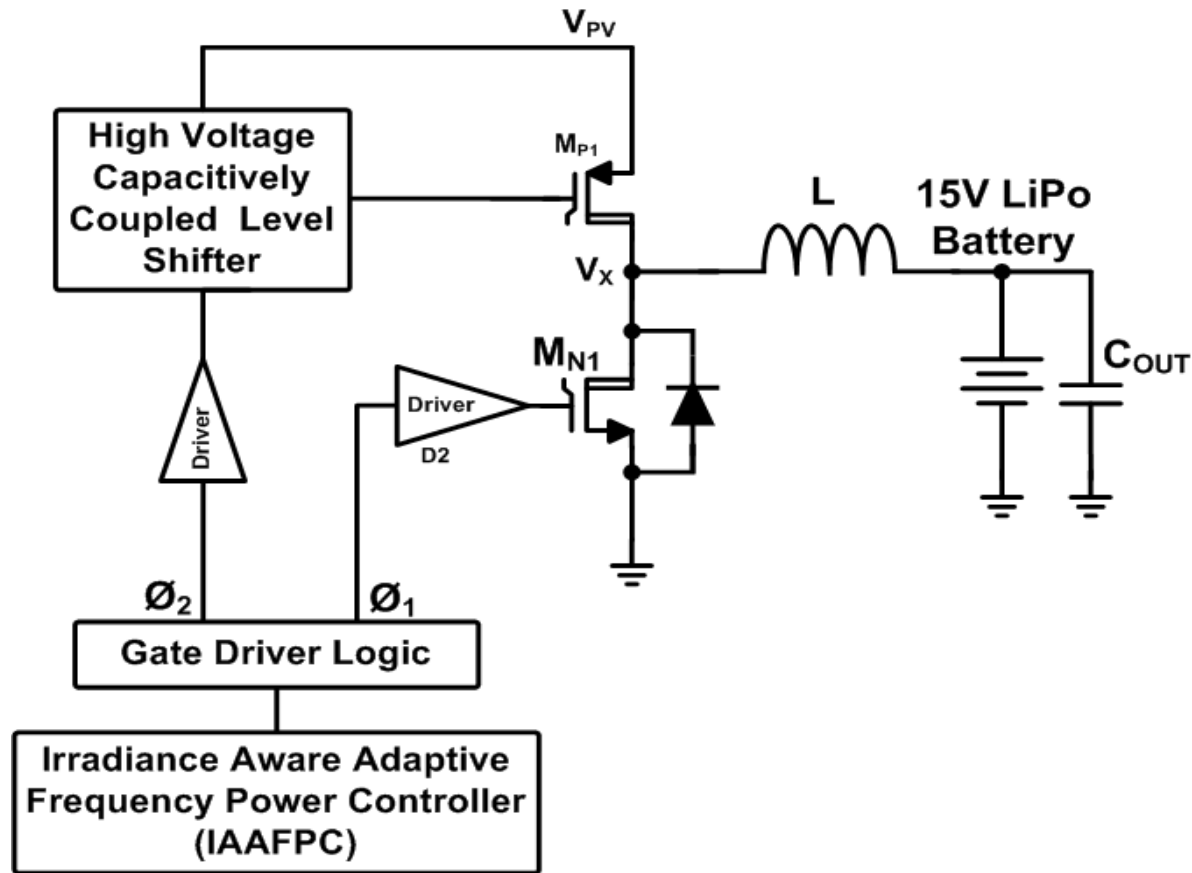
# Adaptive Frequency in DCM



$$f_{sw} = \frac{2 L I_{PV}}{(V_{PV} - V_{BATT}) T_{ON}} \propto I_{PV}$$

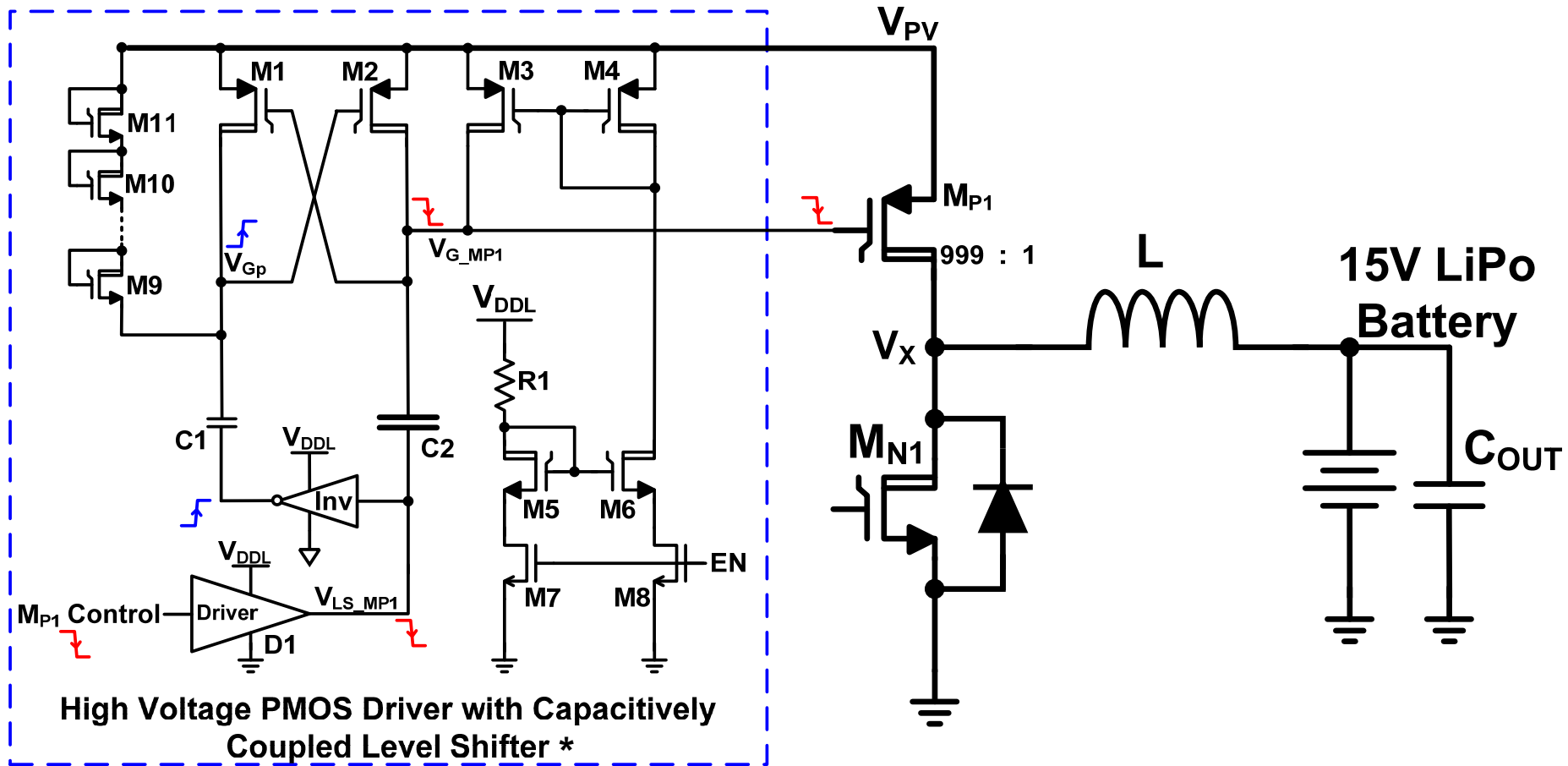
- **Reduced  $f_{sw}$**  helps to maintain **high power efficiency** even when Solar Panel output power is much lower.

# High Voltage Gate Driver and Level Shifter



- $V_{GS}$  for  $M_{P1}$  has to be **<5V** to prevent device **breakdown**.
- Gate-drive **logic** for  $M_{P1}$  is **shifted up** to a high DC voltage.
- Level-shifter requires **low-static current** and **low transition time**.

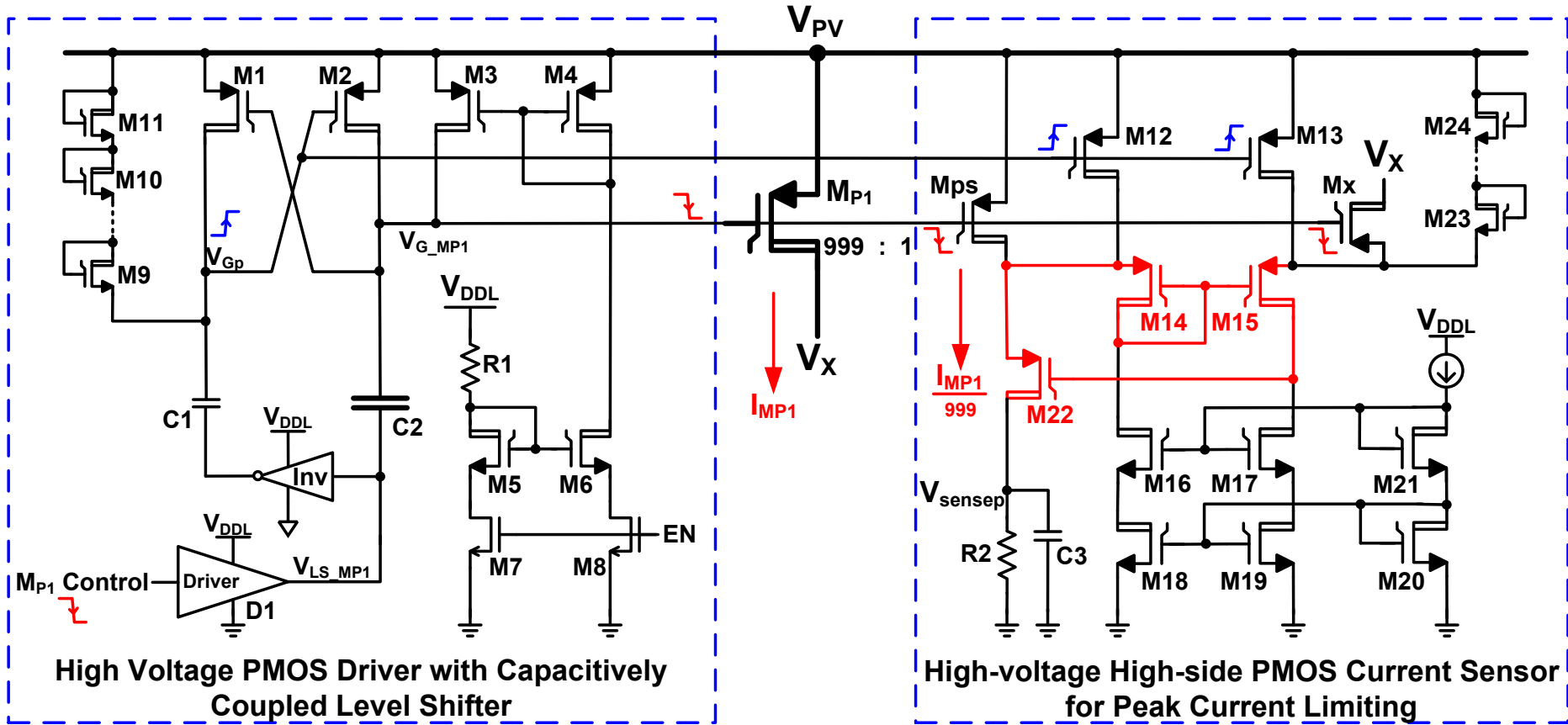
# High Voltage Capacitively Coupled Level Shifter



➤ **HVCCLS exhibits zero static current and sub-ns level-shifting.**

\* Zhidong Liu and Hoi Lee, "A 100V gate driver with sub-nanosecond-delay capacitive-coupled level shifting and dynamic timing control for ZVS-based synchronous power converters," *Proc. IEEE Custom Integrated Circuits Conf.*, San Jose, CA, USA, Sept. 2013.

# HV Gate Driver and Current Sensor



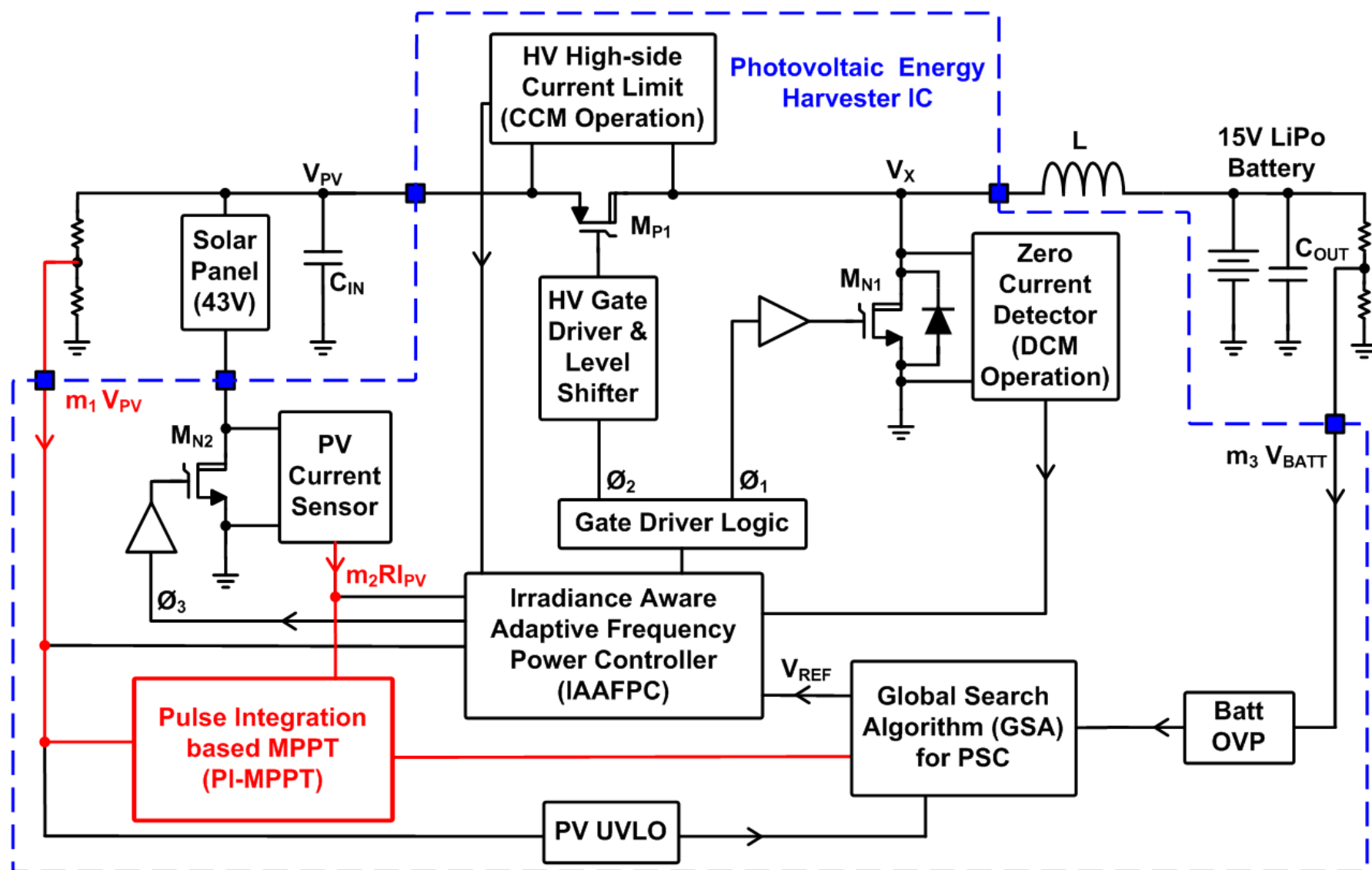
- **HVCCLS** also provides switching signals to operate high-voltage **current-sensor** for **peak-current-limiting** of  $M_{P1}$ .

# Outline

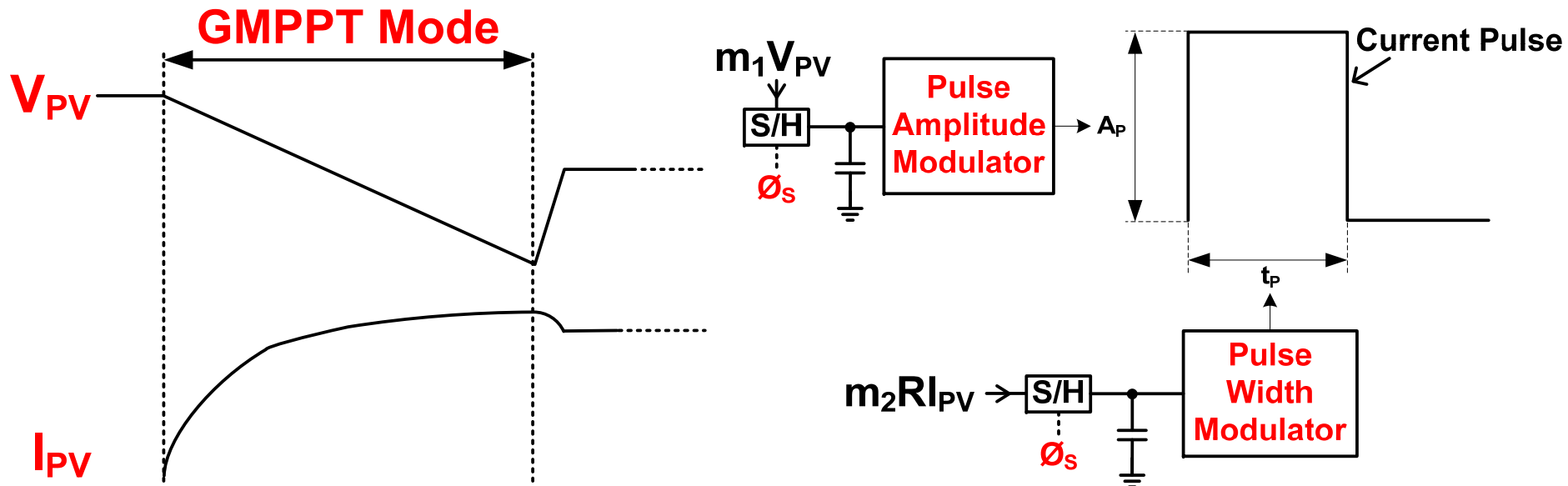
---

- Background and Motivation
- Proposed Energy Harvester Architecture and Algorithm
- Irradiance Aware Adaptive Frequency Power Controller (IAAFPC) and Gate Driver
- **Pulse-Integration Based Maximum Power Point Tracker (PI-MPPT)**
- Measurement Results
- Conclusion

# Pulse Integration based MPPT (PI-MPPT)



# Pulse Integration based MPPT (PI-MPPT)



- 500 kS/s MPPT clock
- 135 instantaneous power samples computed in a  $270\mu\text{s}$  GMPPT time

$$A_P \propto m_1 V_{PV} = c_1 m_1 V_{PV}$$

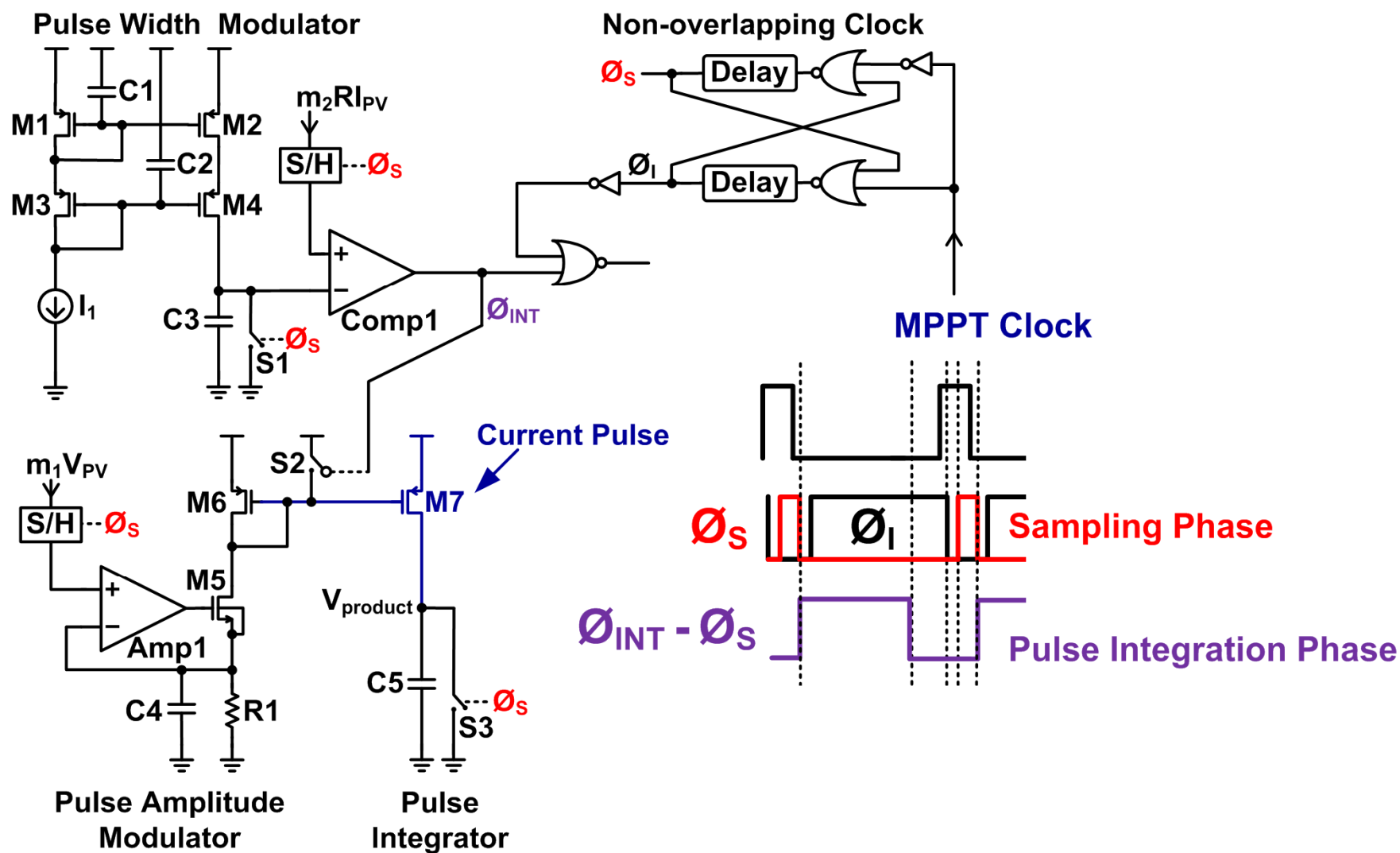
$$t_P \propto m_2 R I_{PV} = c_2 m_2 R I_{PV}$$

$$\text{Integrated area under the pulse} = \int_0^{t_P} A_P \cdot t \, dt = A_P \times t_P$$

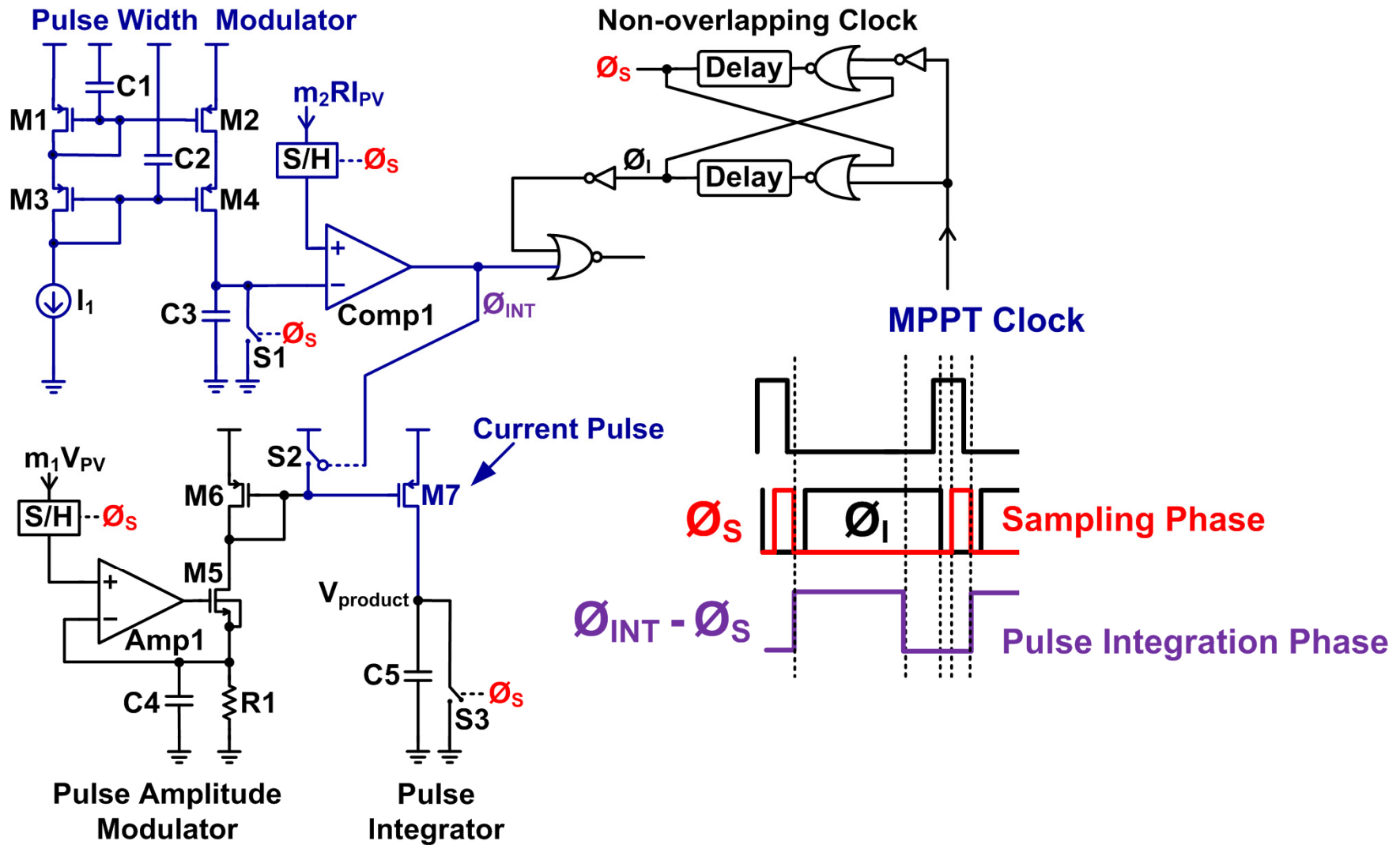
$$= (c_1 c_2 m_1 m_2) V_{PV} I_{PV}$$



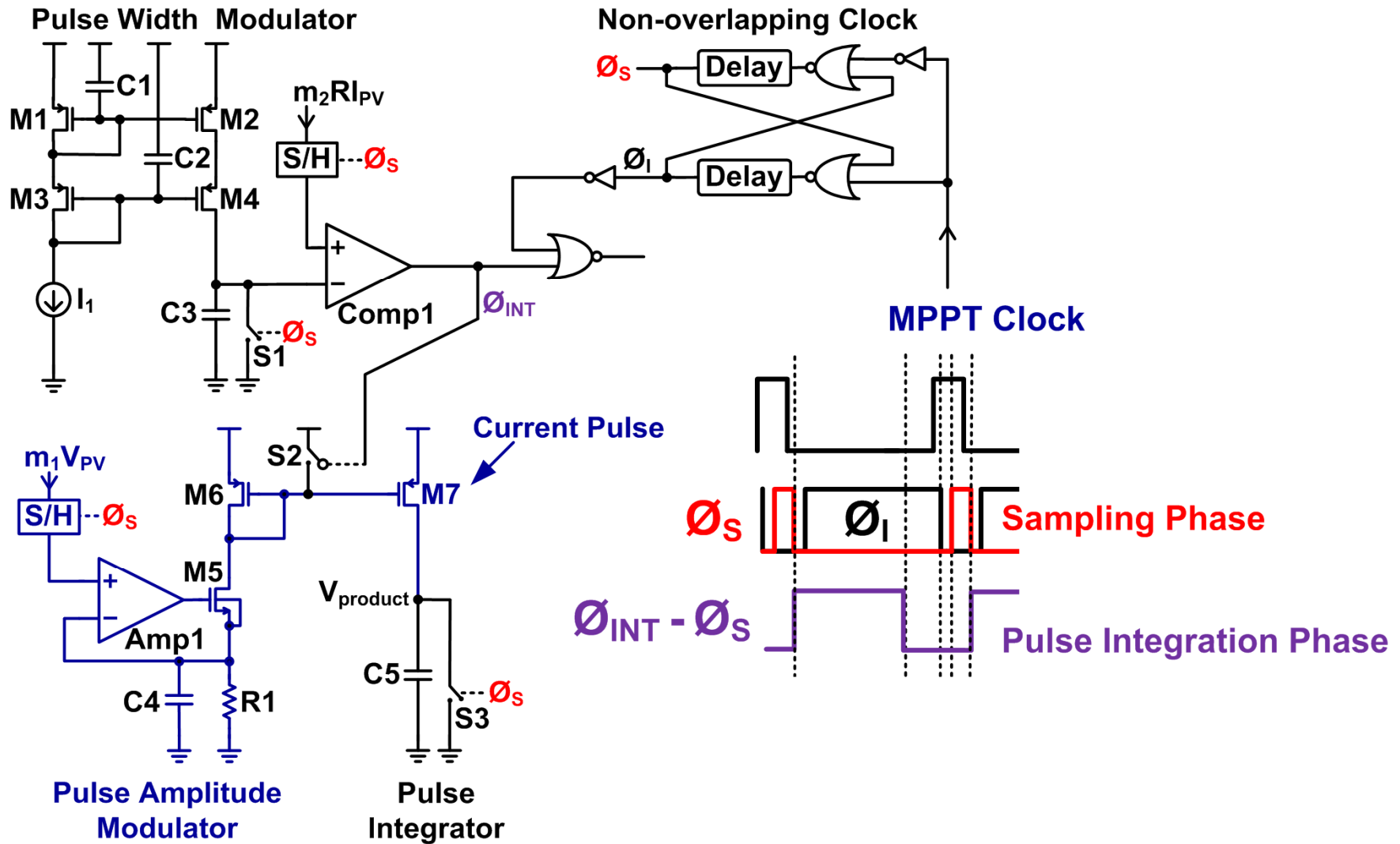
# Pulse Integration based MPPT (PI-MPPT)



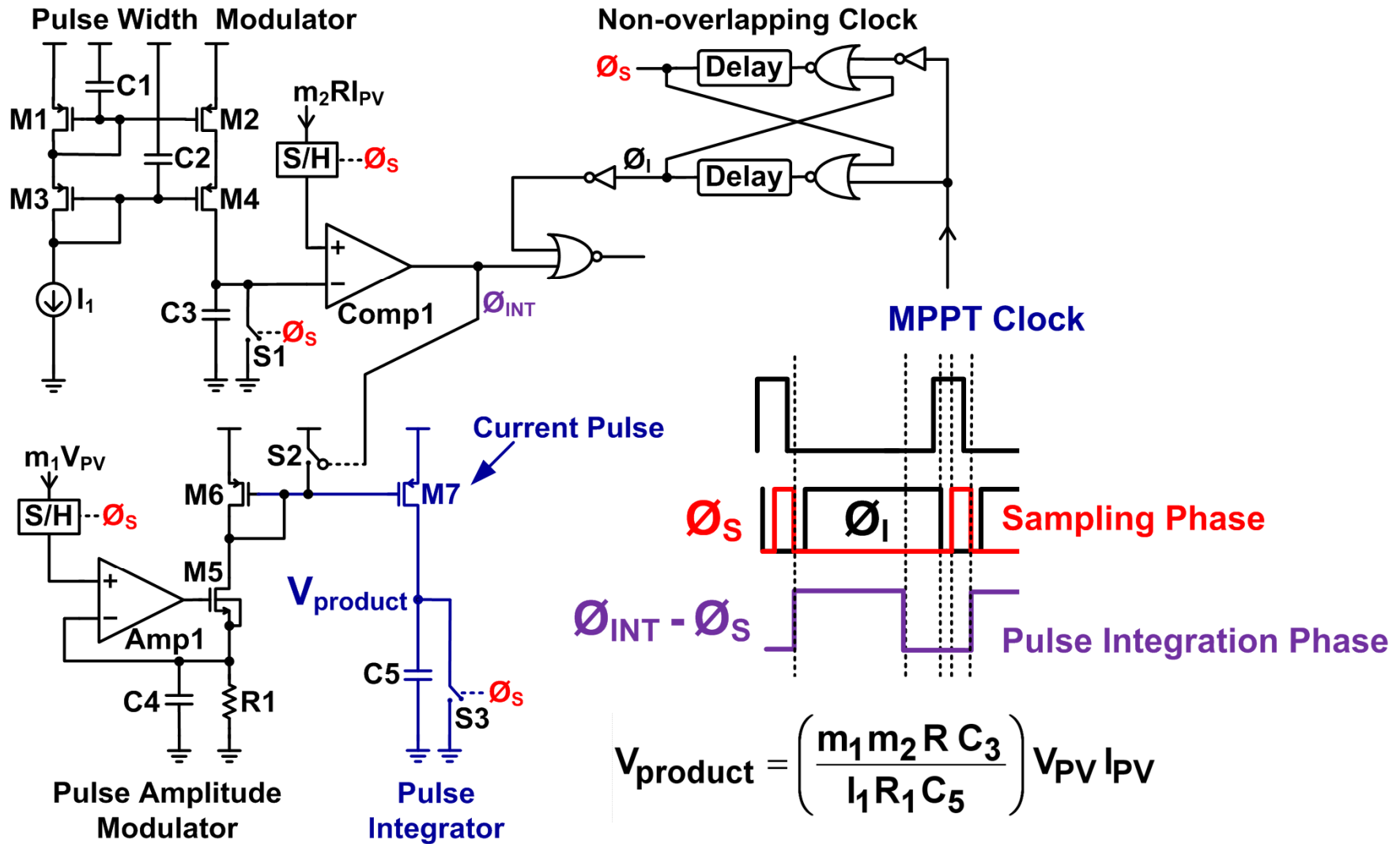
# Pulse Integration based MPPT (PI-MPPT)



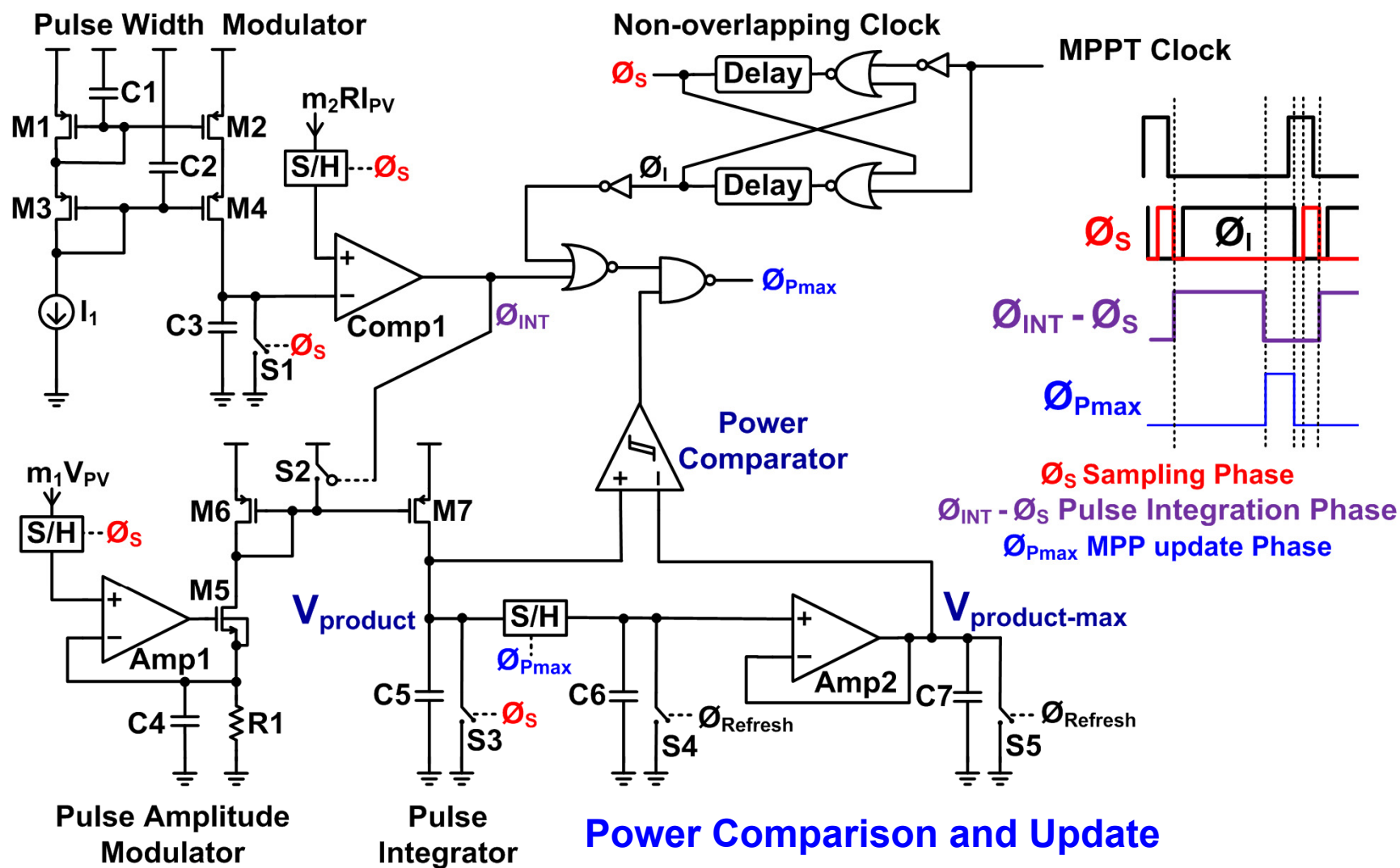
# Pulse Integration based MPPT (PI-MPPT)



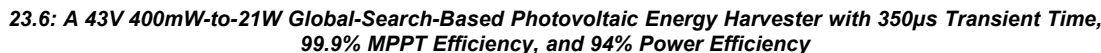
# Pulse Integration based MPPT (PI-MPPT)



# Pulse Integration based MPPT (PI-MPPT)



© 2014 IEEE  
International Solid-State Circuits Conference



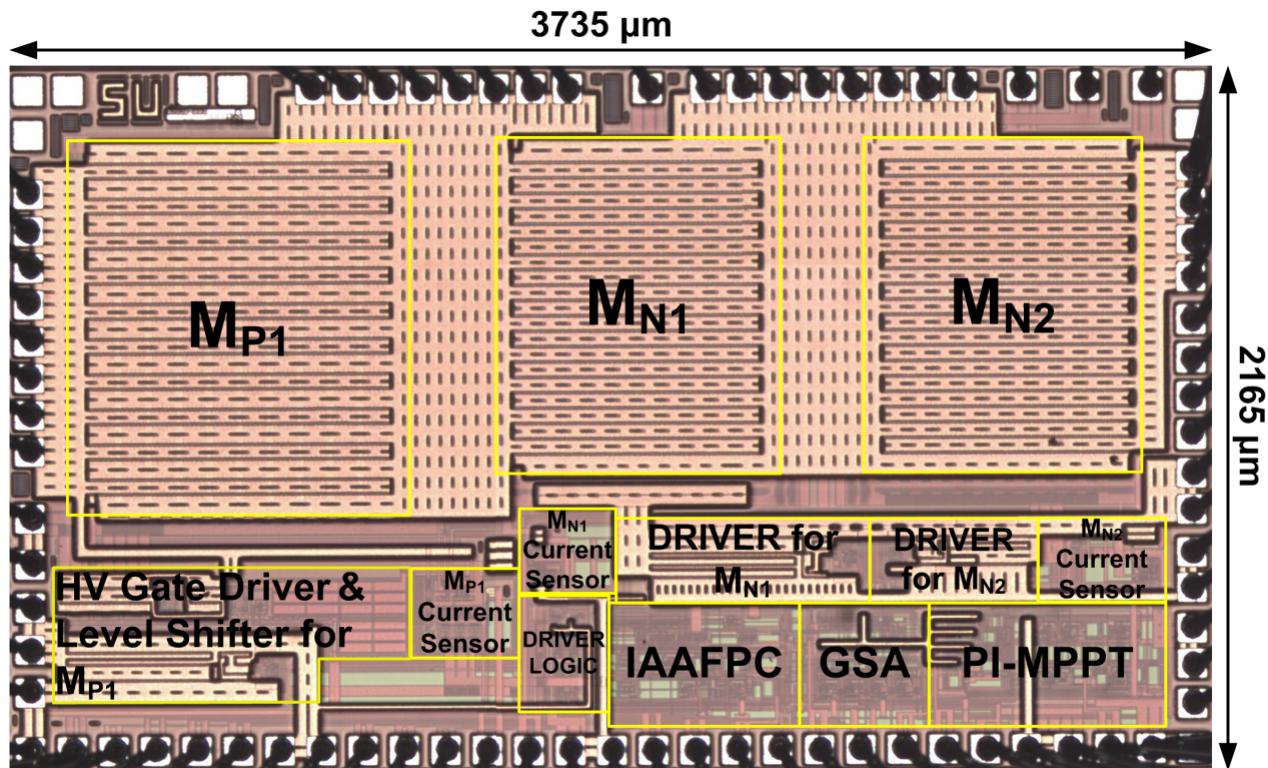
# Outline

---

- Background and Motivation
- Proposed Energy Harvester Architecture and Algorithm
- Irradiance Aware Adaptive Frequency Power Controller (IAAFPC) and Gate Driver
- Pulse-Integration Based Maximum Power Point Tracker (PI-MPPT)
- **Measurement Results**
- Conclusion



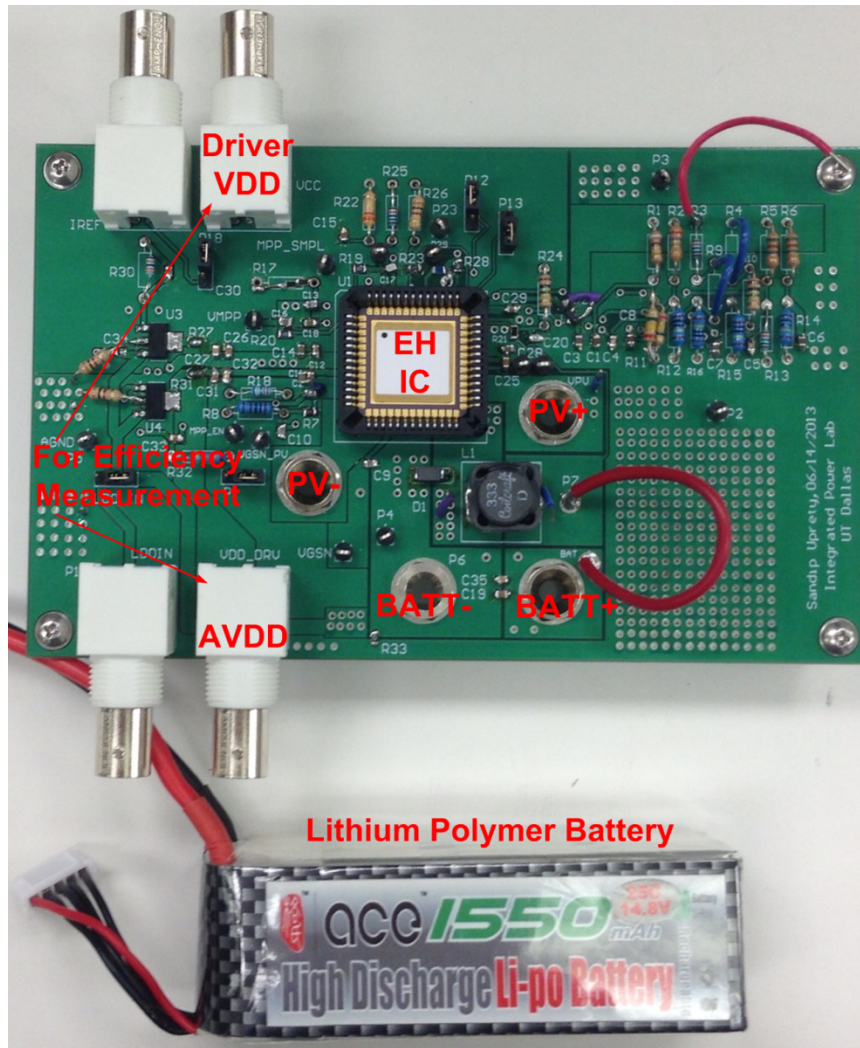
# Chip Micrograph



- Implemented in **0.35μm 50V CMOS** with a total chip area of **8.1mm<sup>2</sup>**
  - **Power Transistors:**  $M_{P1}$ ,  $M_{N1}$  and  $M_{N2}$
  - Irradiance Aware Adaptive Frequency Power Controller (**IAAFPC**)
  - Global Search Algorithm (**GSA**)
  - Pulse-Integration based MPPT (**PI-MPPT**)



# Measurement Setup

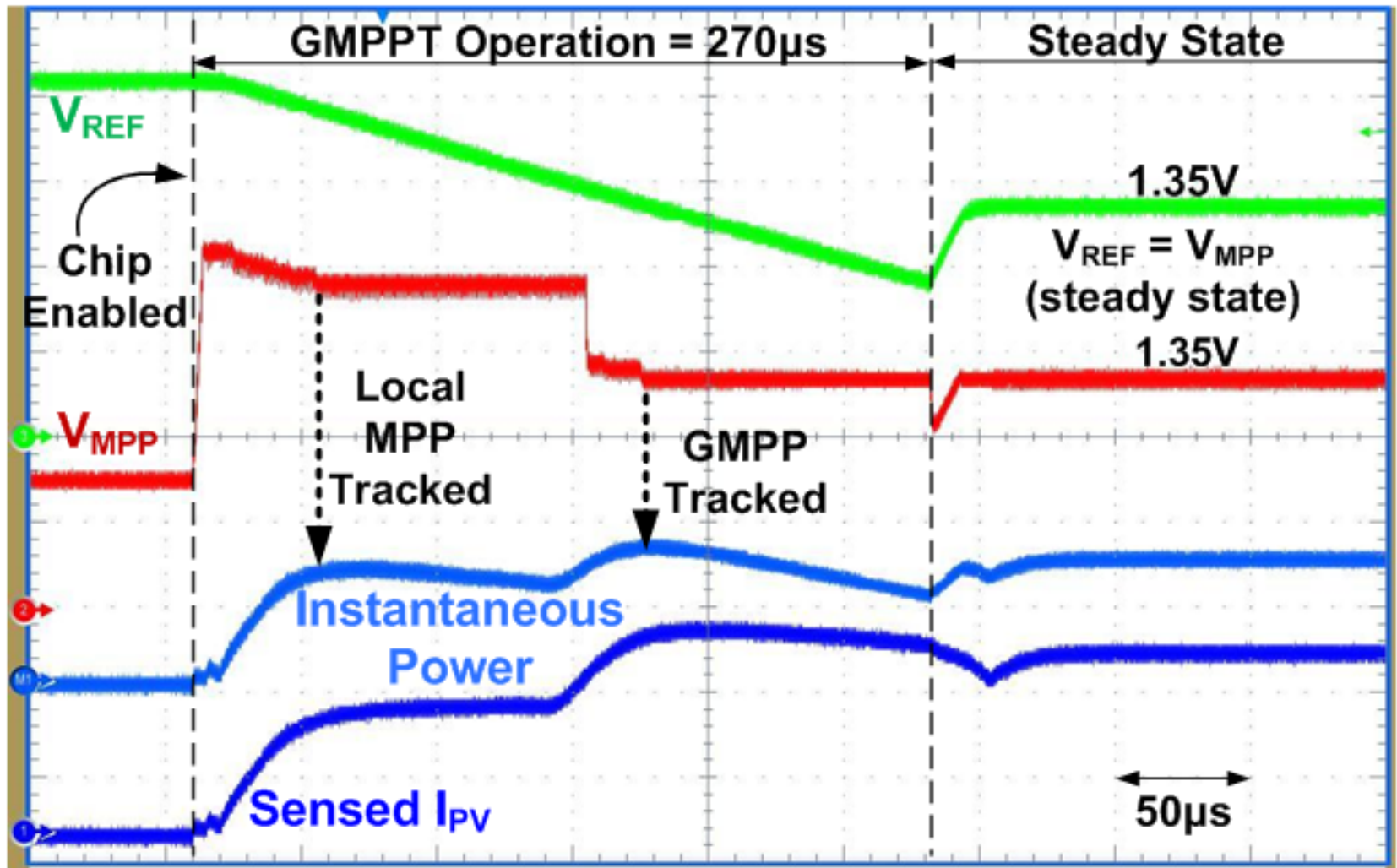


**Test PCB**



**Outdoor Measurement Setup for PSC**

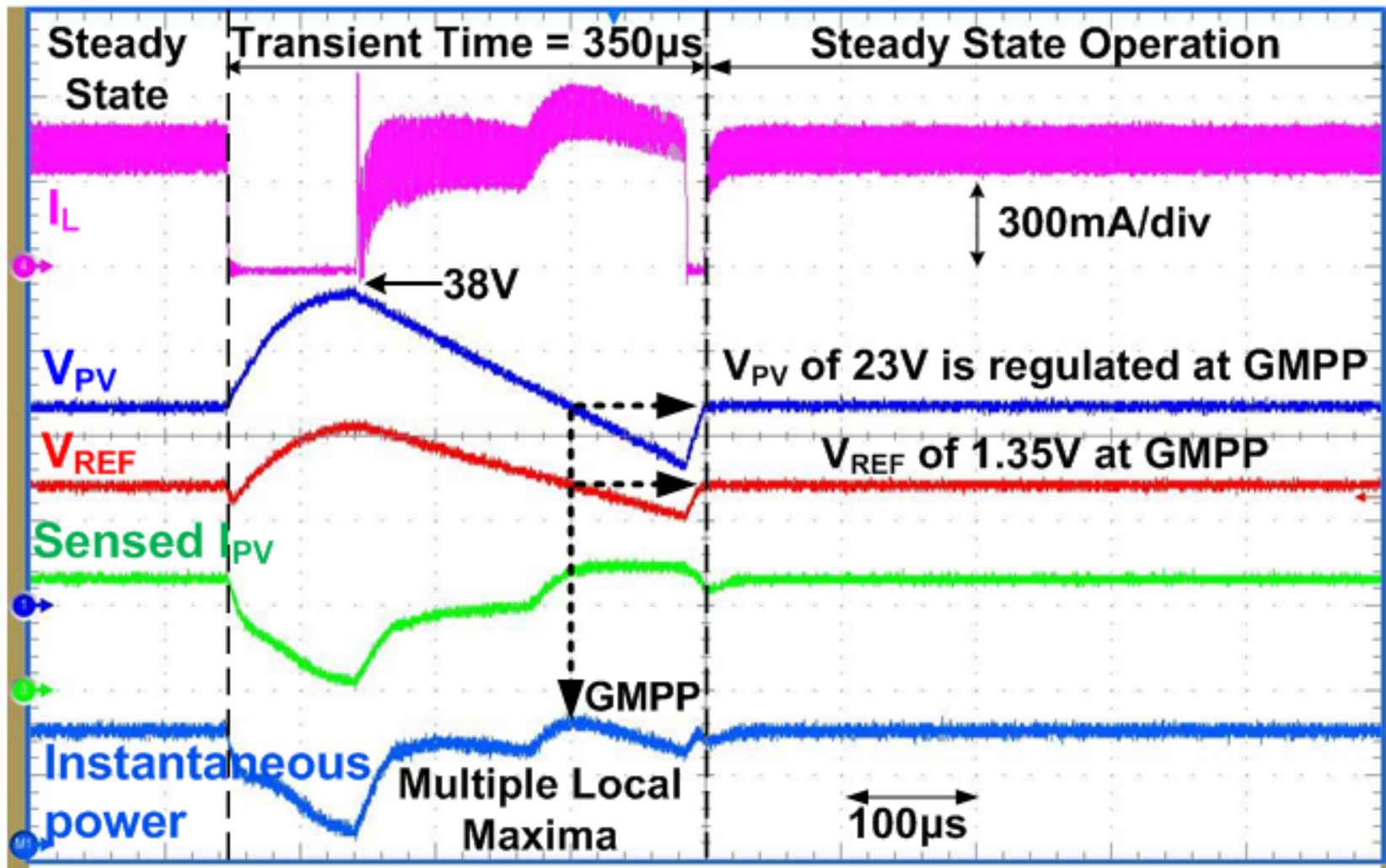
# Startup during Partial Shading Condition



➤ EH tracks **Global Maximum** voltage  $V_{MPP}$  in **270 $\mu$ s** and sets  $V_{REF} = V_{MPP}$ .

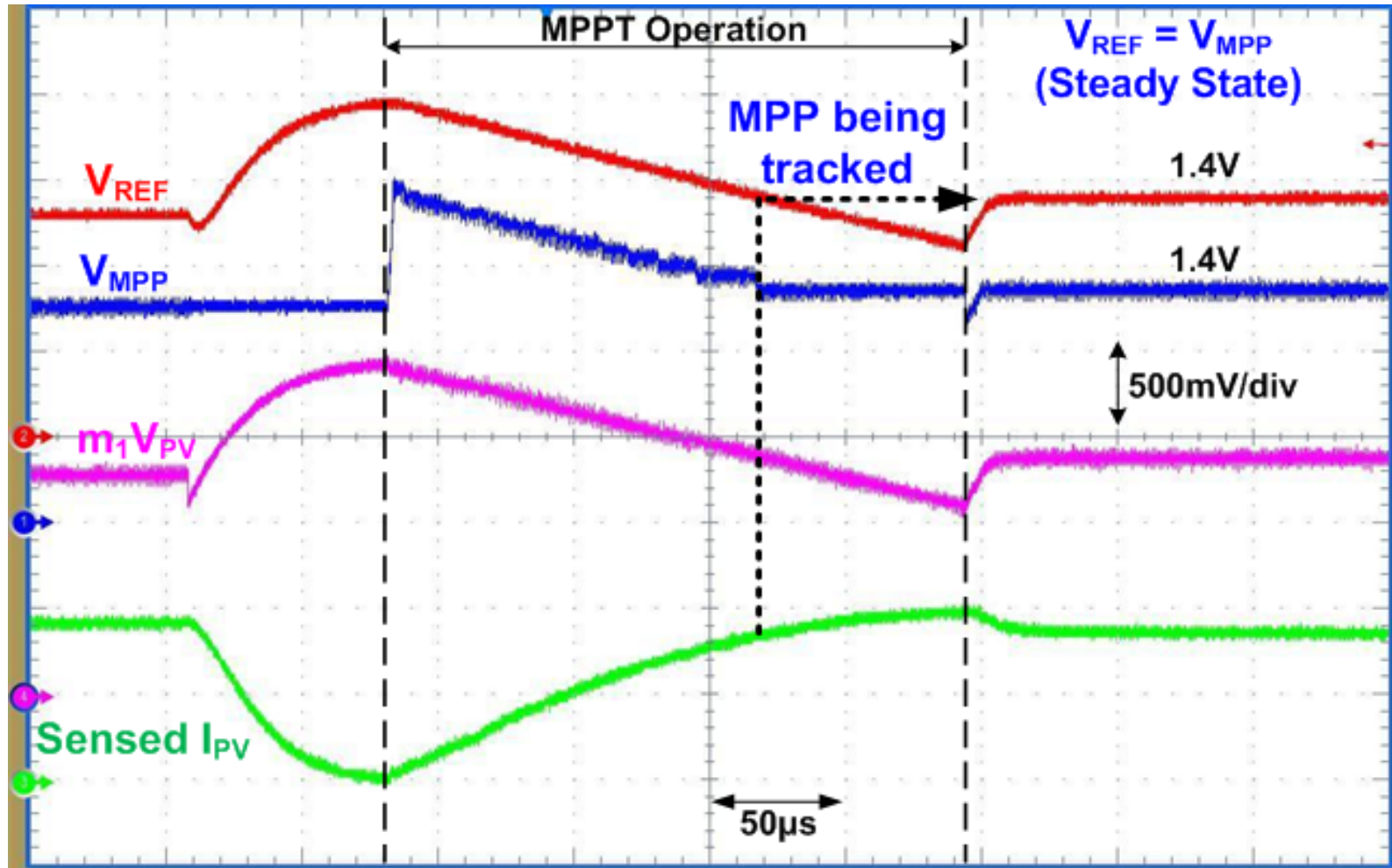


# Normal Operation during PSC



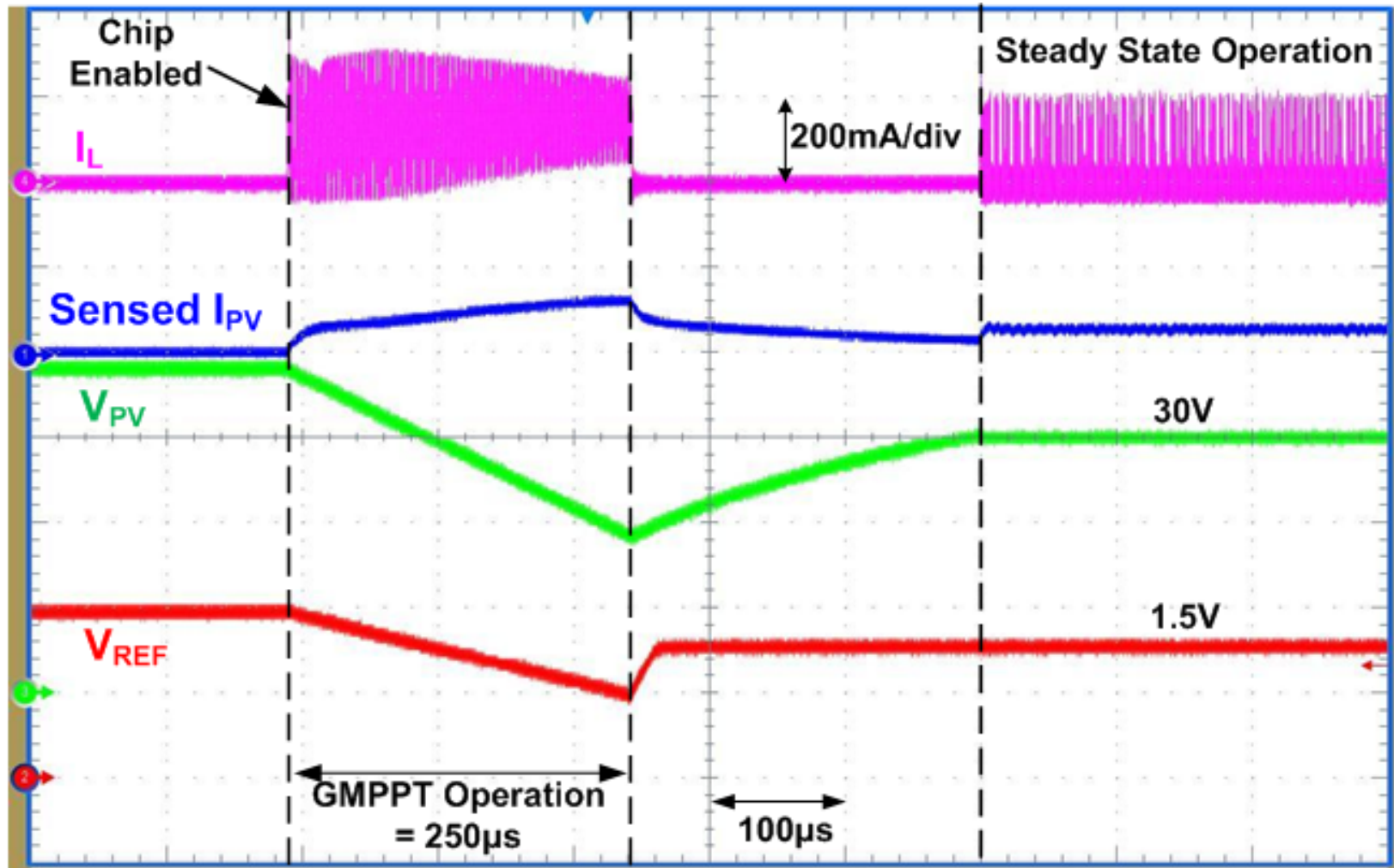
➤ **Total transient time (GMPPT + settling) of  $350\mu\text{s}$  with  $V_{PV} = 23\text{V}$ .**

# High Input Power Un-shaded Condition



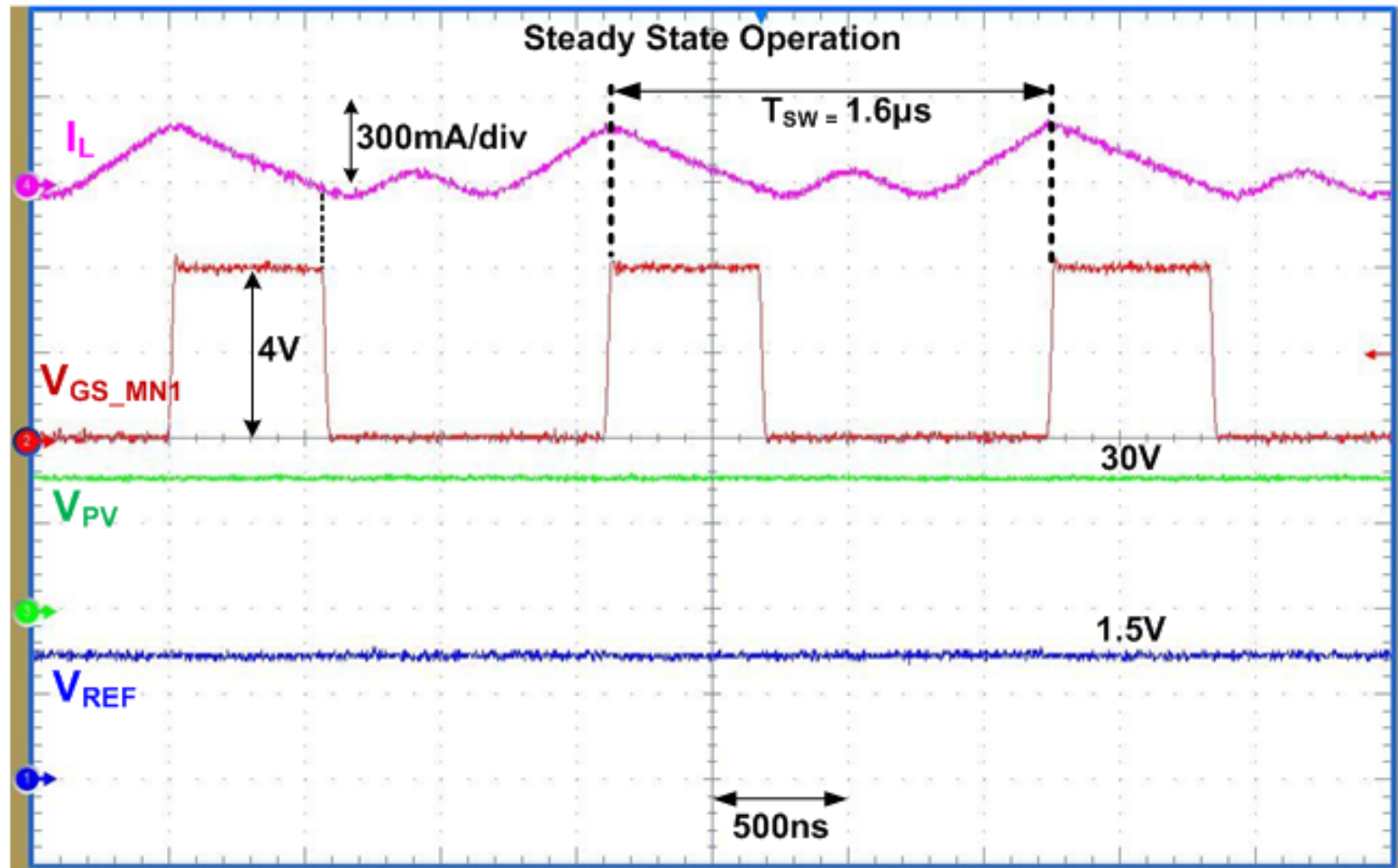
➤ **PI-MPPT** tracks single local maximum voltage  $V_{MPP}$ .

# Low Input Power Un-shaded Condition



➤ Proposed EH in **DCM** achieves **510µs** total transient time.

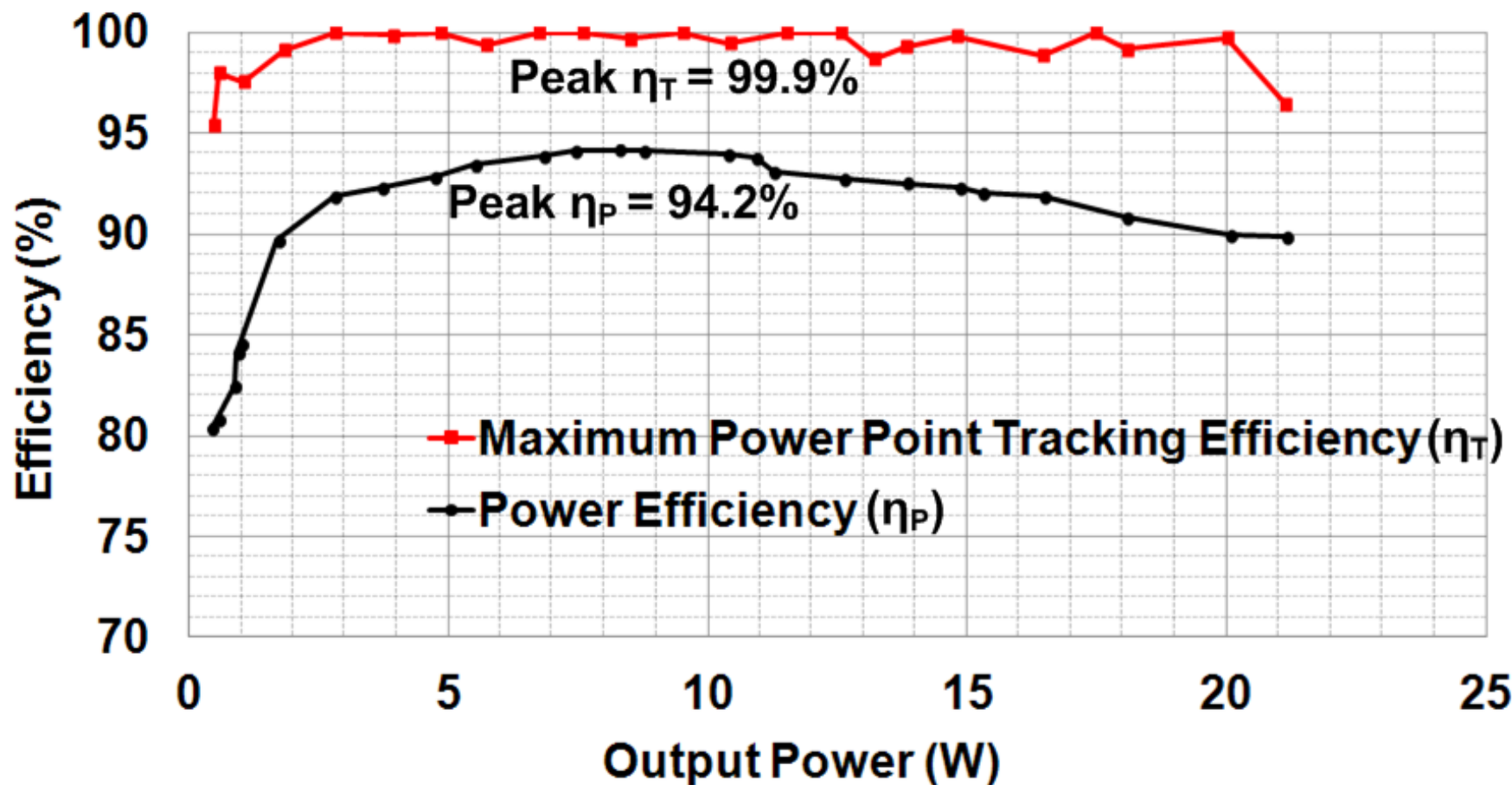
# Low Input Power Un-shaded Condition



- Proposed EH operates with reduced  $f_{sw}$  of **625kHz** in **DCM** with zero current detector.



# Power and MPPT Efficiency Measurements



- $V_{OUT}$  is a 15V Li-Po battery.
- $V_{IN}$  is 40V with ( $I_{SC}$ ,  $R_S$ ) ranging from (20mA, 500 $\Omega$ ) to (800mA, 12 $\Omega$ ).

# Comparisons with State-of-the-Art Designs

	[5] ISSCC 13	[4] LT3652	[3] ISSCC 12	[2] ISSCC 13	This work
Process	TSMC 0.35 $\mu$ m	N.A.	0.35 $\mu$ m HV CMOS	0.5 $\mu$ m CMOS	0.35 $\mu$ m HV CMOS
Harvester Power Throughput (W)	~0.04 – 0.5	7 – 28.8	36 (off-chip power stage)	0.55 – 2.6	0.4 – 21.1
$V_{IN}$ (V)	0.5 – 2	5 – 32	3.4 – 5.5	4	7 – 43
Peak Power Efficiency ( $\eta_P$ )	89% ( $f_{SW} = 500$ kHz)	88% ( $f_{SW} = 1$ MHz)	N.A.	94% ( $f_{SW} = 100$ kHz)	94.2% ( $f_{SW} = 1$ MHz)
$P_{OUT}$ Range (W) for $\eta_P > 85\%$	~0.12 – 0.34	N.A.	N.A.	0.55 – 2.2	0.988 – 21.1
Power Density (mW/mm <sup>2</sup> ) @ Peak $\eta_P$	~158	N.A.	N.A.	168	1022
Peak Tracking Efficiency (w/o PSC)	N.A.	N.A. (fixed $V_{REF}$ )	> 99%	99.9%	99.9%
$P_{OUT}$ Range (W) for Tracking Efficiency ( $\eta_T$ ) > 95%	N.A.	N.A.	N.A. (~2 – 37.7 $P_{IN}$ )	0.55 – 2.6	0.4 – 21.1
Global MPPT in PSC ( $\eta_T$ )	No	No	No	No	Yes (99%)
Transient Time (Total Time for MPPT and Settling to reach $P_{MAX}$ )	N.A.	N.A.	N.A.	~1.6ms (470 $\mu$ s for 50% $P_{MAX}$ settling in one local maxima)	350 $\mu$ s (under multiple local maxima)



# Conclusion

---

- A **43V 21W** Solar Energy Harvester with a **Global Search Algorithm** is presented.
- GSA implemented with **PI-MPPT** can track **GMPP** in presence of multiple local maxima. **99%** GMPPT efficiency and total transient time of **350 $\mu$ s** are reported.
- **IAAFPC** enables the EH to have **>80%** power efficiency across entire **400mW - 21W** power throughput. Peak power efficiency of **94%** is achieved at  $f_{sw}$  of **1 MHz**.
- **1022 mW/mm<sup>2</sup>** power density of this EH improves state-of-the-art EHs' performance by **6×**.

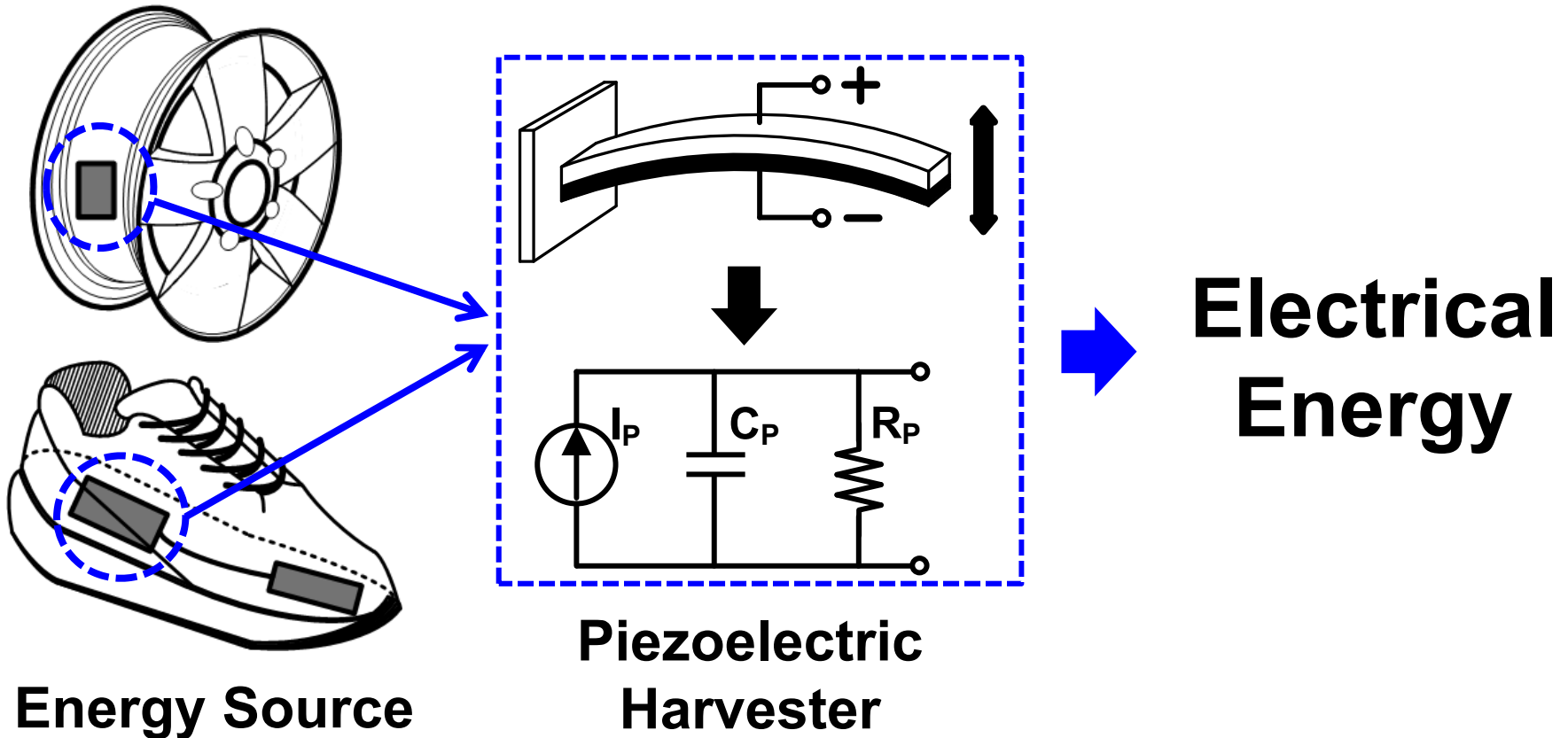
# Self-Powered 30 $\mu$ W to 10mW Piezoelectric Energy Harvesting System with 9.09ms/V Maximum Power Point Tracking Time

Minseob Shim, Jungmoon Kim, Junwon Jung,  
and Chulwoo Kim

*Korea University, Korea*



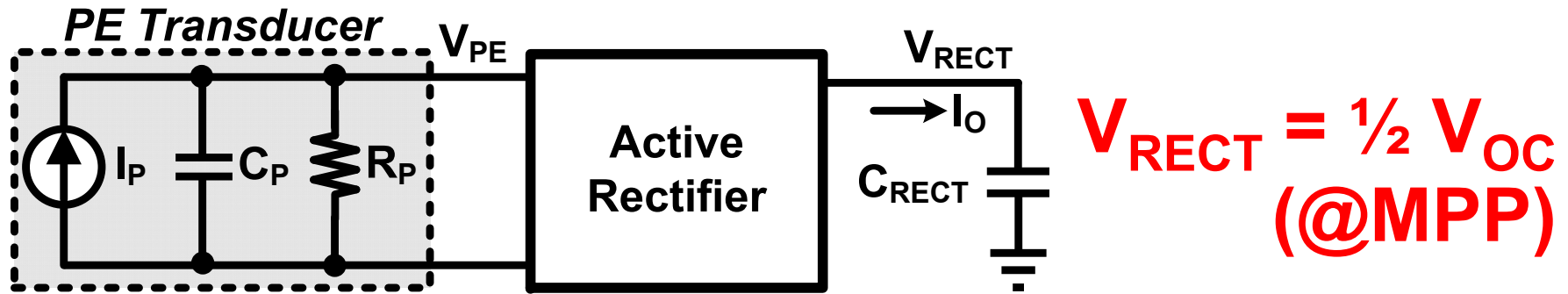
# Introduction



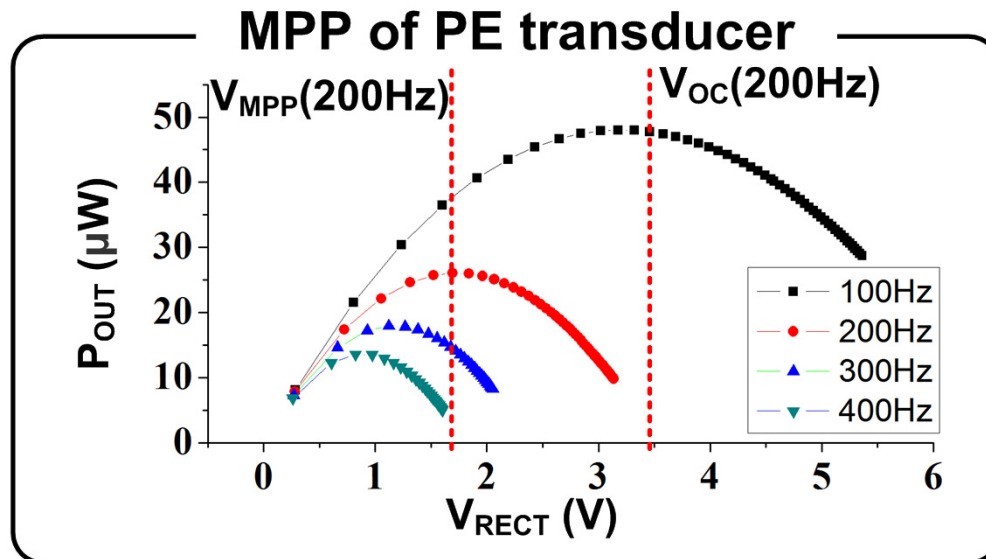
- Generate electrical power from kinetic energy
- Improve battery lifetime or batteryless

# Motivation (1)

- Maximum power point (MPP)



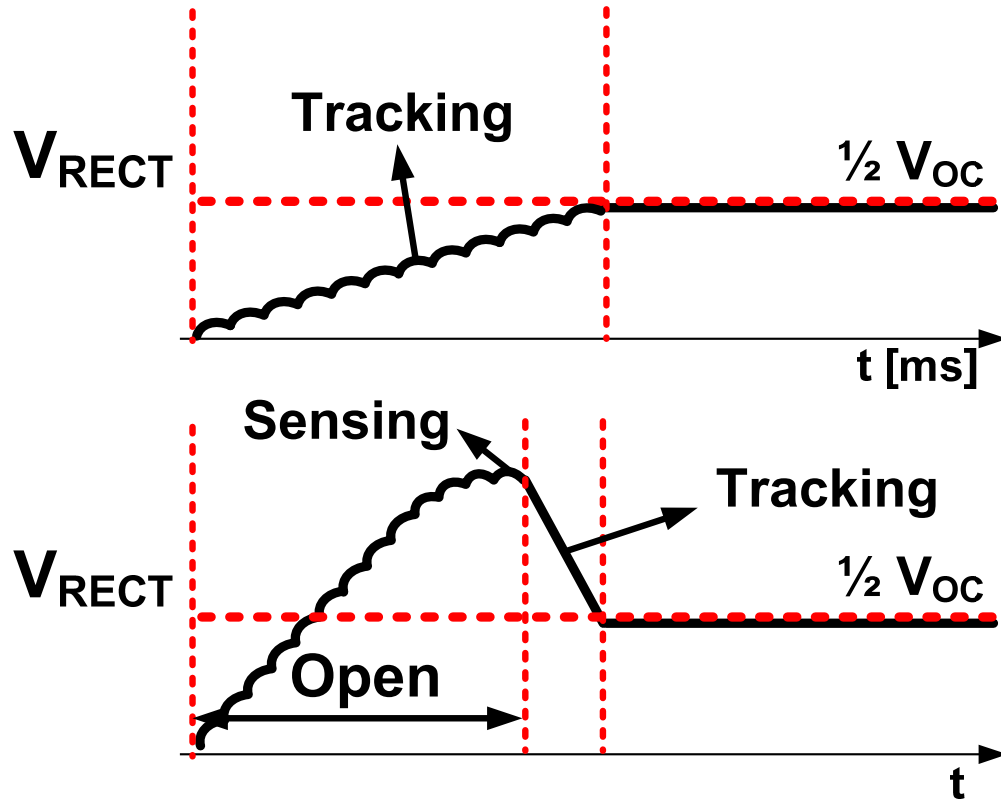
- The MPP is sensitive to changes of the environment



- Frequency
- Amplitude

# Motivation (2)

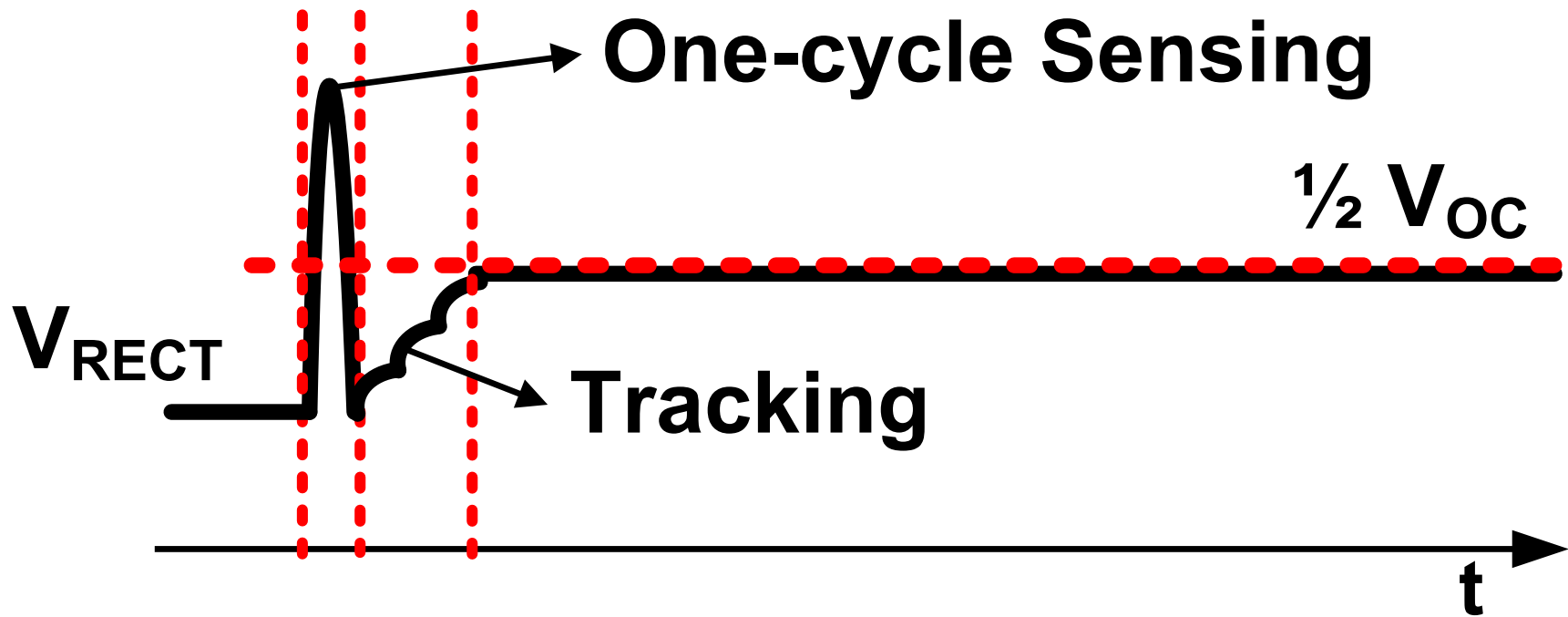
- Conventional MPP tracking (MPPT) methods



- Perturb & Observe (Hill-climbing)
  - Sensing  $V$  &  $I$
- Fractional  $V_{OC}$ 
  - Sensing  $V$

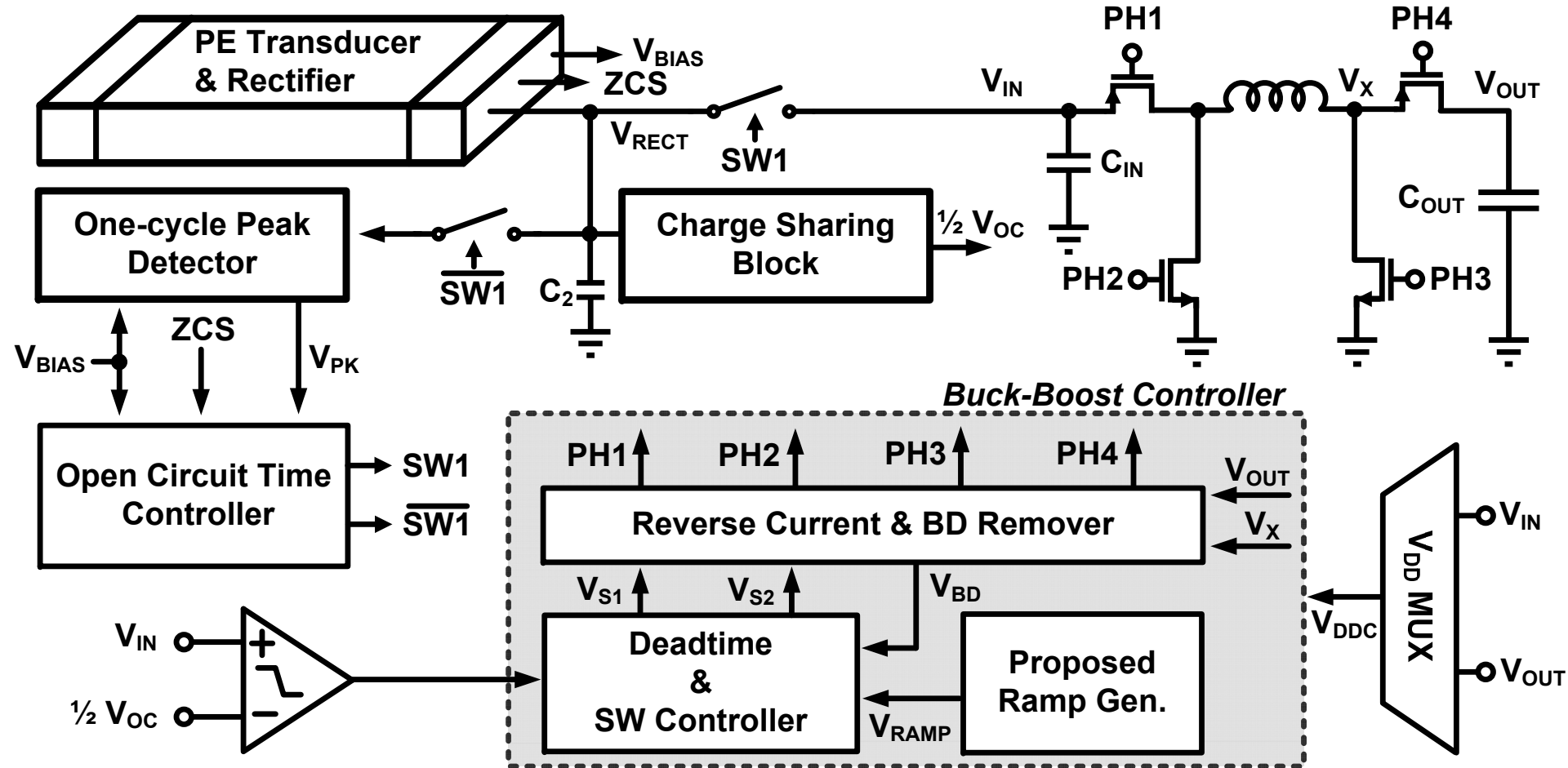
- Tens to hundreds of cycles for tracking

# One-cycle MPP Sensing

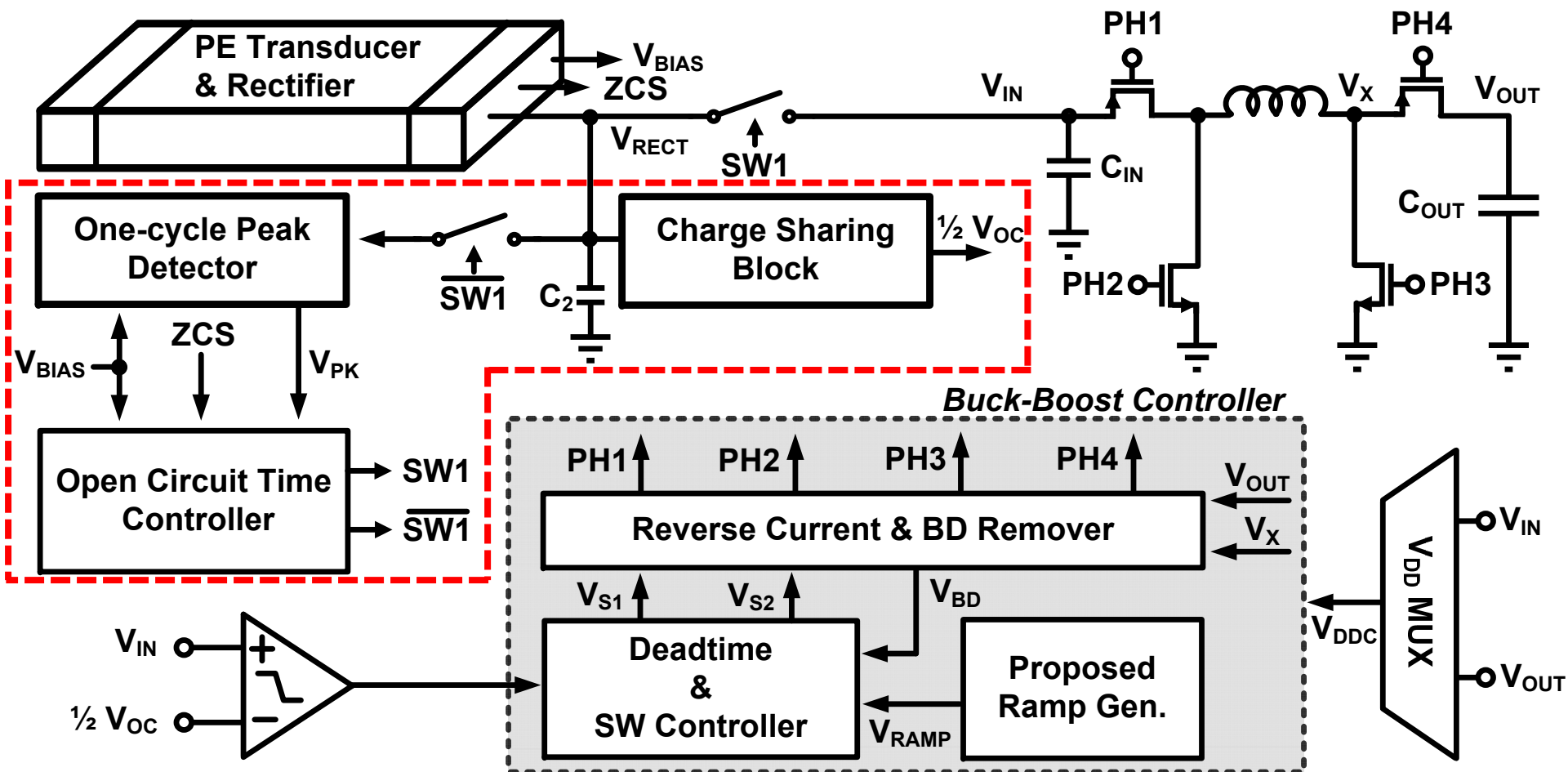


- Use small size sensing capacitor
- Short MPPT time
- Extracts more power from transducer

# Top Block Diagram



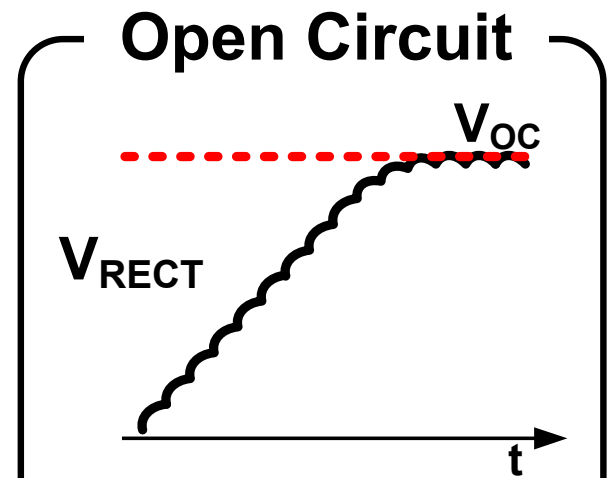
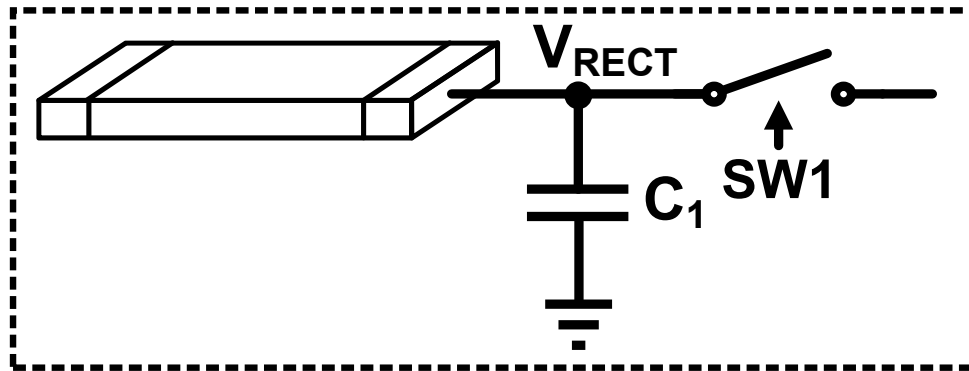
# One-cycle Sensing Blocks



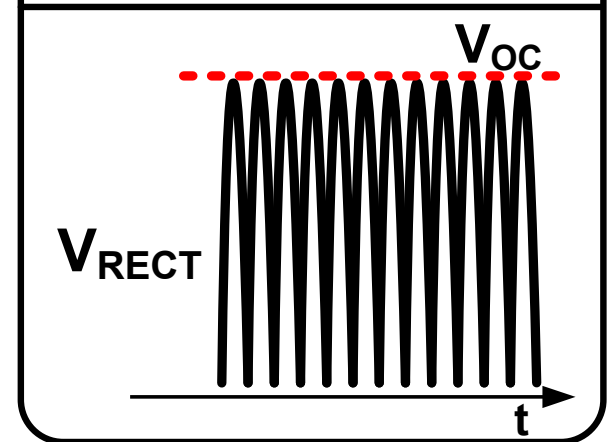
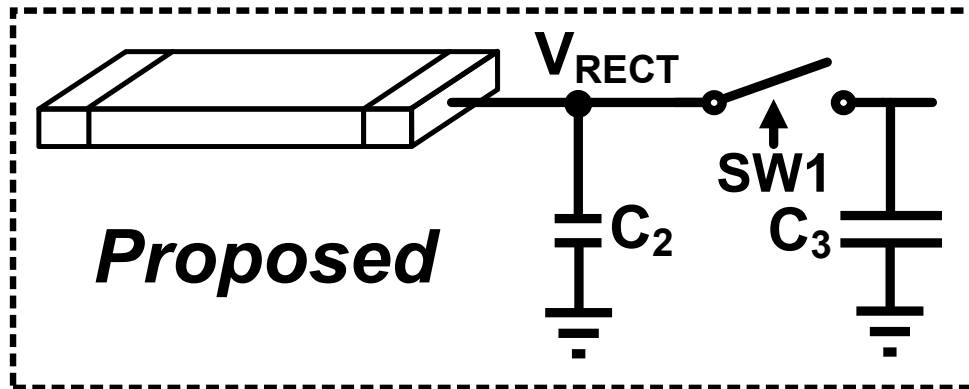


# Sensing Cap. Size Selection

*Large Sensing Cap.*

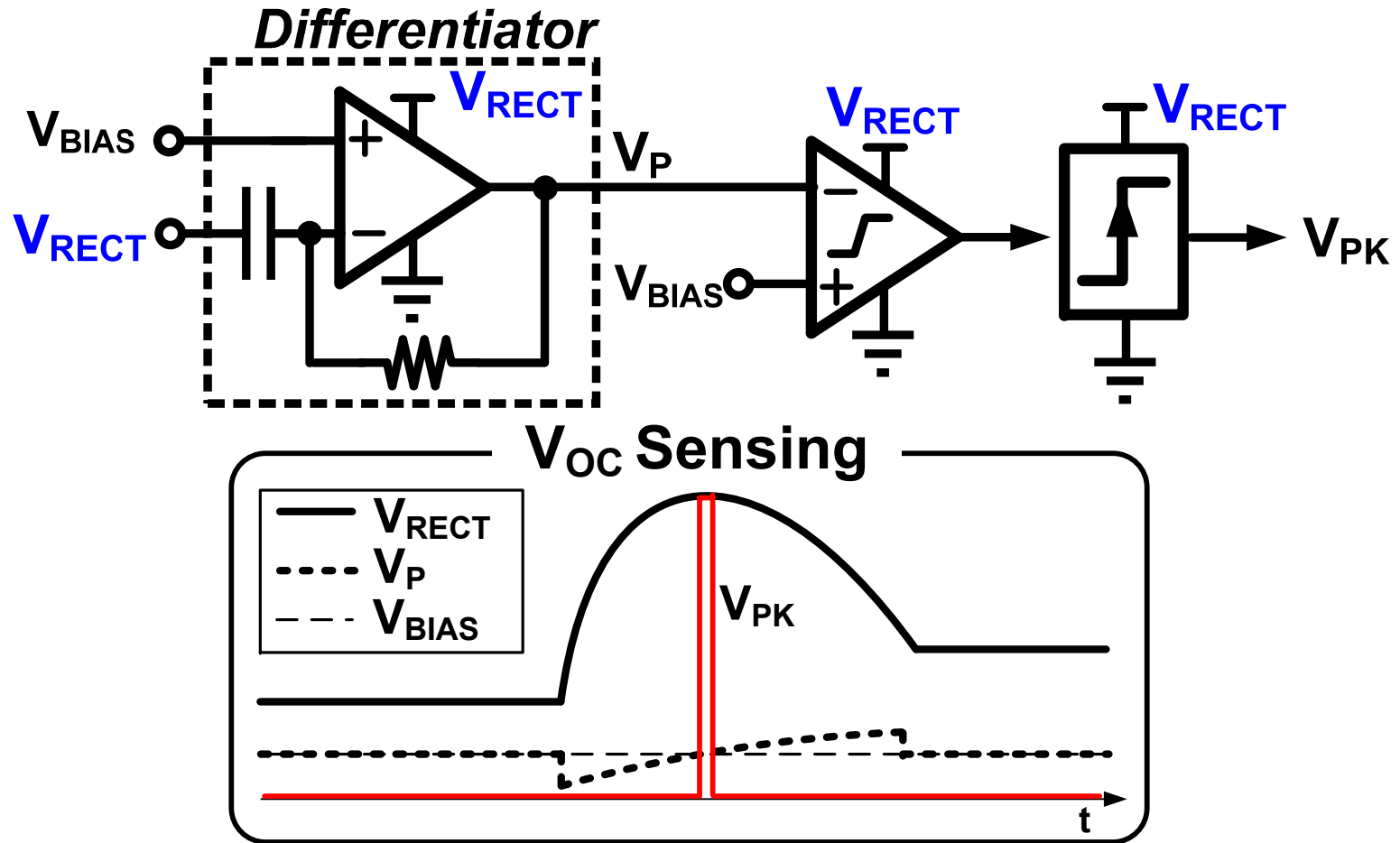


*Small Sensing Cap.*



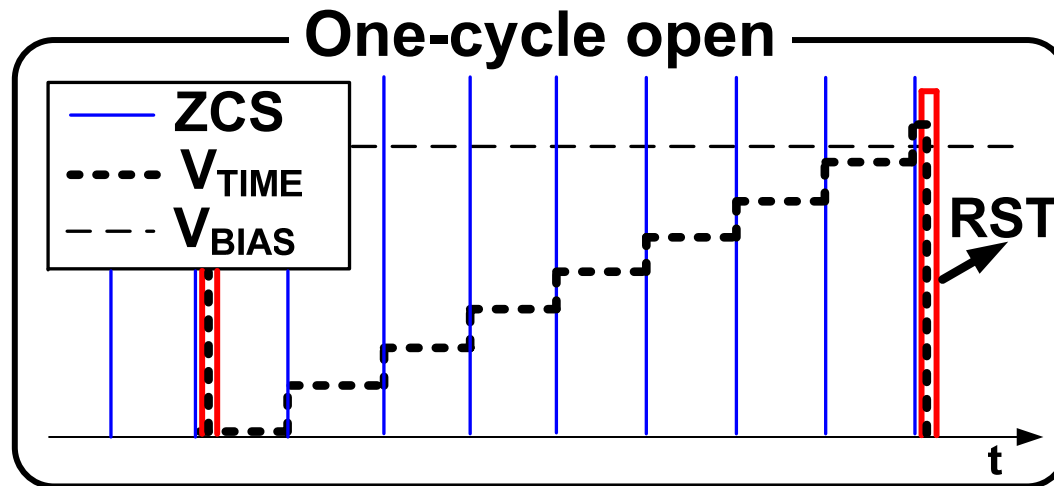
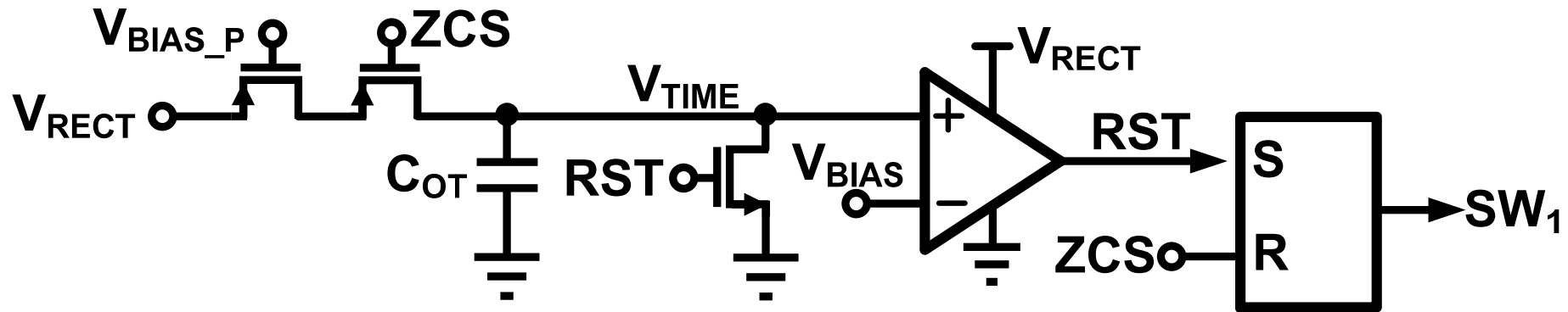
- Large cap ( $C_1$ ) : small ripple & long tracking time
- Small cap ( $C_2$ ) : large ripple & short tracking time

# One-cycle Peak Detector



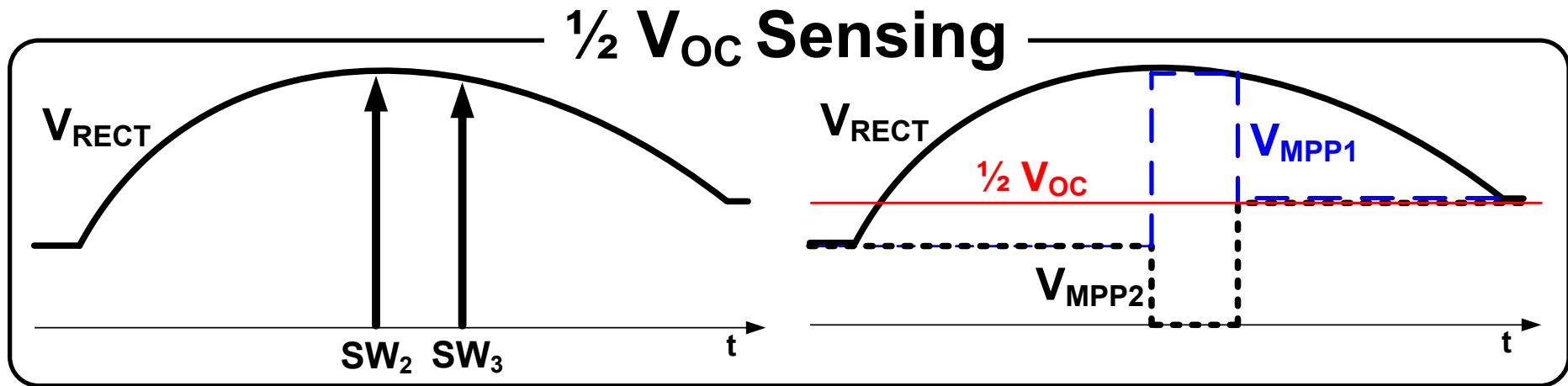
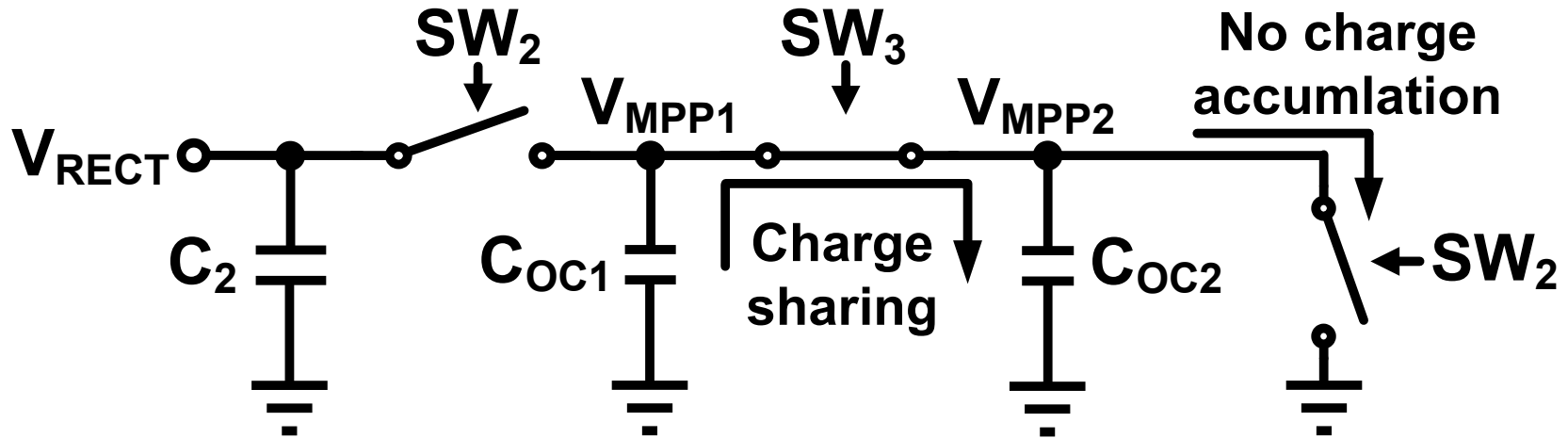
- $V_{RECT}$  : input and supply voltages of peak detector
- $V_{BIAS}$  : common mode voltage

# Open Circuit Time Controller



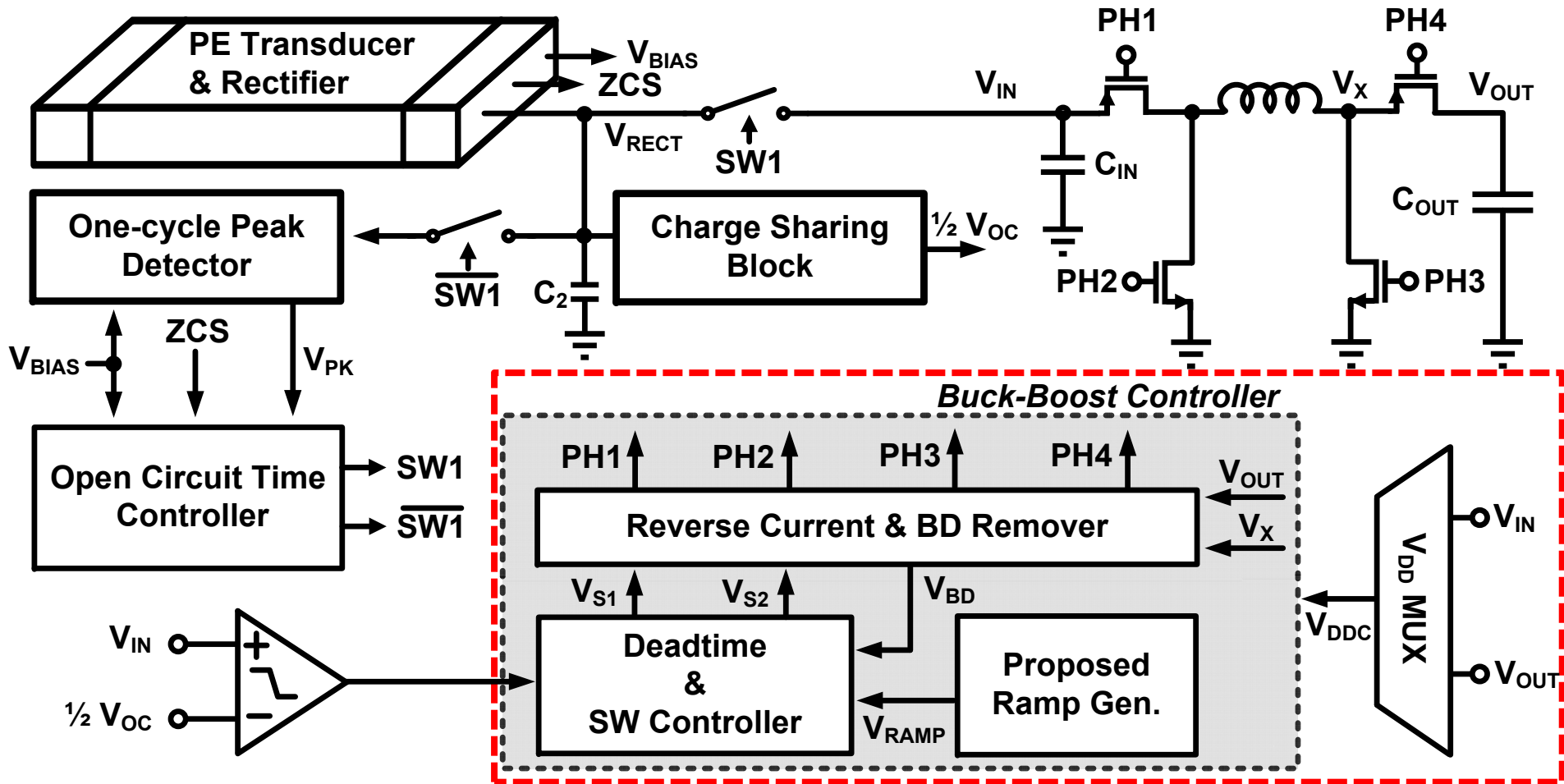
- ZCS signal charges  $C_{OT}$  every cycle
- $SW_1$  opens the rectifier output for one cycle

# Charge Sharing Block



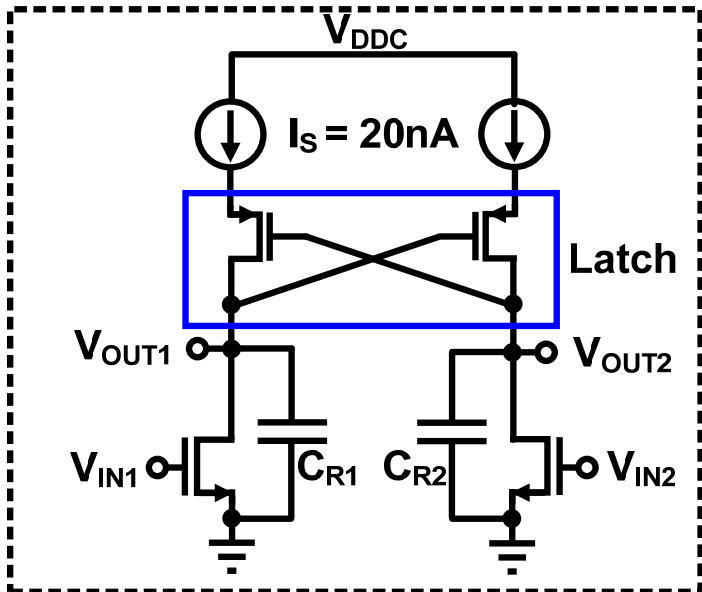
- $V_{MPP2}$  becomes the half of  $V_{OC}$

# Buck-Boost Controller

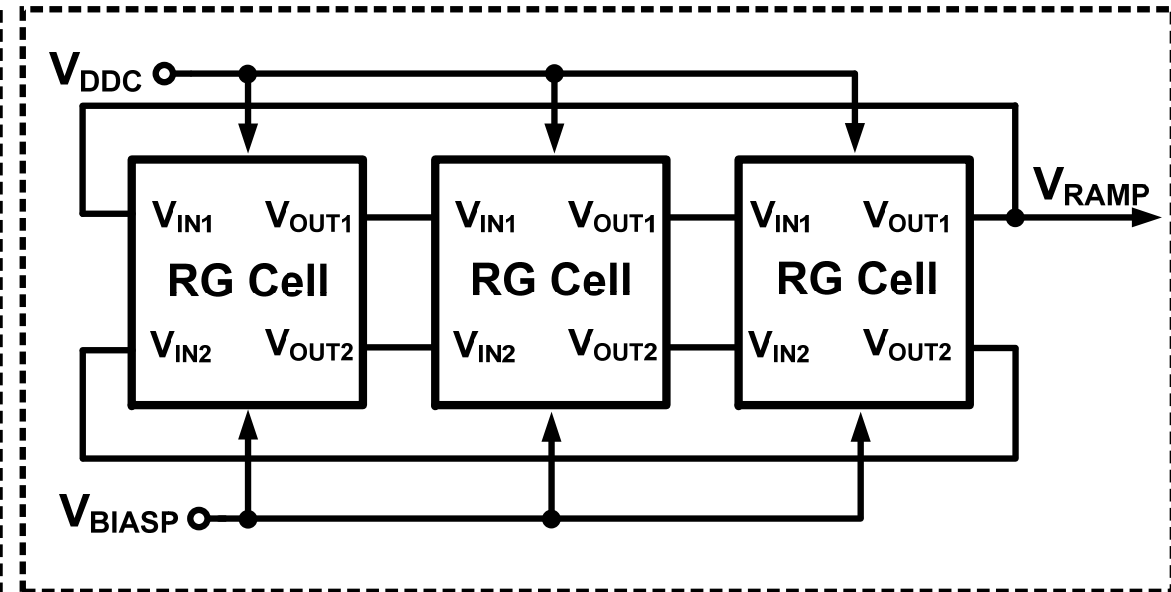


# Ramp Generator (1)

*Ramp Generator (RG) Cell*

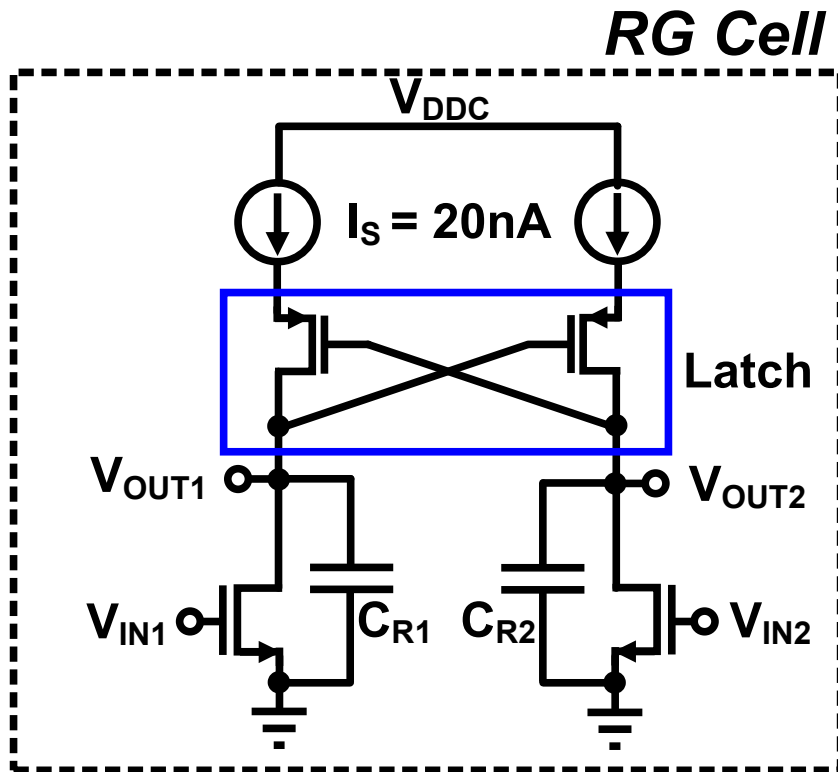


*Ramp Generator*

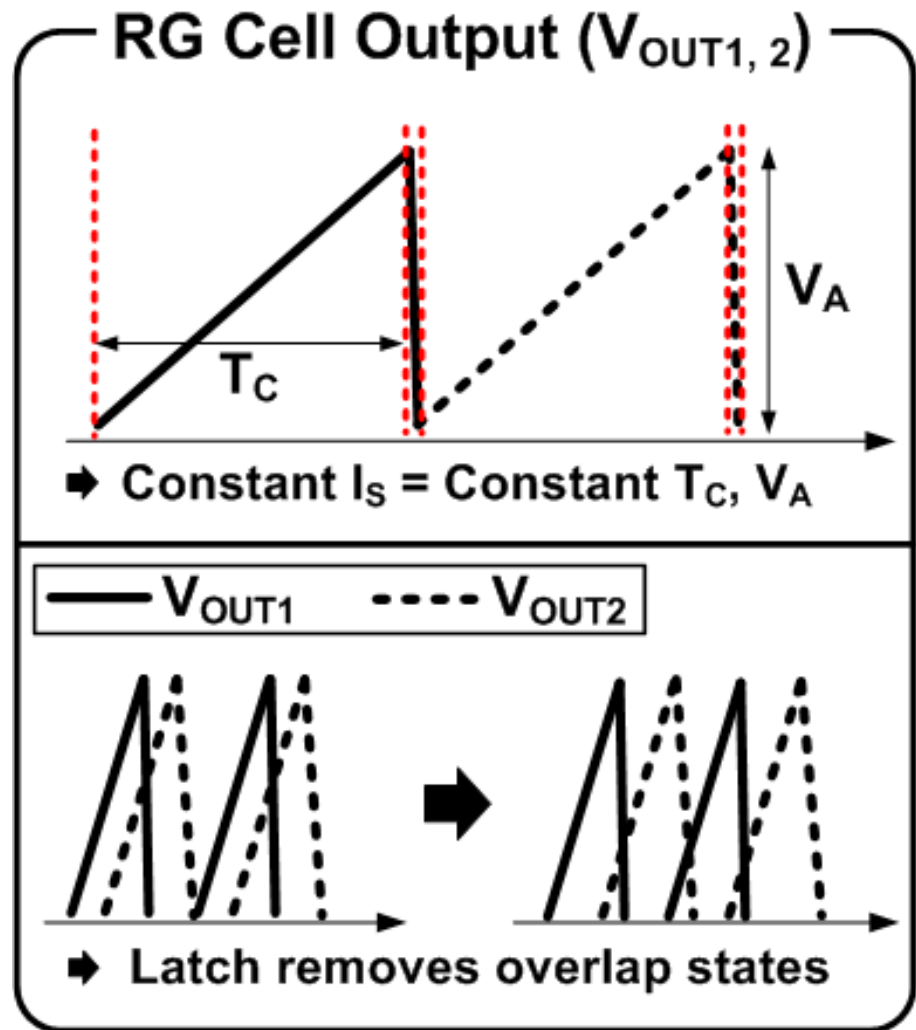


- Deciding frequency and duty of switching signals of buck-boost converter
- Ramp generator with  $V_{DD}$  independence
  - Constant frequency and amplitude
  - Low power consumption and small area

# Ramp Generator (2)

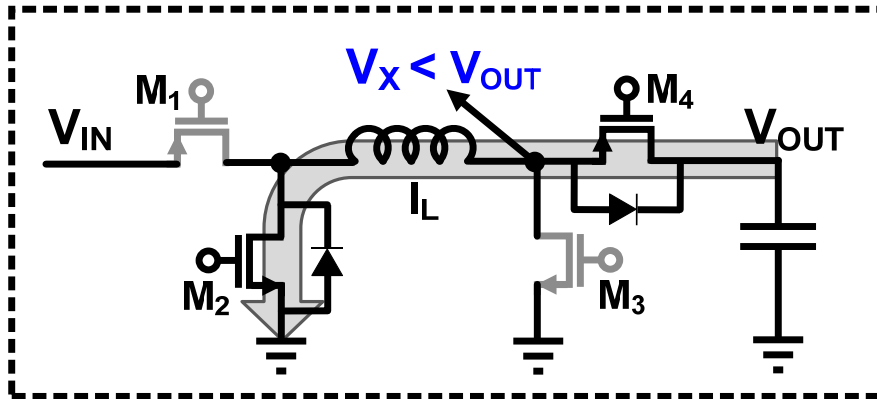


$C_{R1, R2}$  : Small or parasitic capacitors



# Reverse Current & BD Remover (1)

*Reverse Current*

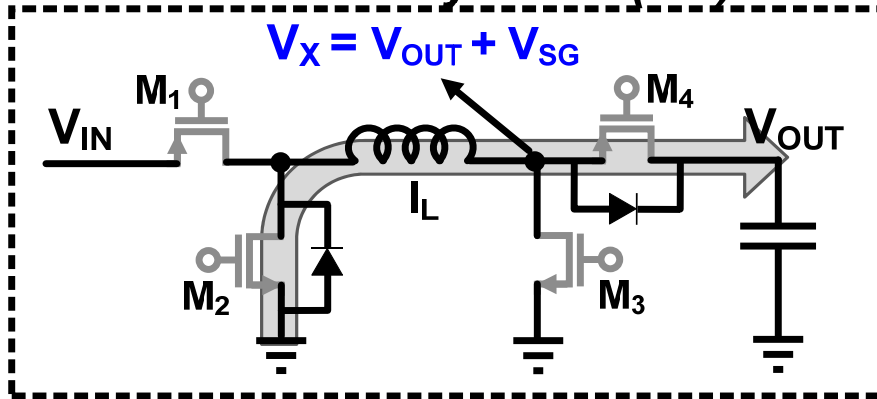


$I_L = 0$  before the end of one cycle



Reverse current from  $V_{OUT}$  to GND  
( $V_{OUT} > V_X$ )

*Body-diode (BD) Effect*



Buck-boost is turned off  
( $V_{IN} < \frac{1}{2} V_{OC}$ ), but  $I_L$  remains

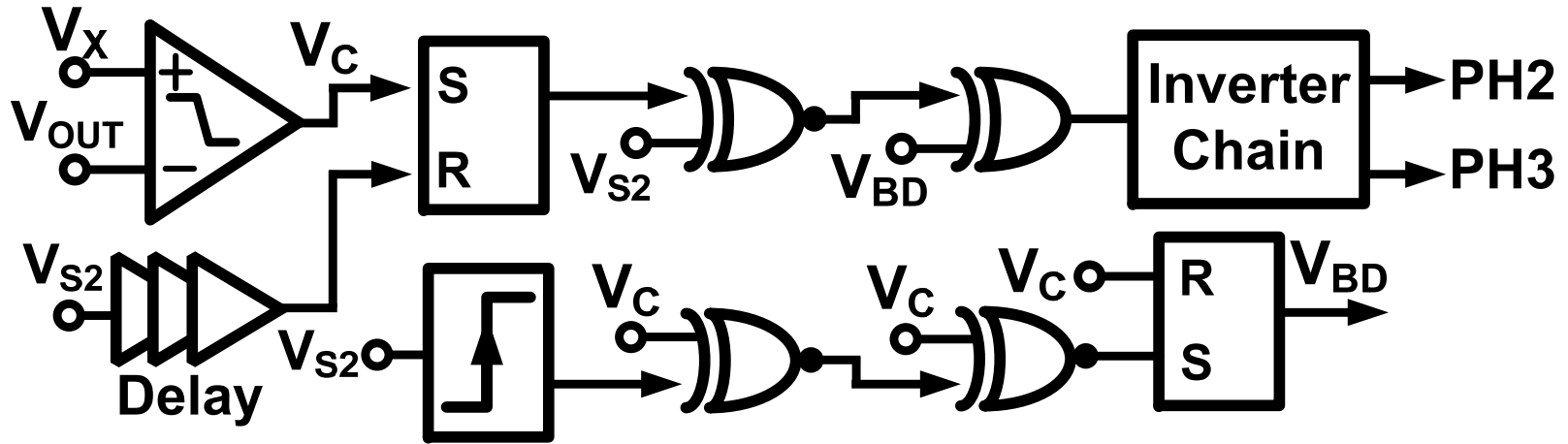


BD effect with large  $V_{DS}$  drop  
( $V_{OUT} > V_X$ )

- Reverse current and BD effect cause large losses



# Reverse Current & BD Remover (2)



**V<sub>s2</sub> = switching signal of buck-boost converter**

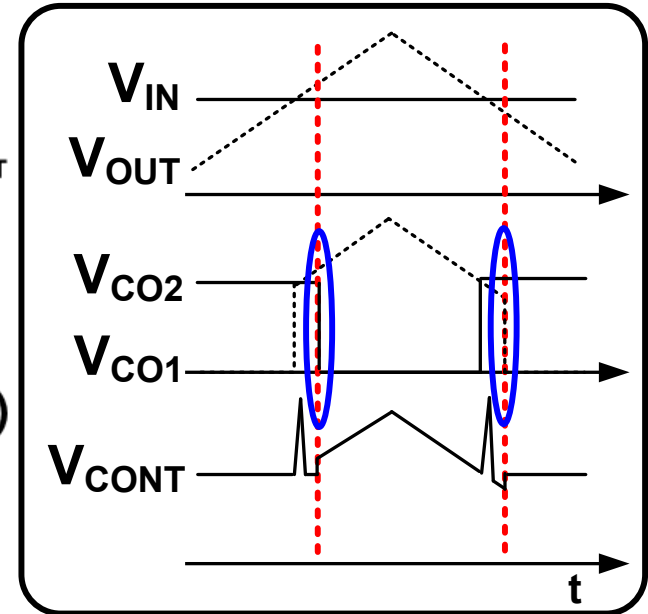
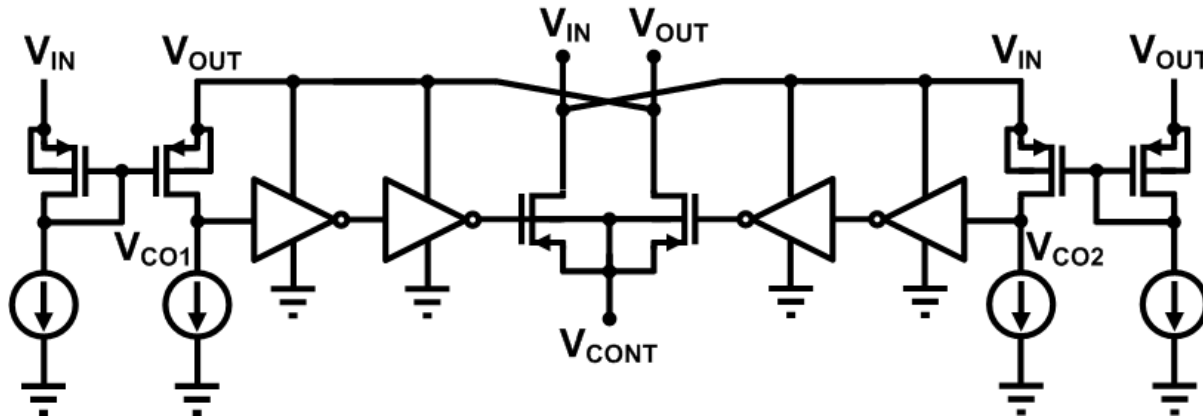
$$V_{OUT} > V_X$$

**Turn off  $M_2$  and  $M_4$   
to prevent the  
reverse current**

$$V_{IN} < \frac{1}{2} V_{OC}, V_{OUT} < V_X$$

## Keep on $M_2$ and $M_4$ to prevent the body diode effect

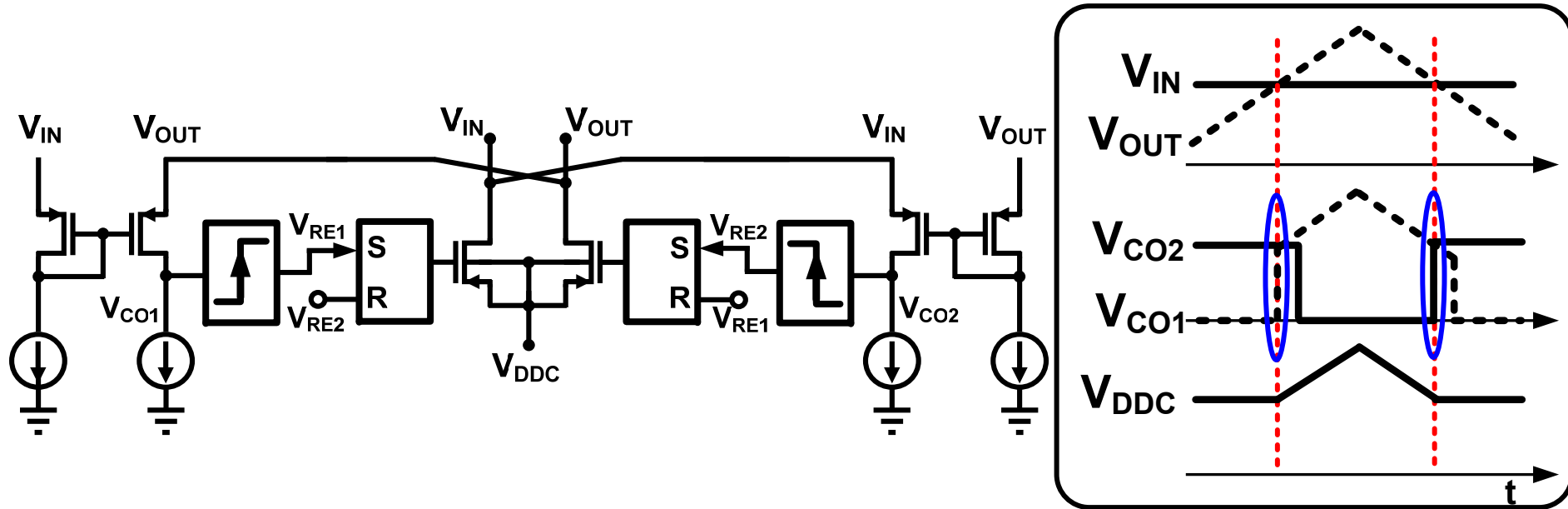
# Conventional Voltage MUX



- **Small bias current for low-power  $V_{DD}$  MUX**
  - Comparator delay
  - Voltage spikes occur at overlapped regions

\* T. Y. Man *et al.*, *JSSC*, vol. 43, pp. 2306–2346, Sep. 2008.

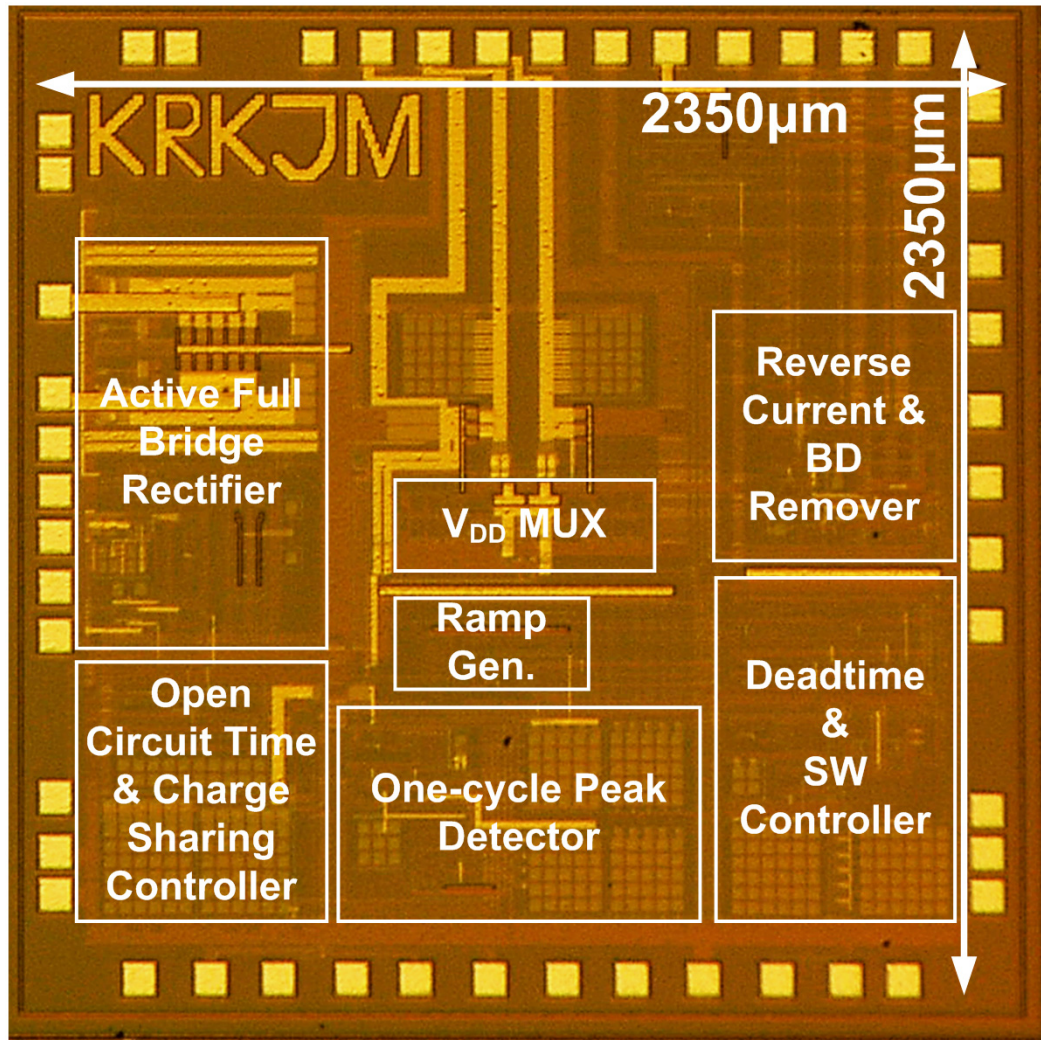
# Proposed Voltage MUX



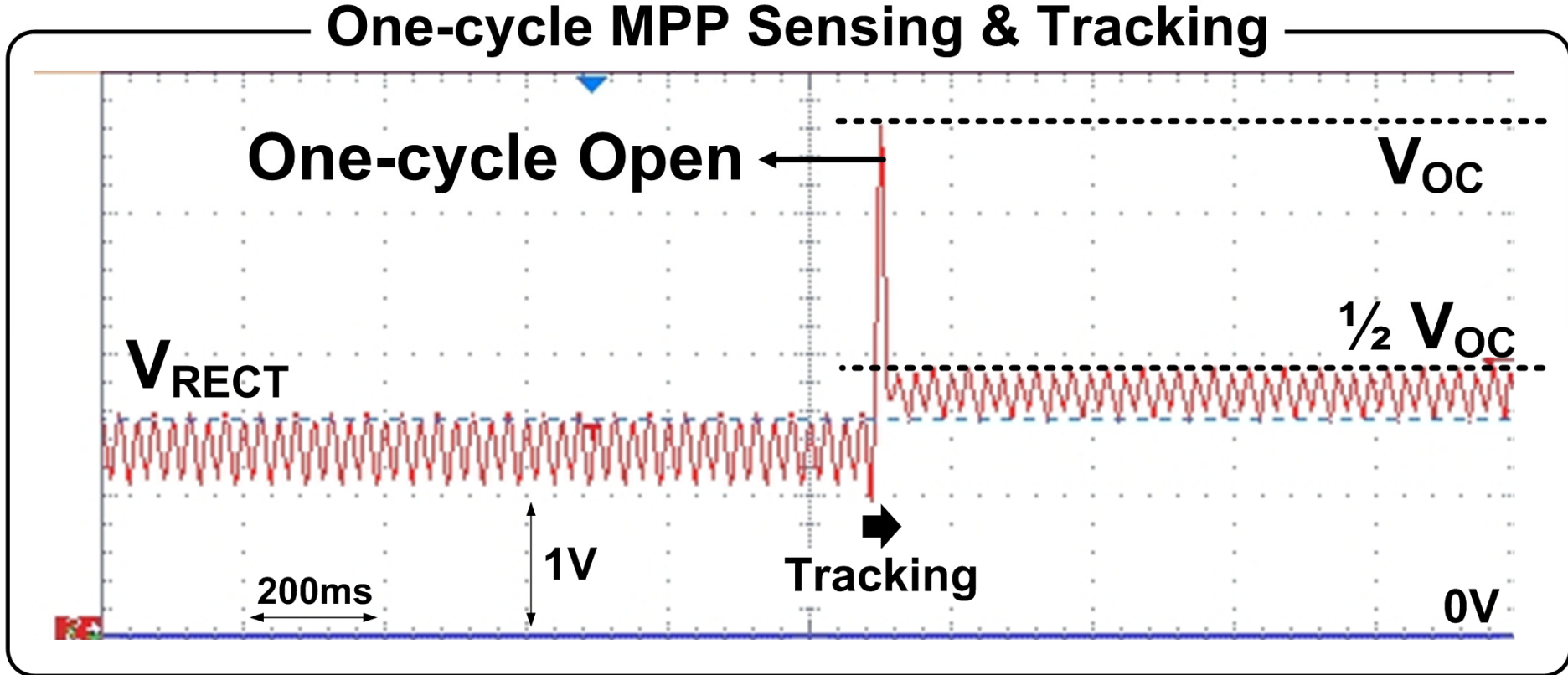
- Rising-edge detector and S-R latch
- Selects a front edge of comparator output
  - No voltage spike

# Chip Photograph

- 0.35 $\mu\text{m}$  BCDMOS process

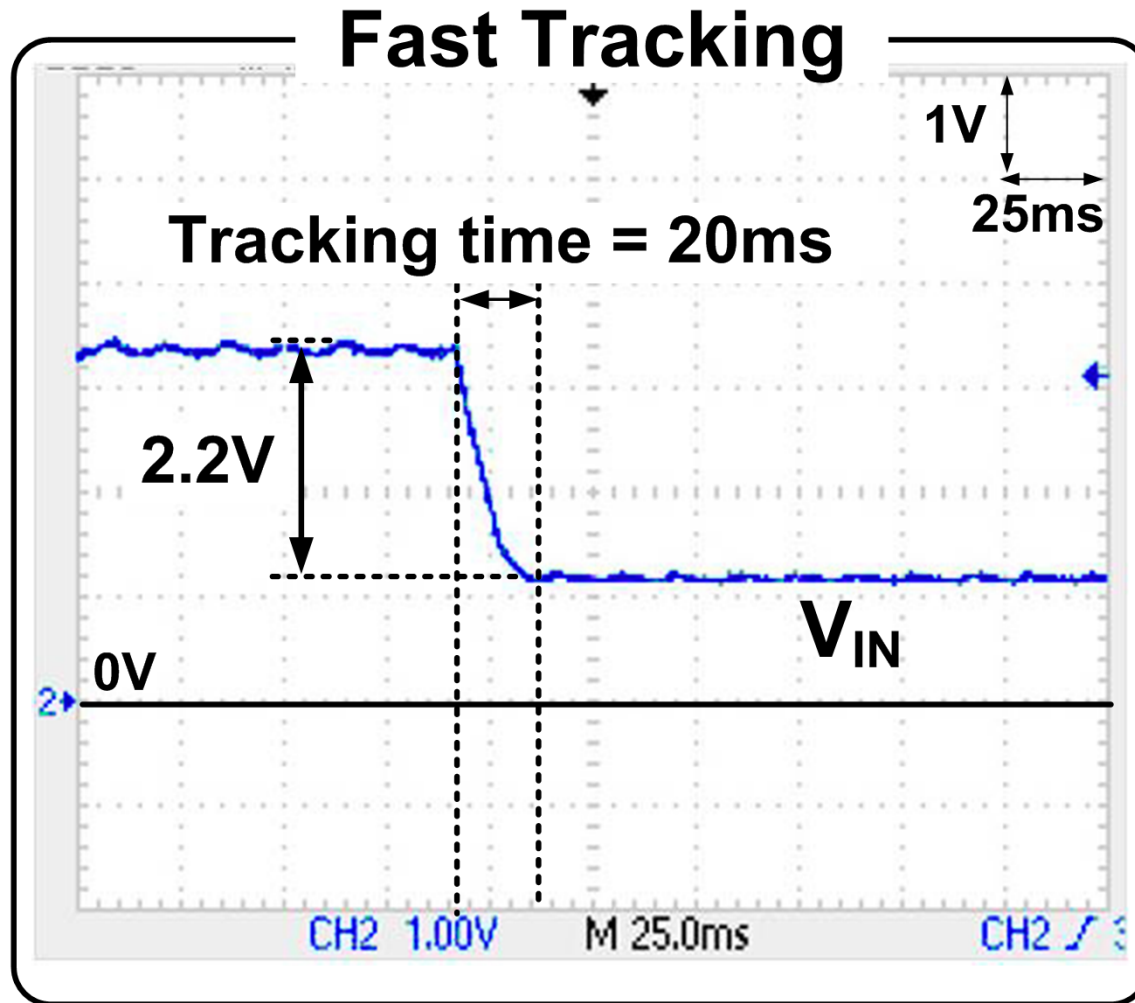


# Measurement Results (1)



- Sensing  $\frac{1}{2} V_{OC}$  in one cycle
- Fast tracking

# Measurement Results (2)

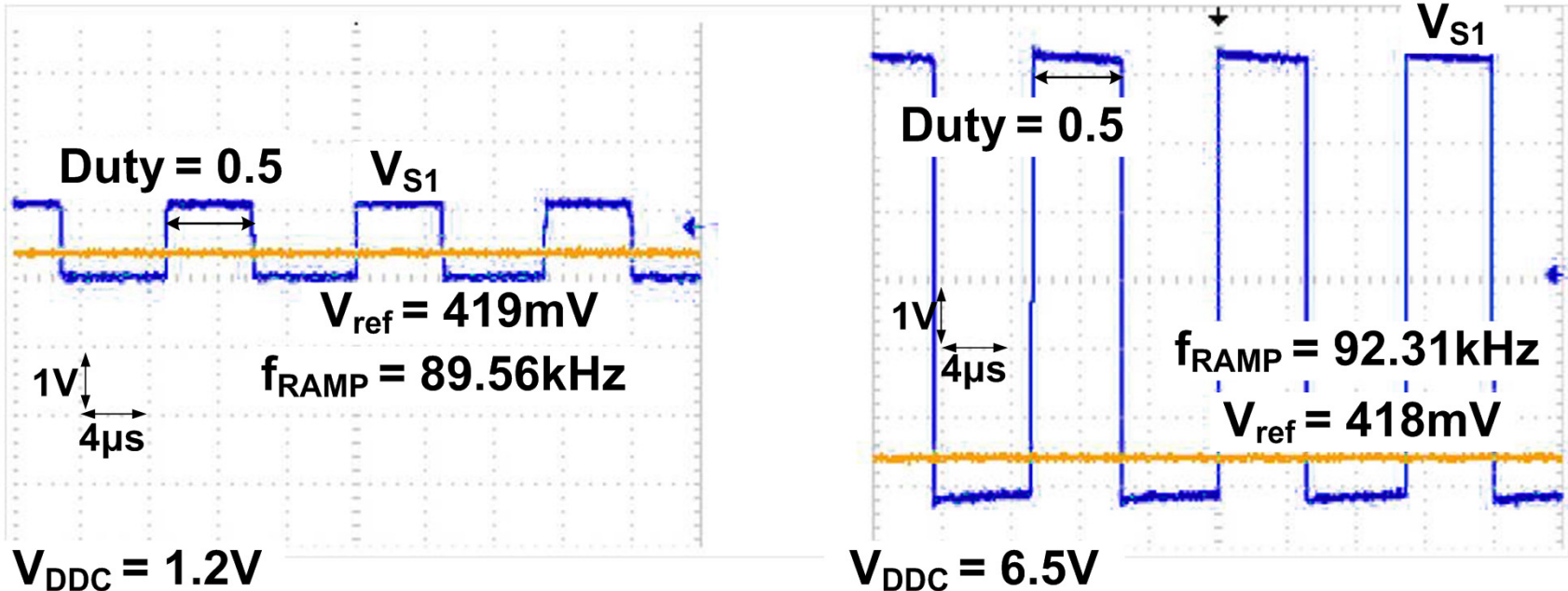


- Tracking time :  $20\text{ms}/(3.4\text{V} \rightarrow 1.2\text{V}) = 9.09\text{ms/V}$



# Measurement Results (3)

## Outputs of SW Controller



- When  $V_{DDC}$  is changed from 1.2V to 6.5V
  - Frequency = 89.5~92.3kHz : changed by 3%
- $V_{ref} = 418\sim 419mV$ 
  - Constant Duty = 0.5

# Comparisons

	ISSCC 2013*	TPEL 2012**	This work
Process	0.25 $\mu$ m BCD	Off-chip	0.35 $\mu$ m BCD
Input voltage	5 – 60V	3 – 25V	1 – 7V
Output voltage	2 – 5 V	3V –	1 – 8V
Input power	25 $\mu$ W – 1.6mW	N/A	33 $\mu$ W – 10mW
Converter type	Buck	Buck-Boost	Buck-Boost
Max. PCE	88.9%	76%	80%
MPPT algorithm	Variable step-size P&O	P&O	Fractional $V_{OC}$
Max. MPPT efficiency	99.9%	97%	99.9%
MPPT time	80ms/V	7.83s/V	9.09ms/V

\* S. Stanzione *et al.*, *ISSCC*, pp. 74–75, Feb. 2013.

\*\* N. Kong *et al.*, *TPEL*, vol. 27, pp. 2298–2308, May 2012.



# Conclusions

- **One-cycle MPP sensing method is proposed**
- **MPPT time : 9x faster**
- **Low-power control blocks :**
  - Ramp generator with  $V_{DD}$  independence
  - Voltage MUX without voltage spikes
- **Prevent BD effect & reverse current**

---

# **A 34V Charge Pump in 65nm Bulk CMOS Technology**

***Yousr Ismail<sup>1</sup>, Haechang Lee<sup>2</sup>, Sudhakar Pamarti<sup>1</sup> and Chih-Kong Ken Yang<sup>1</sup>***

***<sup>1</sup>University of California, Los Angeles, CA***

***<sup>2</sup>Altera, San Jose, CA***



---

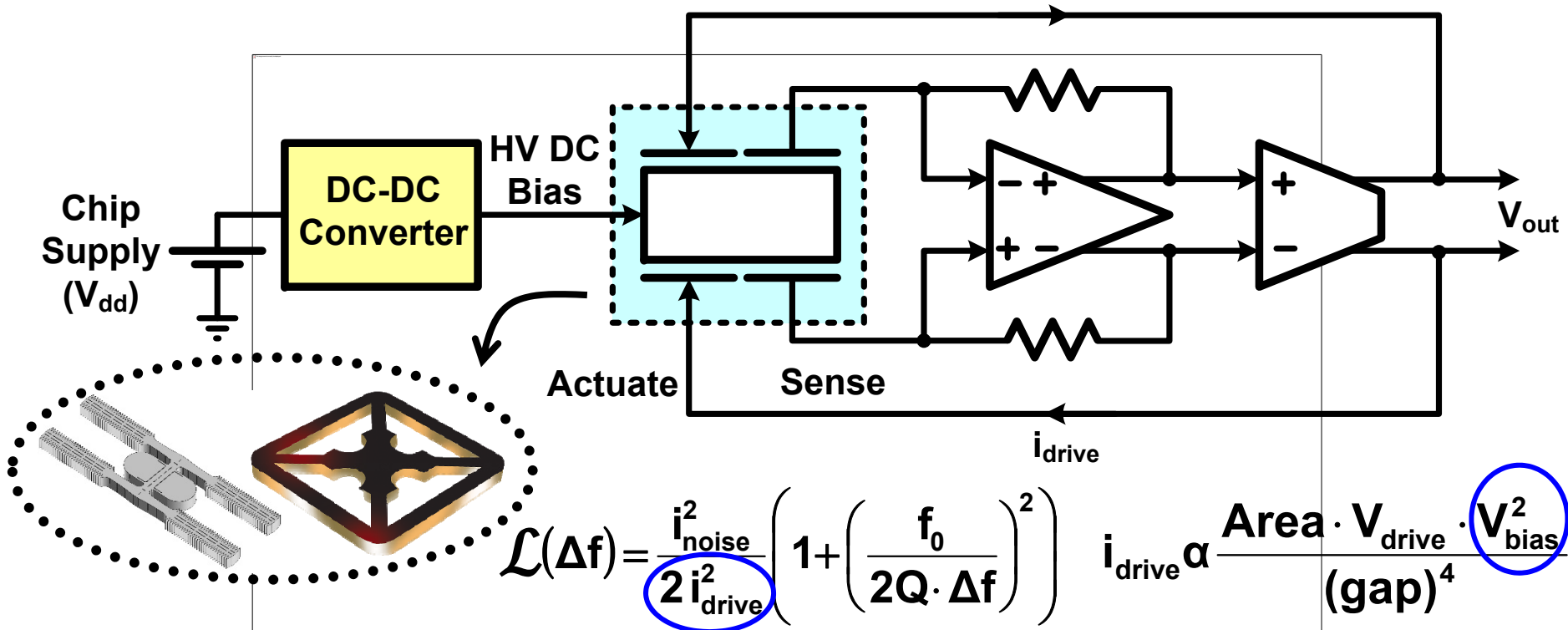
***High Performance Mixed-Mode Circuits Group***

# Outline

---

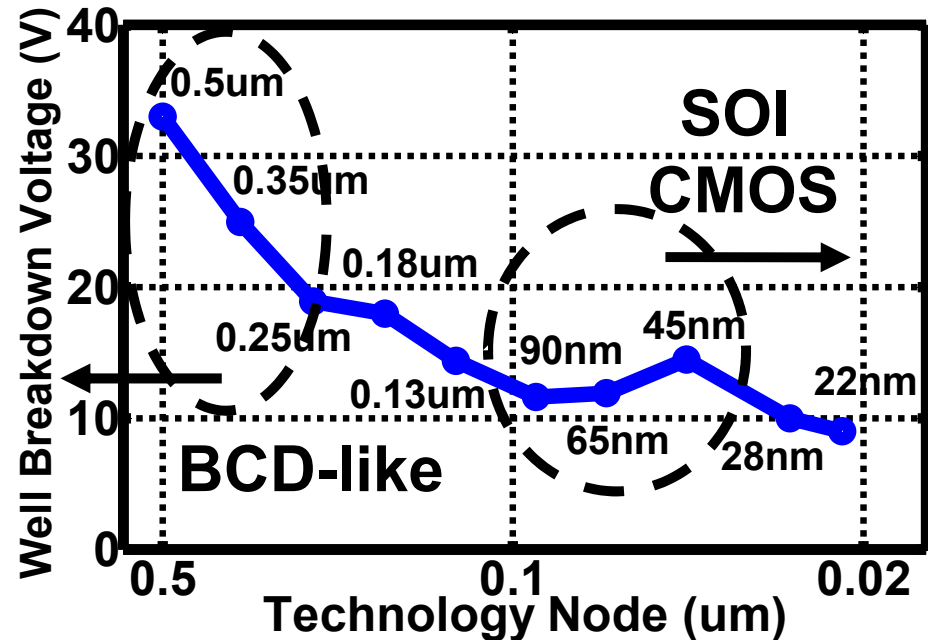
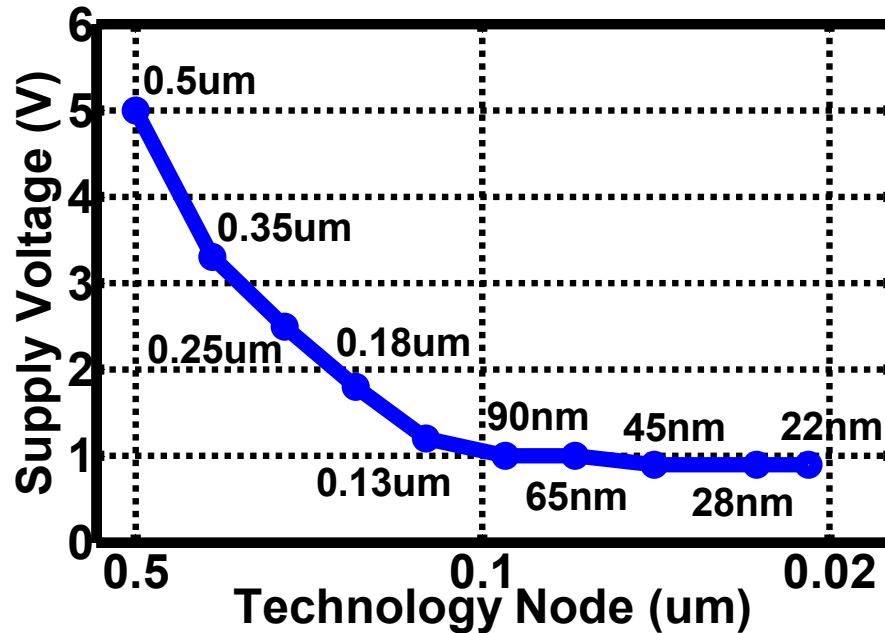
- **Motivation**
- **Technology Limitations**
- **Charge Pump Design**
- **Measurement Results**
- **Conclusion**

# MEMS Resonator System



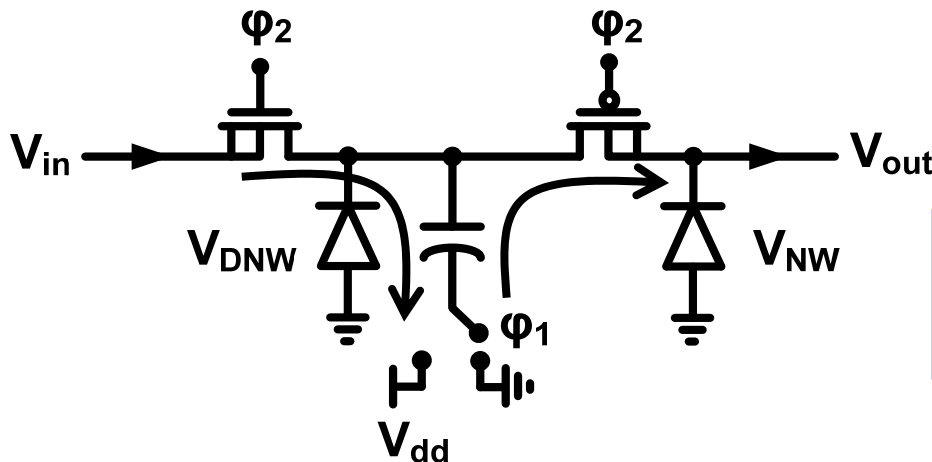
- Cellular and GPS applications demand excellent phase noise performance
- Power conversion efficiency is critical for portable applications

# Bulk CMOS Technology Limitations



- Transistor voltage ratings shrink as technology scales down
- Technology maximum voltage handling is limited to the well diodes breakdown

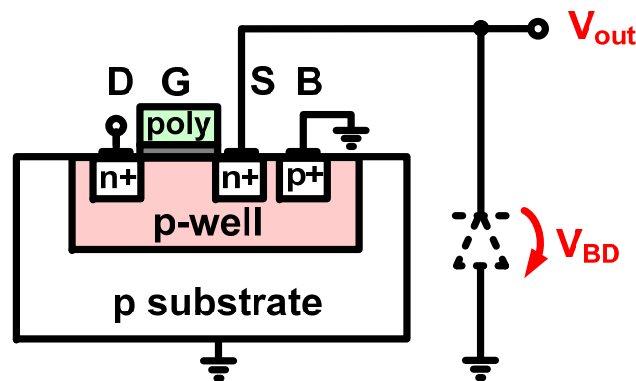
# Voltage Tolerance in Bulk CMOS



Symbol	$V_{BD}$	Description
$V_{NP}$	8V	n+/pwell diode
$V_{NW}$	12V	nwell/psub diode
$V_{DNW}$	12V	dnwell/psub diode

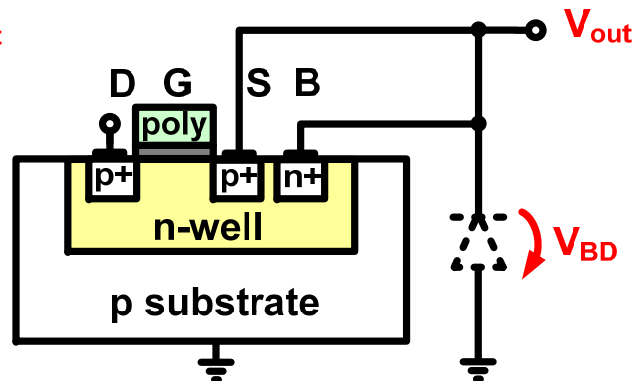
*Approximate values for 65nm CMOS technology*

$$V_{max} = \min(V_{NW}, V_{DNW})$$



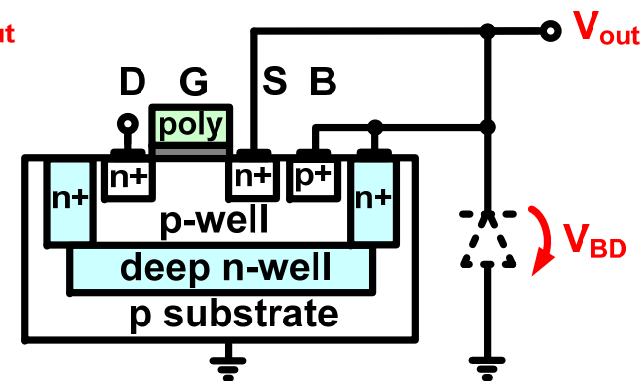
**NMOS**

$$V_{max} = V_{NP}$$



**PMOS**

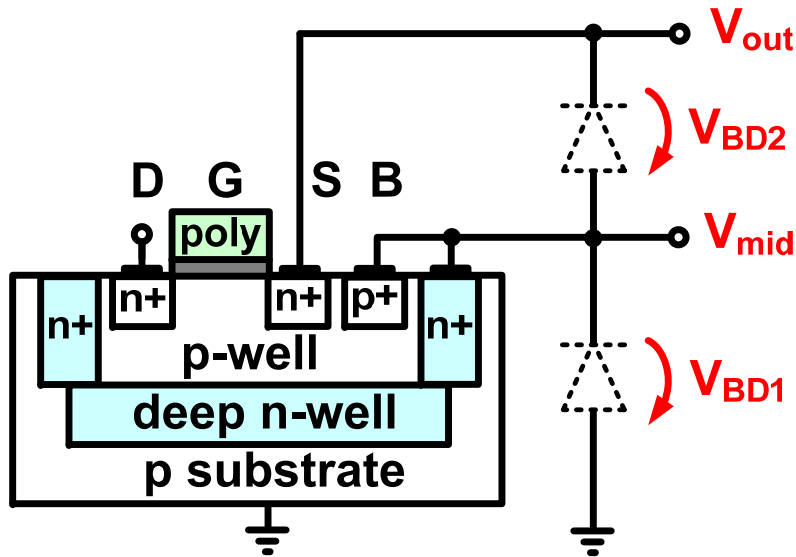
$$V_{max} = V_{NW}$$



**DNWELL NMOS**

$$V_{max} = V_{DNW}$$

# Extended CMOS Voltage Tolerance (1/2)



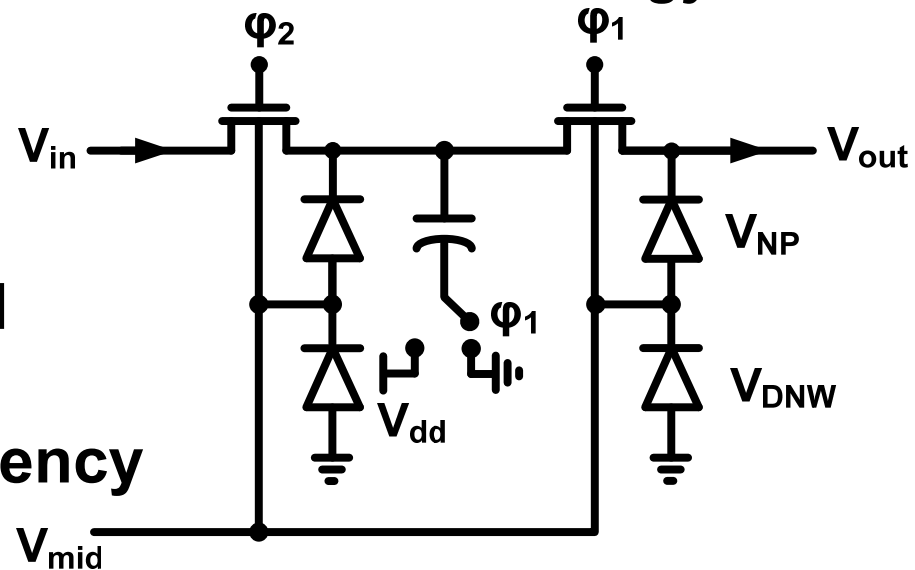
Symbol	$V_{BD}$	Description
$V_{NP}$	8V	n+/pwell diode
$V_{NW}$	12V	nwell/psub diode
$V_{DNW}$	12V	dnwell/psub diode

*Approximate values for 65nm CMOS technology*

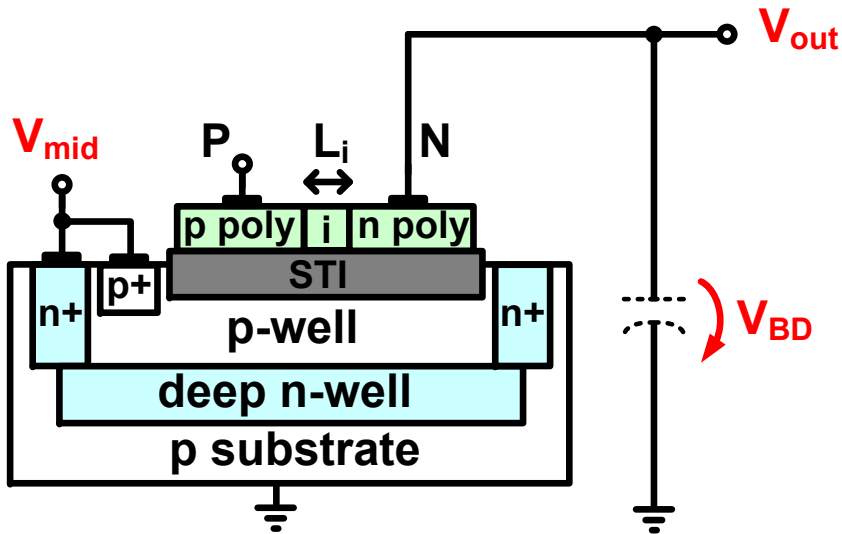
**Proposed deep-nwell bias**

$$V_{\max} = V_{DNW} + V_{NP} = 20V$$

- An all-NMOS CP is proposed
- Backgate bias reduces efficiency



# Extended CMOS Voltage Tolerance (2/2)



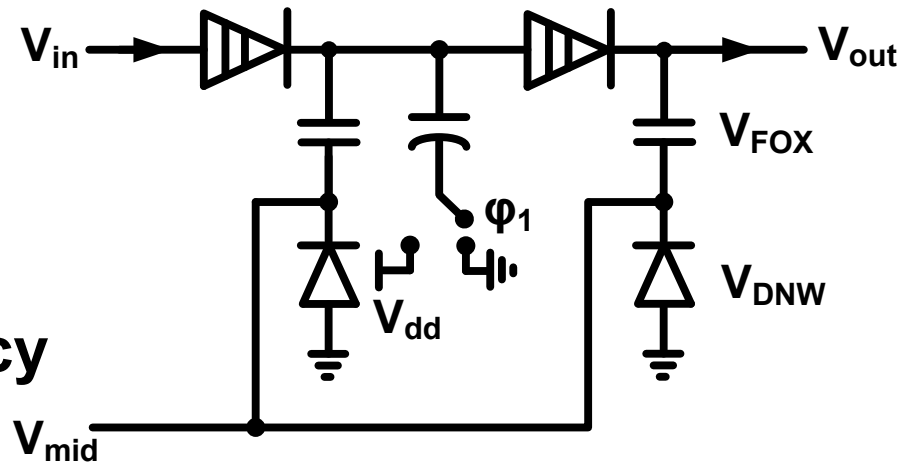
## Polysilicon Diodes

$$V_{\max} = V_{\text{DNW}} + V_{\text{FOX}} = 100\text{V}$$

- Only diodes can be used
- Diode drop reduces efficiency

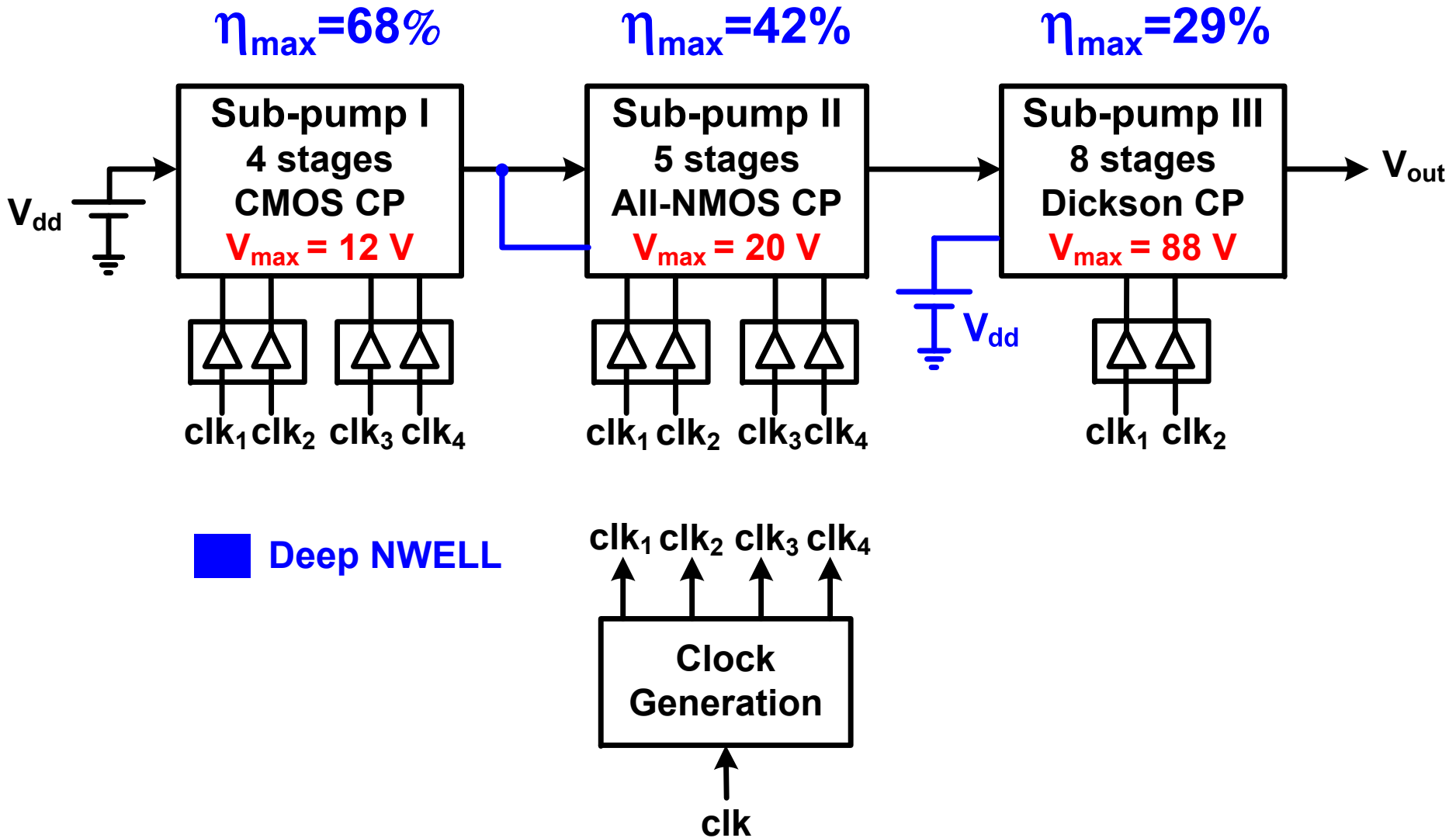
Symbol	$V_{\text{BD}}$	Description
$V_{\text{NP}}$	8V	n+/pwell diode
$V_{\text{NW}}$	12V	nwell/psub diode
$V_{\text{DNW}}$	12V	dnwell/psub diode
$V_{\text{FOX}}$	88V	STI capacitor

*Approximate values for 65nm CMOS technology*

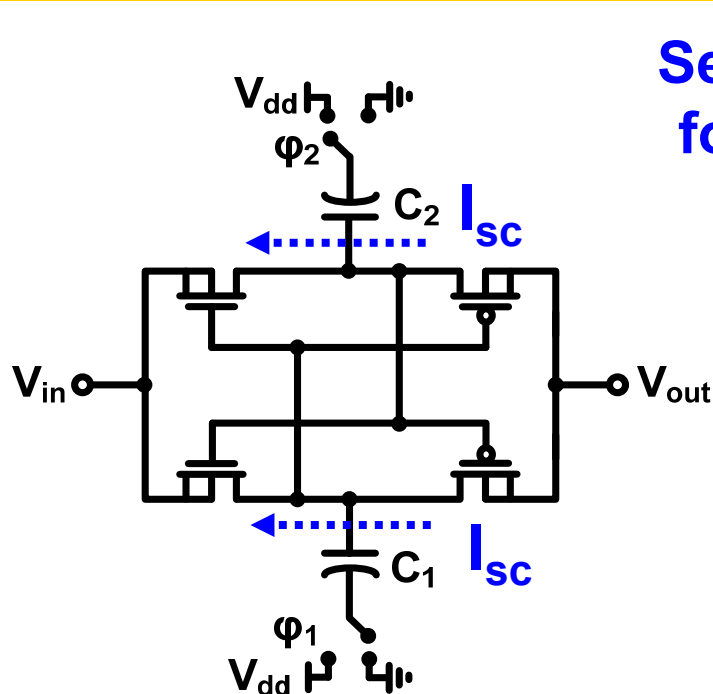




# Charge Pump Architecture

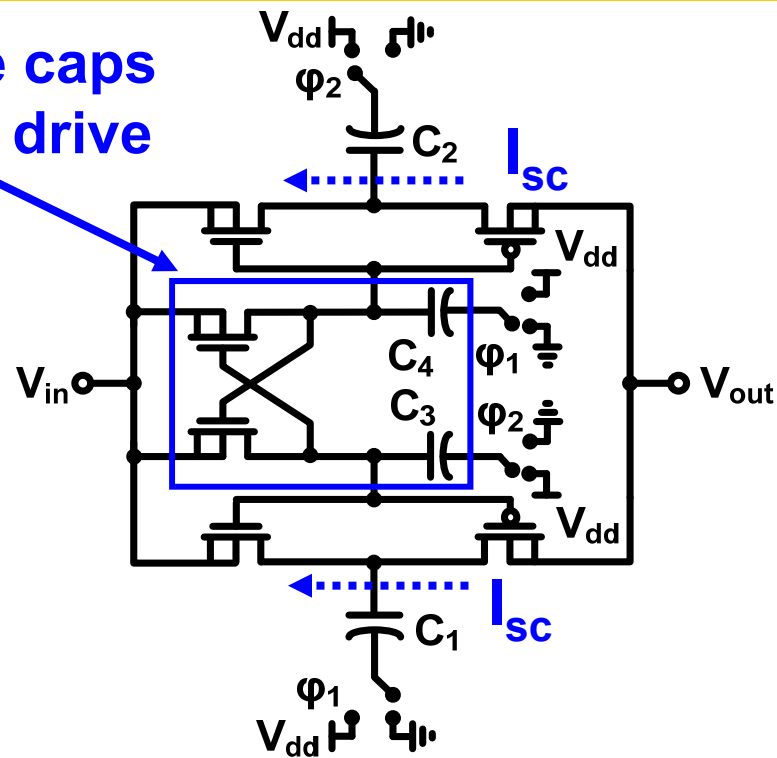


# Sub-pump Design

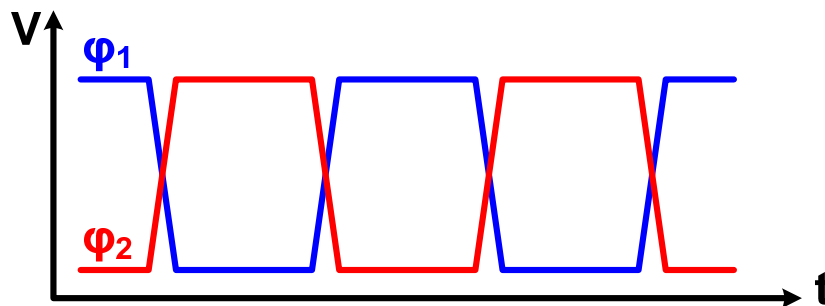


**Two-phase Voltage Doubler (TPVD)**

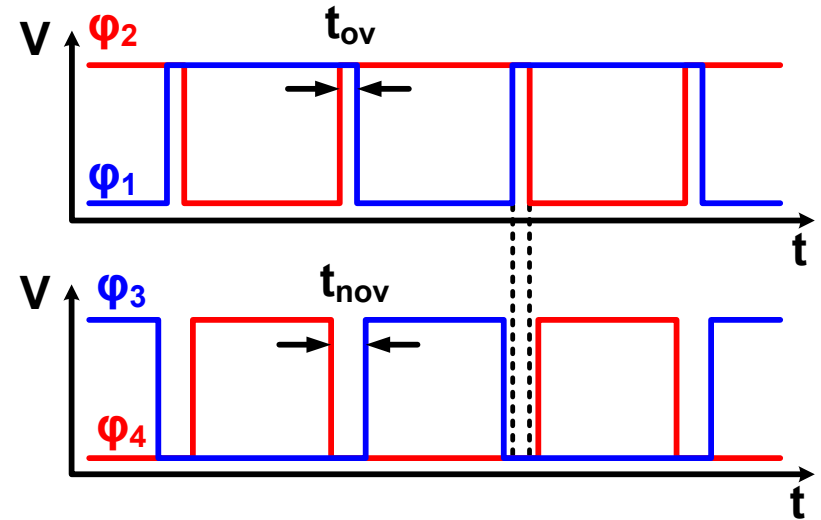
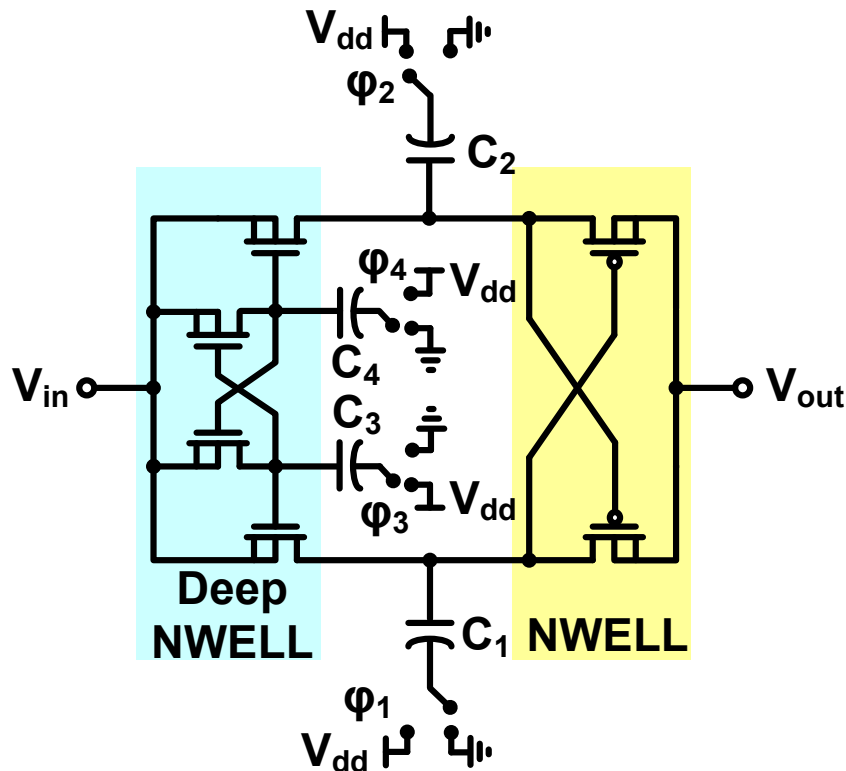
Separate caps  
for gate drive



**Improved TPVD**



# Sub-pump I Design



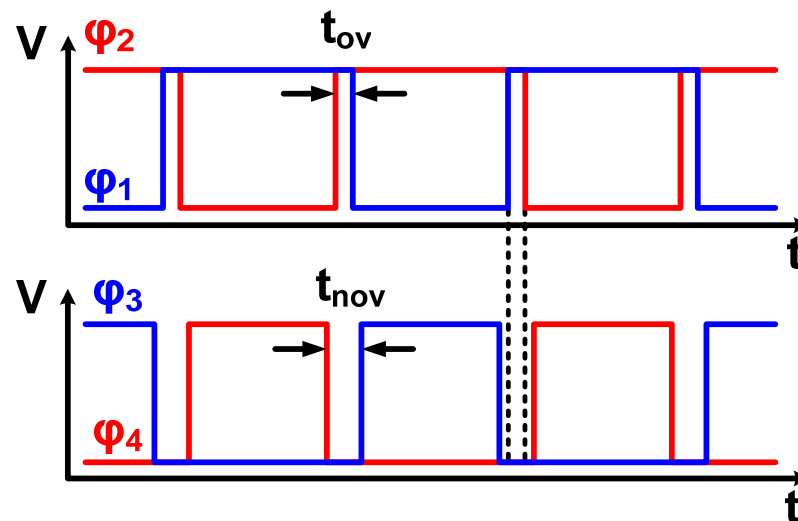
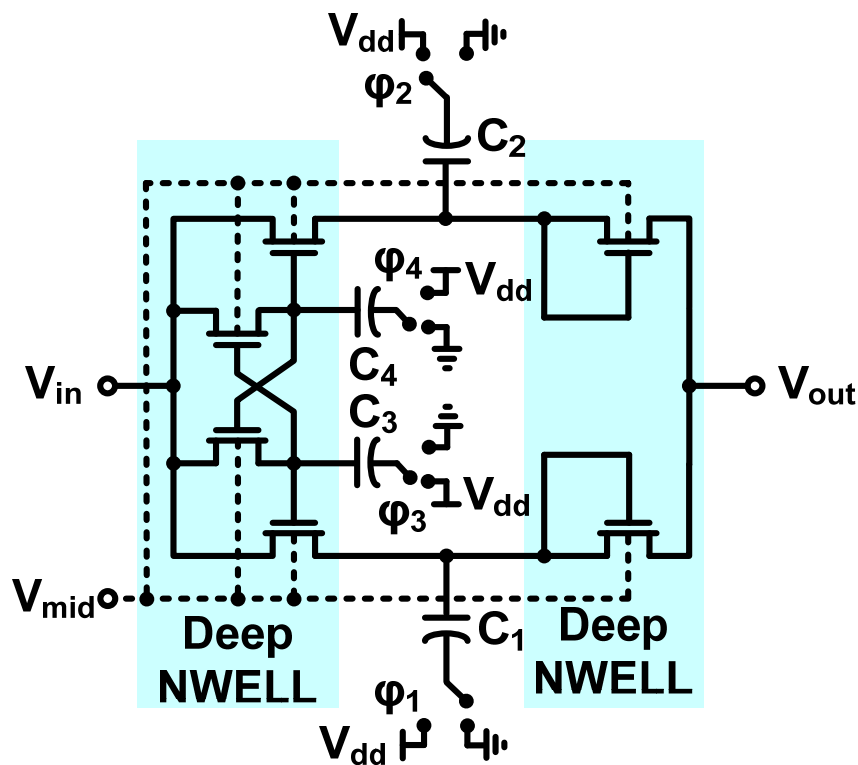
$$0 < t_{ov} < t_{nov}$$

**Clock timing guarantees  
break-before-make switching**

$$V_{out} = f(\alpha V_{dd}, I_{load}) \quad \alpha = 1/(1 + C_p/C)$$

- CMOS four phase voltage doubler (FPVD)
- 4 cascaded stages/ 2.5V thick oxide devices

# Sub-pump II Design



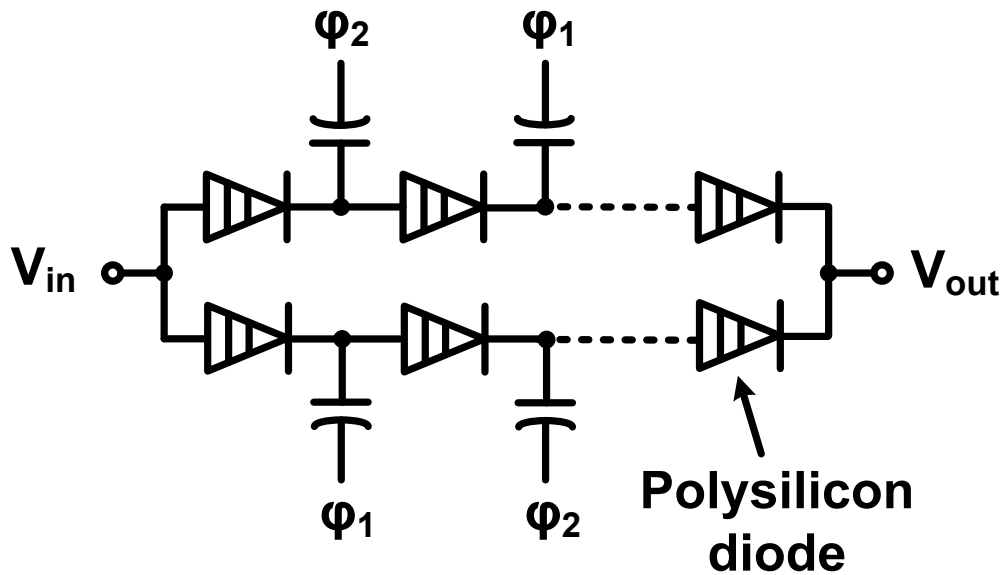
$$-t_{nov} < t_{ov} < t_{nov}$$

**Clock timing guarantees  
break-before-make switching**

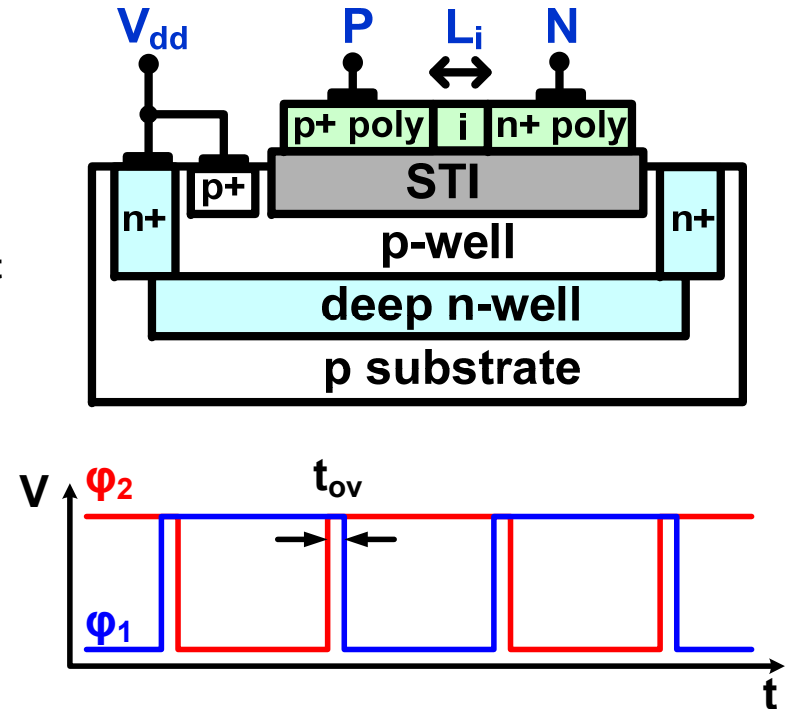
$$V_{out} = f(\alpha V_{dd} - V_{th}, I_{load}) \quad V_{th} = g(V_{out} - V_{mid})$$

- All-NMOS four phase voltage doubler (FPVD)
- 5 cascaded stages/ 2.5V thick-oxide devices

# Sub-pump III Design

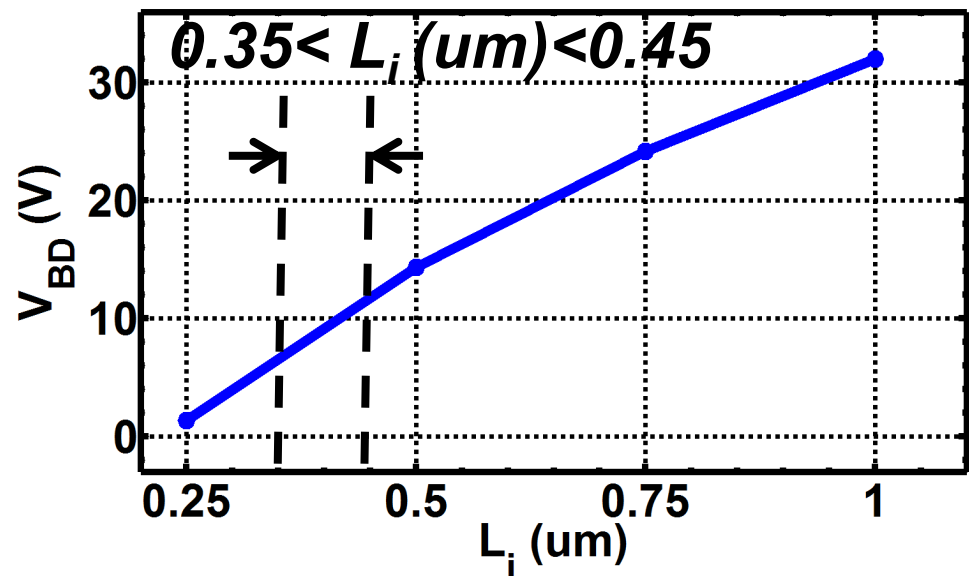
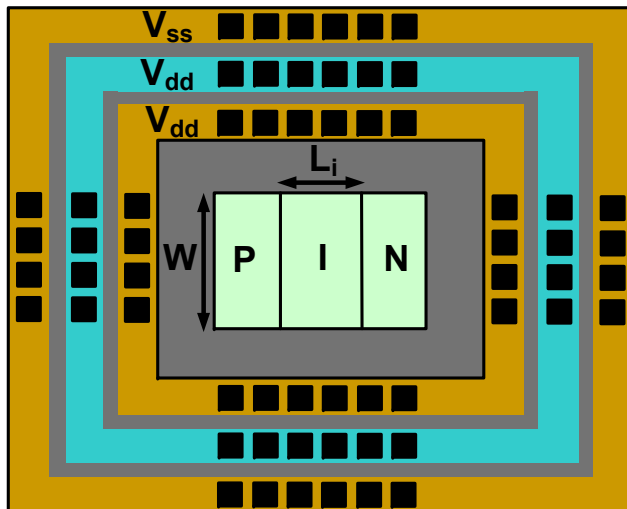
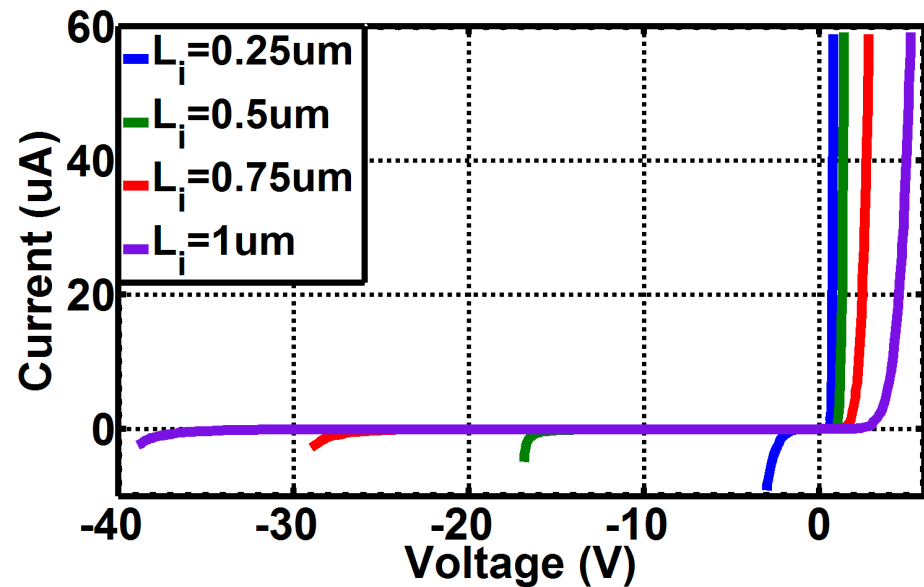
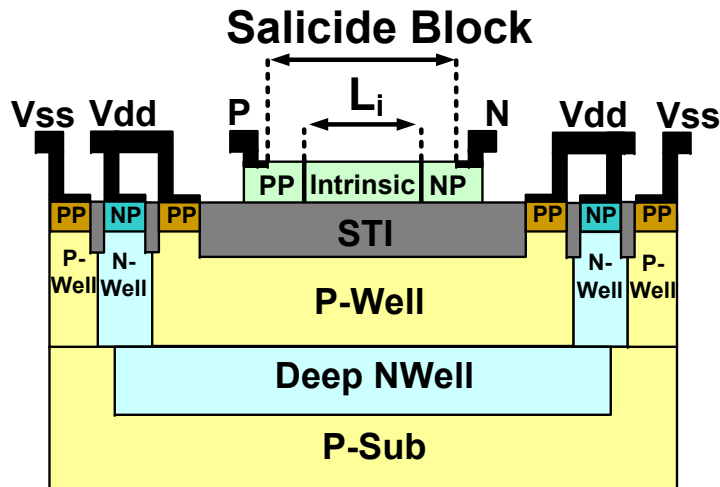


$$V_{out} = f(\alpha V_{dd} - V_D, I_{load})$$

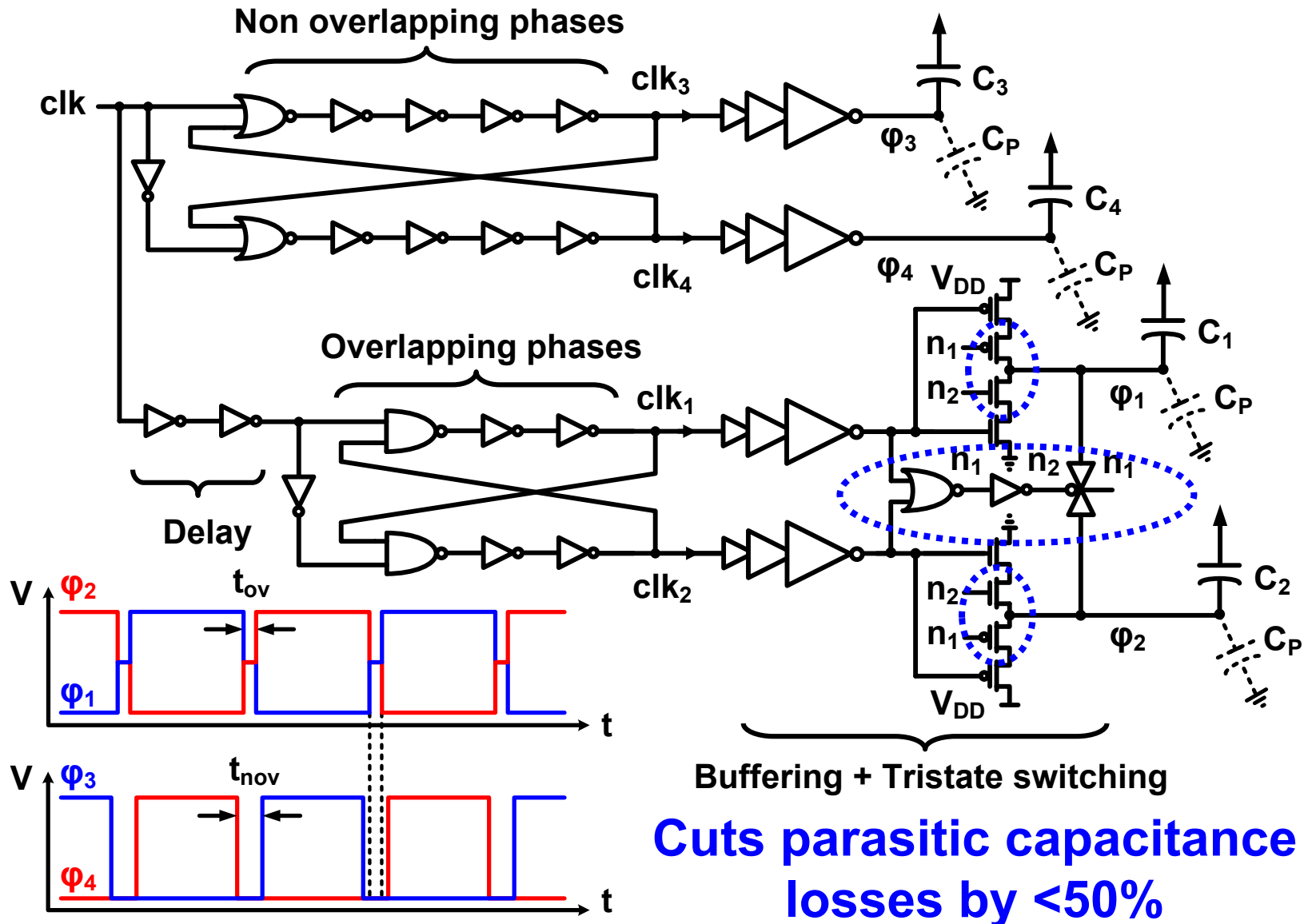


- Dickson charge pump using polysilicon diodes
- Sub-pump consists of 8 stages

# Polysilicon Diodes

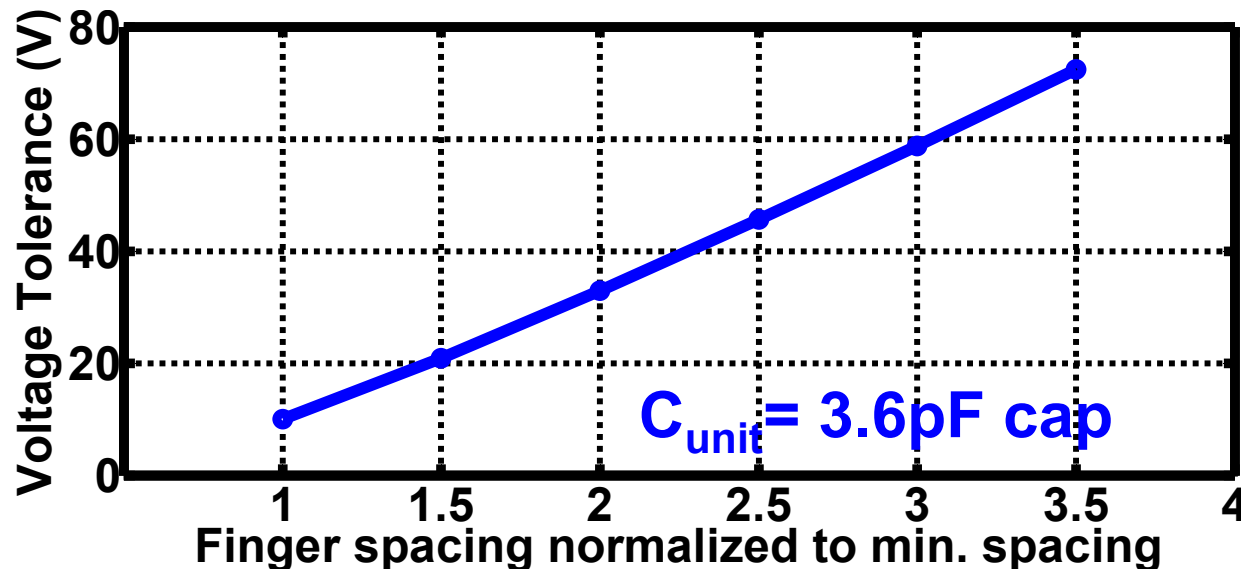


# Clock Generation and Drive



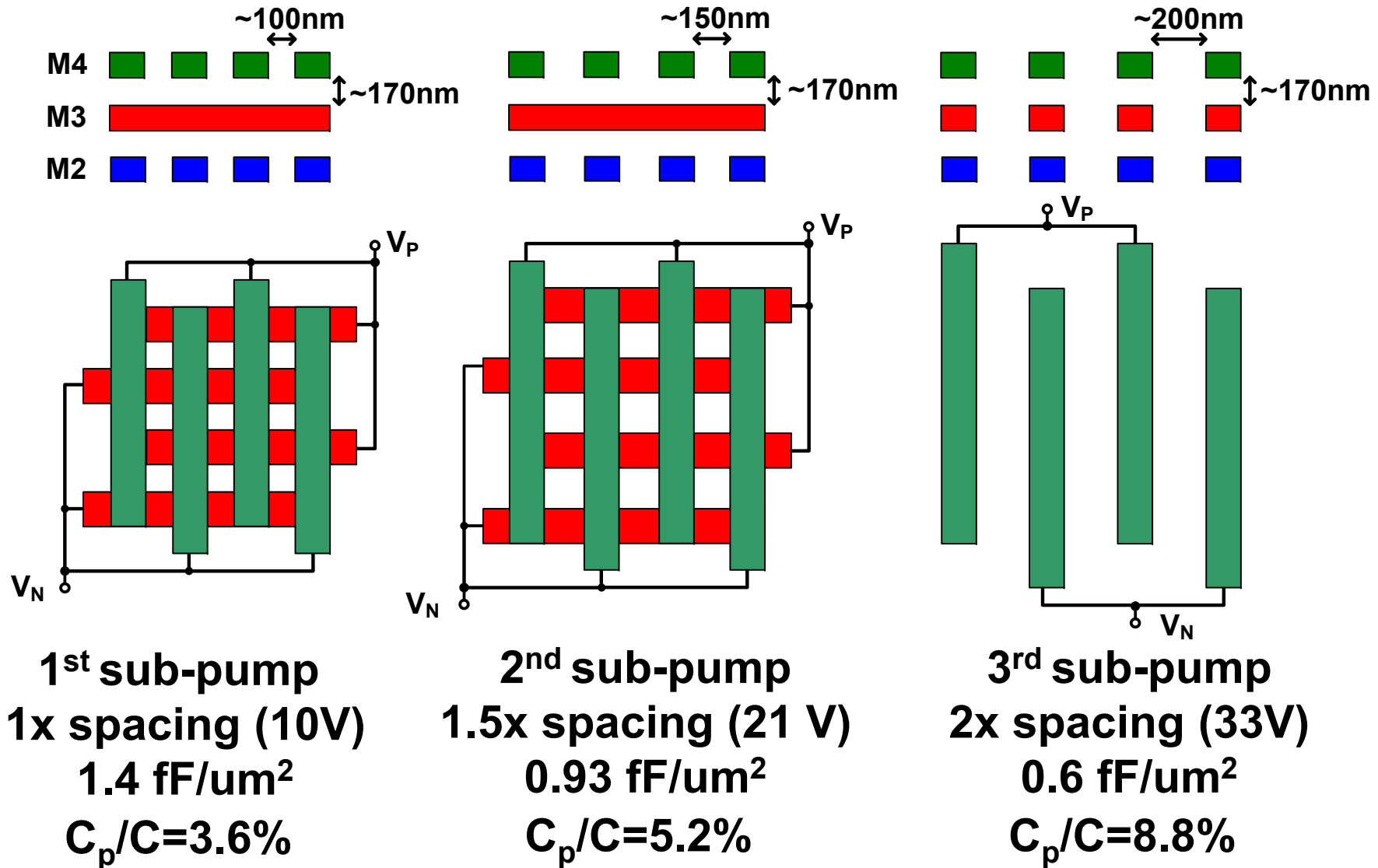
# Capacitor Design for Reliability (1/2)

- Time-dependent dielectric breakdown (TDDB)
- Reliability criterion is 0.01% failure over 10 years at 85°C
  1. Weibull statistics  $CDF = 1 - \exp[-(t/\tau)^\beta]$
  2. Accelerated sqrt-E model  $\tau \propto \exp[\gamma(\sqrt{V_{st}} - \sqrt{V_{op}})]$
  3. Arrhenius temp. Relation  $\tau \propto \exp[(E_a/K)(1/T_{op} - 1/T_{st})]$
  4. Poisson area scaling  $\tau \propto (A_{st}/A_{op})^\beta$

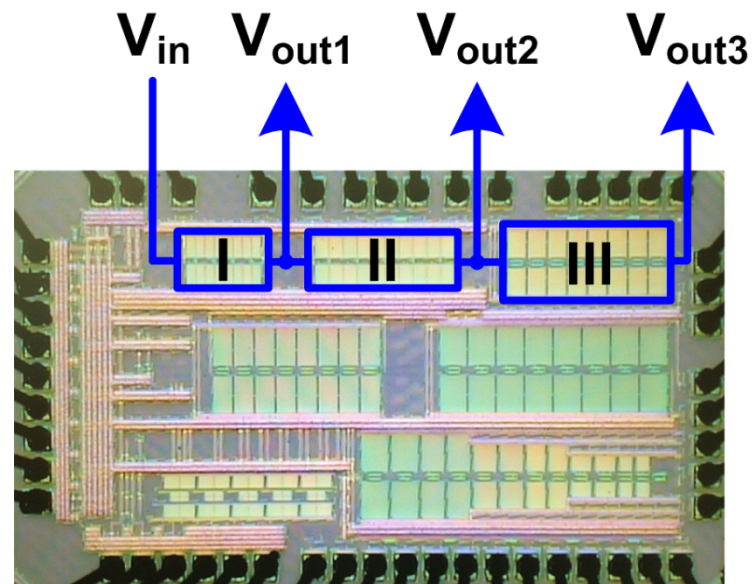
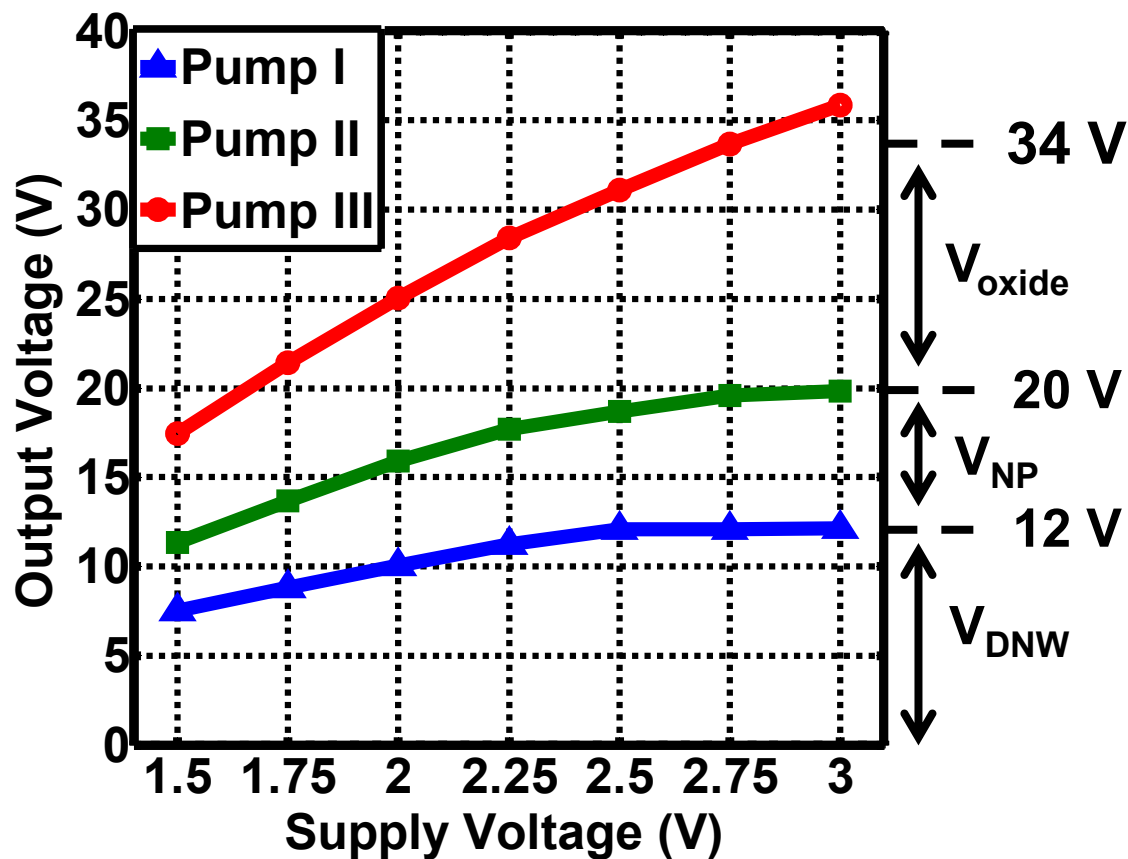




# Capacitor Design for Reliability (2/2)



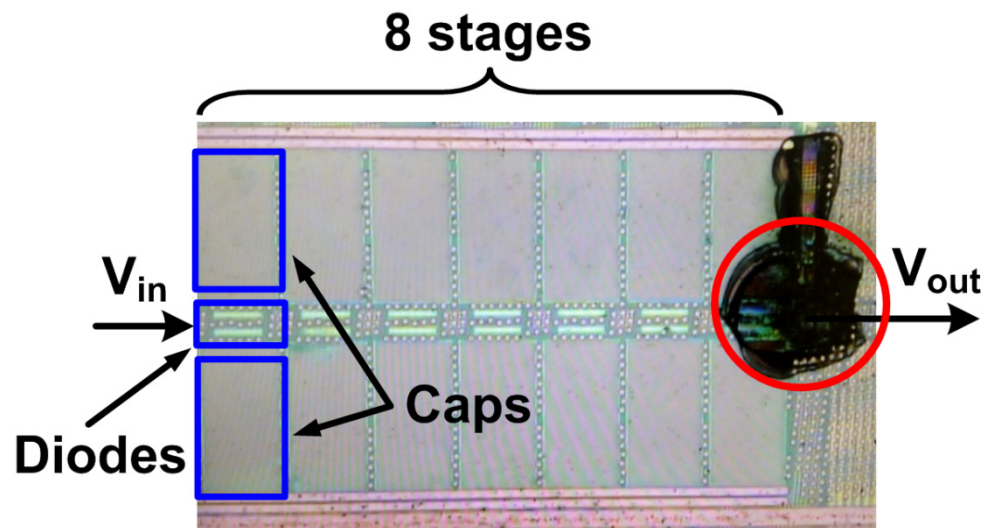
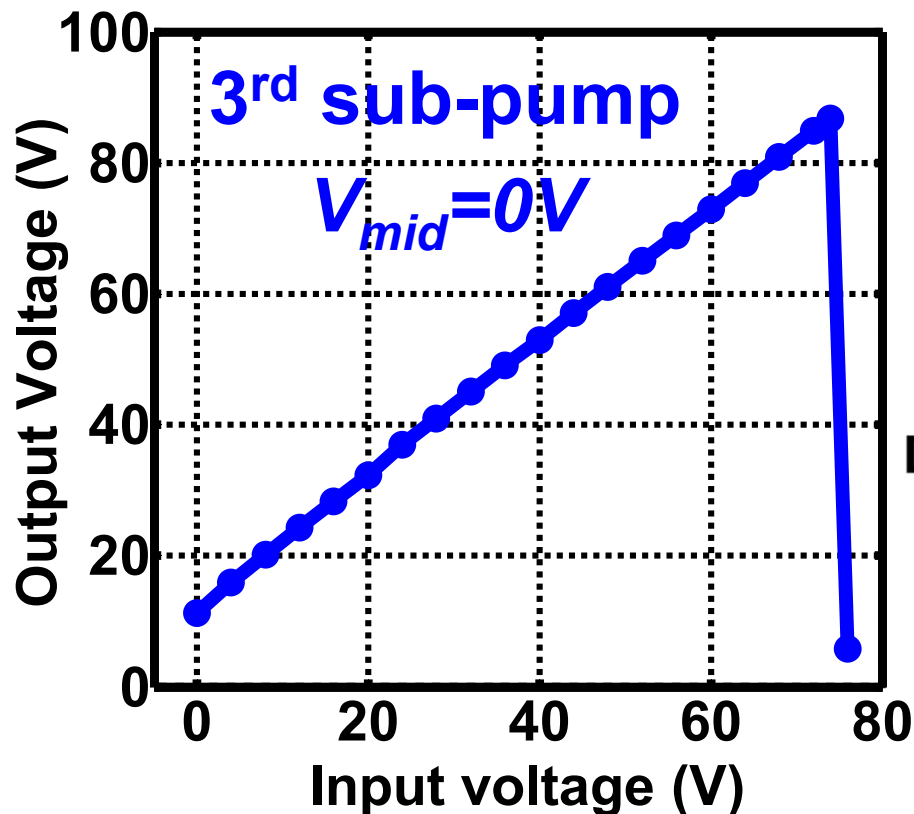
# Measurement Results (1/3)



**All pumps cascaded**  
 $F_{\text{pump}} = 8\text{MHz}$   
**No load condition**

1 <sup>st</sup> sub-pump	2 <sup>nd</sup> sub-pump	3 <sup>rd</sup> sub-pump	Total
0.028mm <sup>2</sup>	0.053mm <sup>2</sup>	0.071mm <sup>2</sup>	0.152mm <sup>2</sup>

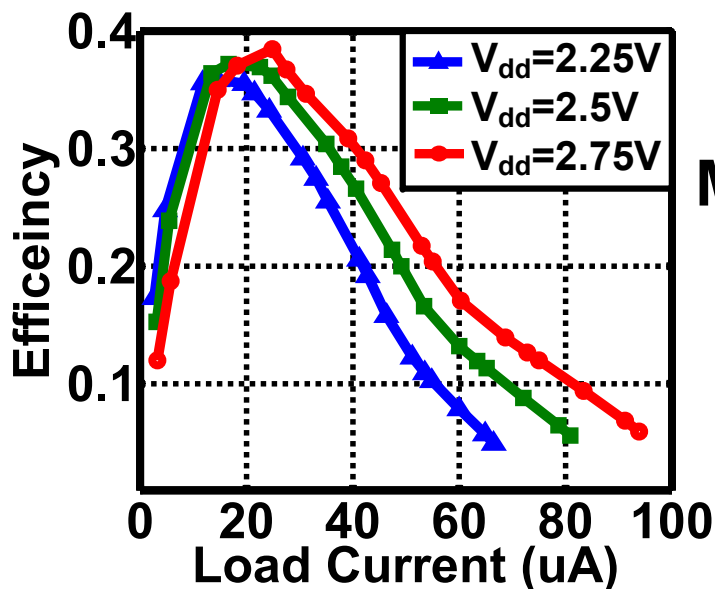
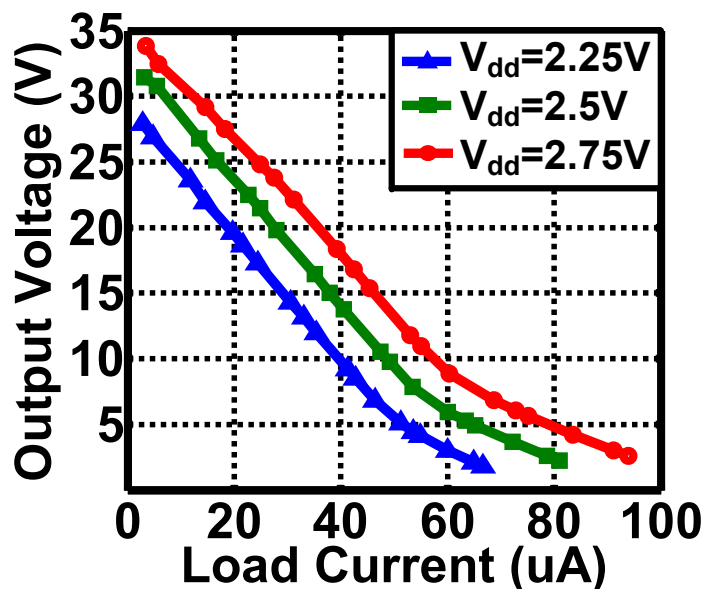
# Measurement Results (2/3)



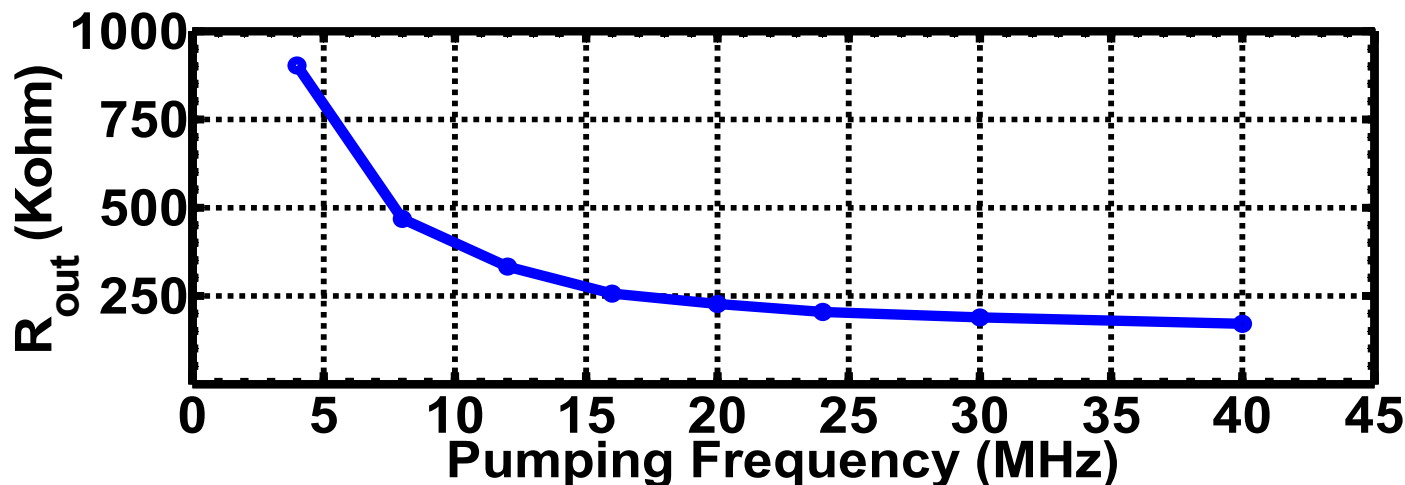
Device failure micrograph

- Clock amplitude and frequency are fixed
- Input voltage is manually ramped

# Measurement Results (3/3)



Measurements  
@  $f_{\text{pump}}=8\text{MHz}$



Measurement  
@  $V_{dd}=2.5V$

# Conclusion

- **A 34V charge pump in 65nm Bulk CMOS represents a 3x improvement in max. voltage**
  - Stacking substrate diodes + All-NMOS CP cell
  - Polysilicon diodes
- **A hybrid architecture enables improved power efficiencies**
- **Device and component reliability carefully preserved**

	Tech.	# of stages	$V_{\text{clk}}$	Voltage range	Eff.	$R_{\text{out}} @ f = 8\text{MHz}$	Area
[3]	0.25 $\mu\text{m}$	4	10V	>43V	--	~ 150K $\Omega$	~0.6mm <sup>2</sup>
This work	65nm	17	2.5V	>34V	38%	370K $\Omega$	0.15mm <sup>2</sup>